



Logic Design – CSE 111

Arithmetic Logic Unit (ALU)

Submitted by:

Name	ID	Program
Carol Farah Nabil	1901478	Sophomore Electrical
Mohamed Salah Abdel-Aziz	1901945	Junior Mechatronics
Mohamed Wagdy Ewiss	1900271	Sophomore Electrical

Examination Committee:

Prof: Hossam Abdelmunim

Eng: Kyrelloss Nashaat



Contents

Introduction.....	4
List of Materials	4
Components Details.....	5
• 4-Bit Adder (74LS283)	5
Pinout:	5
Logic Diagram:	6
• BCD to 7-Segment Decoder (74LS47).....	6
Pinout:	7
7-Segment Display Pinout (Common Anode):	7
Logic Diagram of (74LS47):	8
• 2 to 1 Mux (74LS157).....	9
Pinout:	9
Logic Diagram:	10
• AND Gates (74LS08).....	10
Pinout:	10
Logic Diagram:	11
• OR Gates (74LS32)	11
Pinout:	11
Logic Diagram:	12
• NOT Gates (74LS04)	12
Pinout:	13
Logic Diagram:	13
• 5V Regulator (LM7805).....	14
Pinout:	14
Software Design.....	14
• Full Adder	14



• BCD to 7-Segment Decoder	15
• 2 to 1 Multiplexer	16
• Integrated Circuit.....	16
Hardware Implementation.....	17
Appendix.....	18
References	19

Table of Figures

Figure 1 ALU Diagram	4
Figure 2 4-Bit Adder Pinout	5
Figure 3 1-Bit Full Adder Logic Diagram	6
Figure 4 BCD to 7-Segment Decoder Pinout	7
Figure 5 7-Segment Display Pinout	7
Figure 6 BCD to 7-Segment Decoder Logic Diagram	8
Figure 7 Mux Pinout	9
Figure 8 (2 to 1) Mux Logic Diagram	10
Figure 9 AND Gates Pinout	10
Figure 10 AND Gates Logic Diagram	11
Figure 11 OR Gates Pinout.....	11
Figure 12 OR Gates Logic Diagram	12
Figure 13 NOT Gates Pinout	13
Figure 14 NOT Gates Logic Diagram	13
Figure 15 Regulator Pinout.....	14
Figure 16 Full Adder Blackbox	14
Figure 17 Full Adder Logic Diagram.....	14
Figure 18 BCD to 7-Segment Decoder Blackbox	15
Figure 19 BCD to 7-Segment Decoder Logic Diagram	15
Figure 20 Mux Logic Diagram	16
Figure 21 Mux Blackbox.....	16
Figure 22 ALU Logic Diagram	16
Figure 23 ALU Blackbox	17
Figure 24 ALU Breadboard Implementation	17



Introduction

In general, Arithmetic Logic Unit is a digital circuit used in performing both arithmetic and logic operations. It is also considered a major building unit for a computer's CPU.

Operations of a CPU are being performed through ALUs, that are used in loading data from input registers (a register is a one-bit memory unit). The control unit gives orders to the ALU and instructs it to perform different operations on the data, then the ALU stores the output of such operations in an output register.

Different arithmetic and logic operations are performed by ALUs. Arithmetic operations such as: addition, subtraction, multiplication and division. Logic operations such as: NOT, AND and OR.

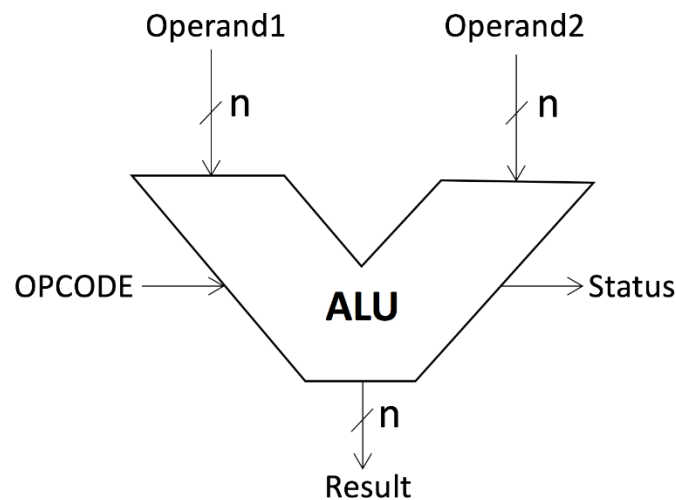


Figure 1 ALU Diagram

Our ALU performs **6** different operations with **two** inputs each has 3-bits:

- Increment
- Addition
- Subtraction
- Complement (one's and two's)
- OR
- AND

List of Materials

Component	Model No.	Quantity
-----------	-----------	----------



4-Bit Adder	74LS283	1
BCD to 7-Segment Decoder	74LS47	1
2 to 1 Multiplexer	74HC157	2
AND Gates	74LS08	1
OR Gates	74LS32	1
NOT Gates	74LS04	1
5V Regulator	LM7805	1
DIP Switch	8-Inputs	4
Push Button	-	3
7-Segment Display	Common Anode	1
LED	-	3
Breadboard	-	3
U-Shaped Wires	-	Kit
Resistors	330 Ω - 1 k Ω	10 - 14

Components Details

- 4-Bit Adder (74LS283)

It is used to perform addition operation between 2 numbers each of 4 bits, as if it contains a combination of half and full single bit adders that cascade together.

Pinout:

- The 4-bit adder IC contains 16 pins.
- Pins 5 and 12 are used to power up IC with +5V and GND terminal of power supply.
- For two 4-bit numbers: A4 A3 A2 A1 and B4 B3 B2 B1.
- Pins 1,3,8,10 are input pins and are used to feed A4 A3 A2 A1.
- Pins 16,4,7,11 are input pins and are used to feed B4 B3 B2 B1.
- Pin 13 is an input pin and is used to feed the carry in.
- Pins 15,2,6,9 are output pins and are used to observe the addition output of the two 4-bit numbers: S4 S3 S2 S1.

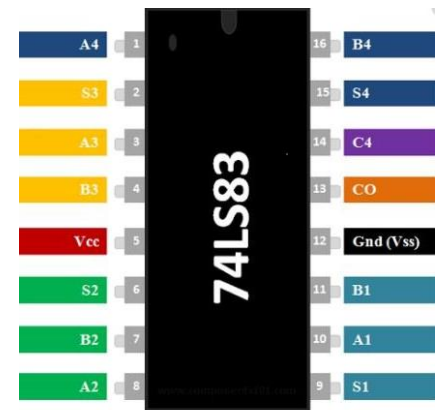


Figure 2 4-Bit Adder Pinout



- Pin 14 is an output pin and displays the carry out resulting from addition.

Logic Diagram:

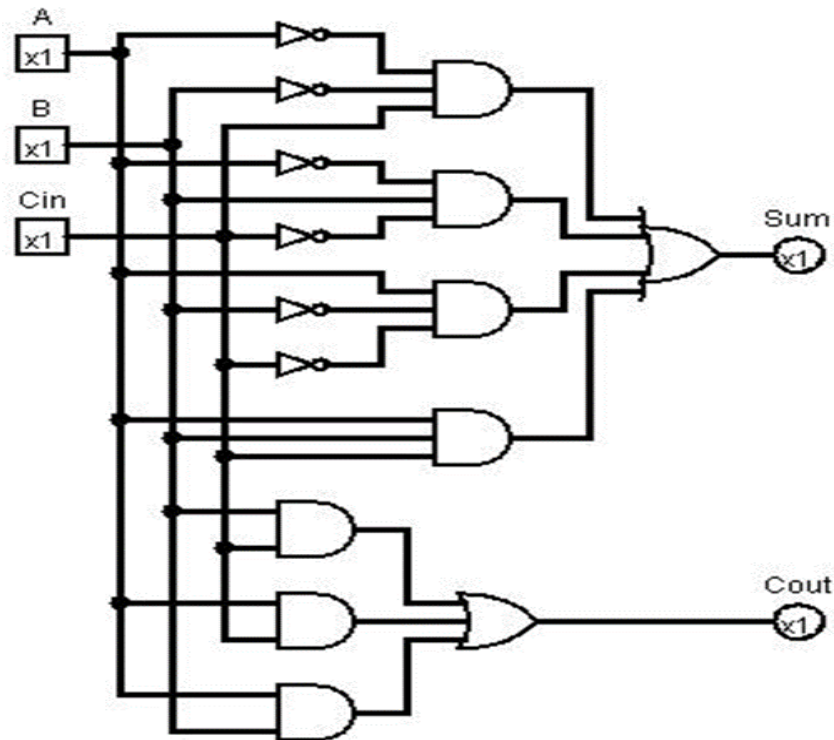


Figure 3 1-Bit Full Adder Logic Diagram

- BCD to 7-Segment Decoder (74LS47)

A decoder is a circuit that translates the input code into a set of output signals. An important type of decoder is the line decoder that takes n -digit binary numbers and decodes it into 2^n data lines. It can have an enable signal.



Pinout:

- Pins 1,2,6,7 (A,B,C,D) are 4 BCD inputs
- Pin 3 is lamp test input that is used to test the display.
- Pin 4 is blanking input that is used to turn off or control the brightness.
- Pin 5 is for Latch Enable or Strobe input that is used to store BCD code.
- Pin 8 is GND and pin 16 is positive power supply (Vcc).
- Pins 9, 10, 11, 12, 13, 14, 15 (a,b,c,d,e,f,g) are seven segment outputs.

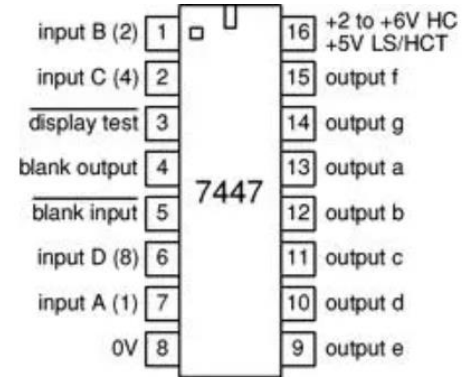


Figure 4 BCD to 7-Segment Decoder Pinout

7-Segment Display Pinout (Common Anode):

- The Seven-segment consists of 7 LEDs arranged in a way that allows constructing a display of the numbers of (0-9). It has 10 pins assigned as follows:
- 7 pins act as the Vcc for the 7 LEDs (1 pin for each LED, assuming that we are dealing with common cathode seven segment display)
- 1 pin is the VCC for decimal point display at the lower right corner.
- 2 pins represent a common ground to all the LEDs.

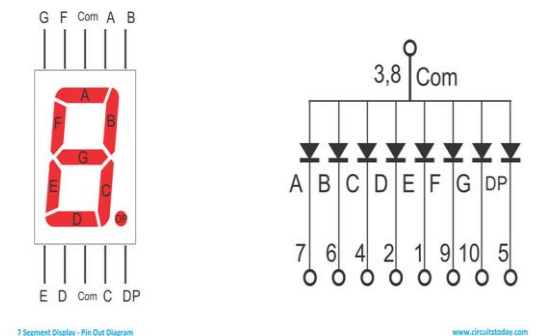


Figure 5 7-Segment Display Pinout



Logic Diagram of (74LS47):

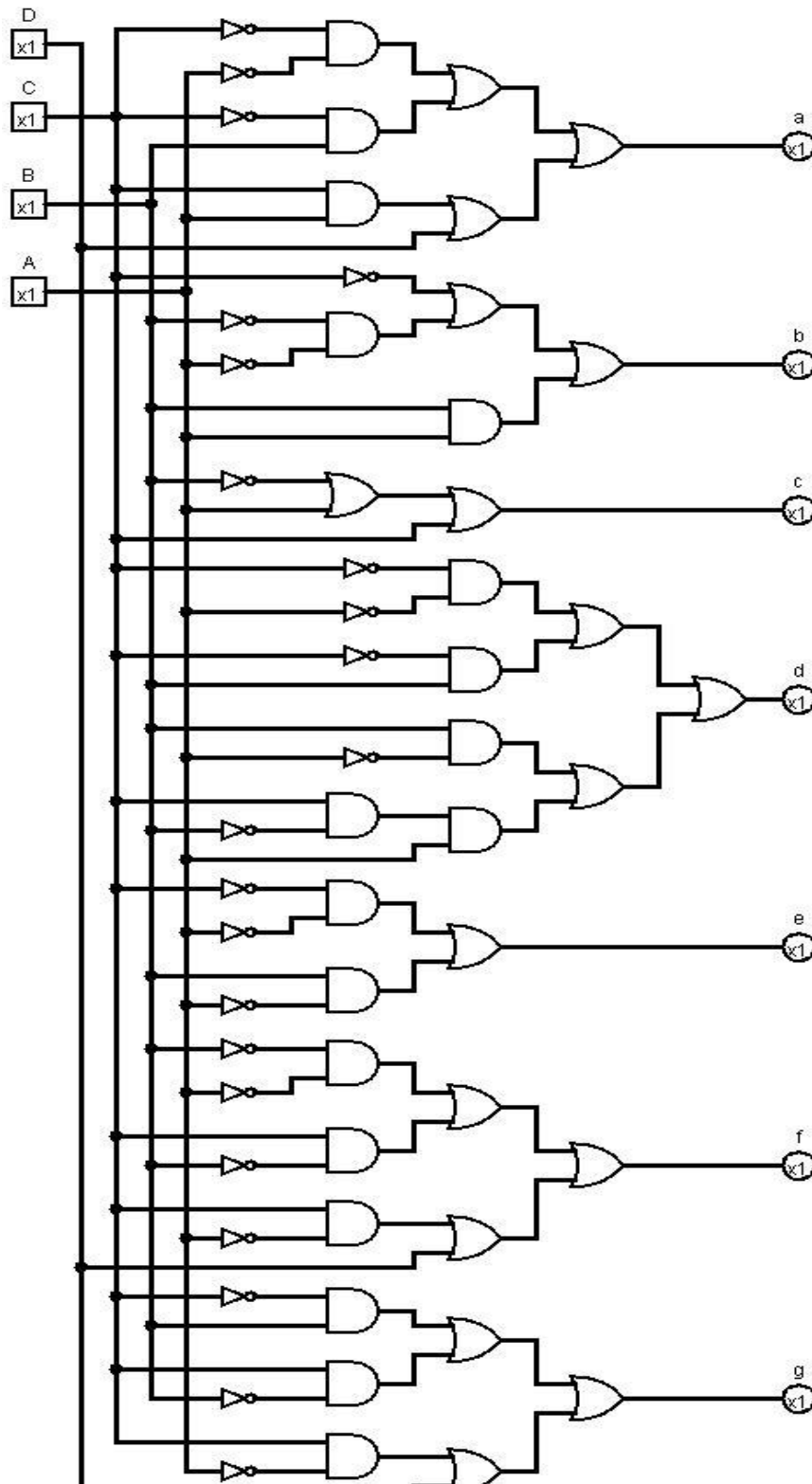


Figure 6 BCD to 7-Segment Decoder Logic Diagram

- 2 to 1 Mux (74LS157)

- This type of mux has 2 inputs and one output. It selects from two incoming signals using data from selection lines (a control input) to combine the incoming signals on one output line. The resulted output signal is transmitted. For n selection lines, we have 2^n inputs.

- It is an IC consisting of four 2-inputs digital multiplexers inside the chip with 2 control inputs (enable and select). In this shown pinout diagram, there are four multiplexer channels given different colors. It has 16 pins and a common power supply for all multiplexers. Input voltage range is from 1.35V to 3.15V.

Pinout:

- Pin 1 is select, it is used to select the input lines from which the data is presented at the outputs.
- Pins 2,5,11, 14 are the input A of the four 2 to1 multiplexers.
- Pins 3,6,10, 13 are the input B of the four 2 to 1 multiplexers.
- Pins 4,7,9, 12 are the output pins of multiplexers.
- Pin 8 is GND, connected to the ground of the circuit.
- Pin 15 is Strobe ,it is active low and it is responsible for enabling or disabling outputs.
- Pin 16 is the positive power supply (Vcc).



Figure 7 Mux Pinout



Logic Diagram:

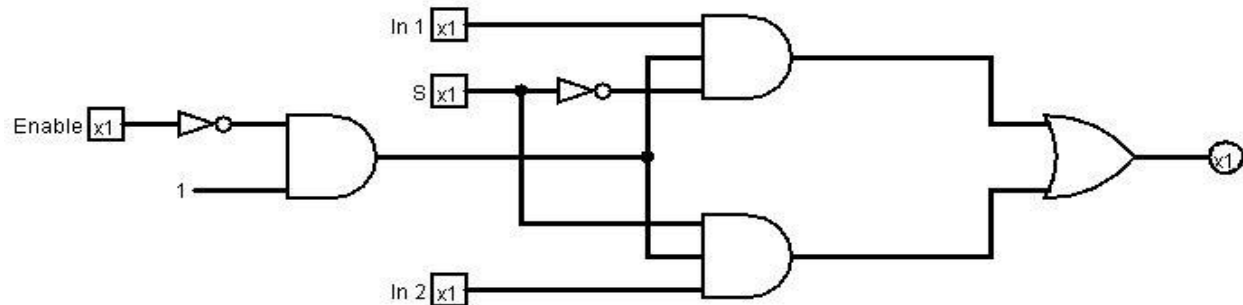


Figure 8 (2 to 1) Mux Logic Diagram

- AND Gates (74LS08)

Quadruple 8-bit Two Input AND IC, In AND gates there are two logic state signals: HIGH (3-5 Volts) and LOW (0-2.6 Volts). Each AND gate uses two input pins and a single output pin.

Pinout:

- Pin 1 (A1) is used as the first input pin for the first AND gate.
- Pin 2 (B1) is used as the second input pin for first AND gate.
- Pin 3 (Y1) is the output of the first AND gate is received at Pin 3.
- Pin 4 (A2) is used as the first input pin of second AND gate.
- Pin 5 (B2) is used as the second input to the second AND gate.
- Pin 6 (Y2) is used to receive the output of second AND gate.
- Pin 7 (GND) is a ground pin that is used as a common ground by the communication devices and the Power Supply.
- Pin 8 (Y3) is used to receive the output of third AND gate.
- Pin 9 (A3) is used as the first input to the third AND gate.



Figure 9 AND Gates Pinout



- Pin 10 (B3) is used as the second input to the third AND gate.
- Pin 11 (Y4) is used to receive the output of fourth AND gate.
- Pin 12 (A4) is used as the first input pin of forth AND gate.
- Pin 13 (B4) is used as the second input pin of forth AND gate.
- Pin 14 (Vcc) The Positive Power Supply is to be provided at pin 14 to make the IC functional.

Logic Diagram:

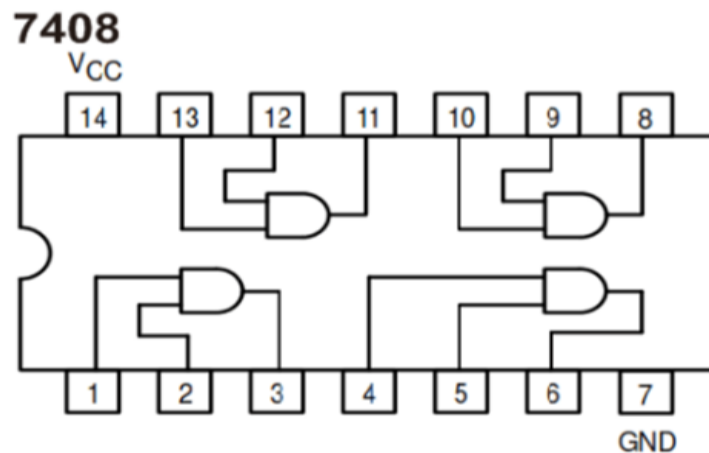


Figure 10 AND Gates Logic Diagram

- OR Gates (74LS32)

Quad 2-Input Logic OR Gates, Supply Voltage 7V and Input Voltage 5.5V.

Pinout:

- Pin1 A Input Gate 1
- Pin 2 B Input Gate 1
- Pin 3 Y Output Gate 1
- Pin 4 A Input Gate 2
- Pin 5 B Input Gate 2
- Pin 6 Y Output Gate 2



Figure 11 OR Gates Pinout



- Pin 7 Ground
- Pin 8 Y Output Gate 3
- Pin 9 A Input Gate 3
- Pin 10 B Input Gate 3
- Pin 11 Y Output Gate 4
- Pin 12 A Input Gate 4
- Pin 13 B Input Gate 4
- Pin 14 Vcc – Positive Power Supply

Logic Diagram:

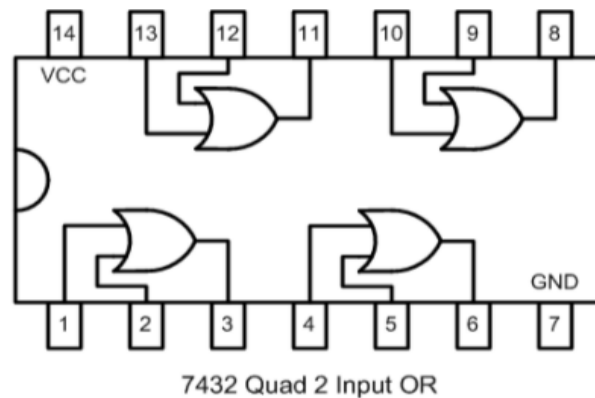


Figure 12 OR Gates Logic Diagram

- NOT Gates (74LS04)

It is an inverter whose basic functions is to invert/convert the incoming logic weather it is HIGH or LOW. It has six internal inverters. Supply voltage range for IC is 4.75V to 5.25V.



Pinout:

- Pin 1 (1A) is used as an input pin for the first OR gate.
- Pin 2 (1Y) gives the output of the first OR gate.
- Pin 3 (2A) is used as an input for the second OR gate.
- Pin 4 (2Y) gives the output of the second OR gate.
- Pin 5 (3A) is used as an input for the third OR gate.
- Pin 6 (3Y) gives the output of the third OR gate.
- Pin 7 (GND) is used as a common ground pin.
- Pin 8 (4Y) gives the output of the fourth OR gate.
- Pin 9 (4A) is used as an input for the fourth OR gate.
- Pin 10 (5Y) gives the output of the fifth OR gate.
- Pin 11 (5A) is used as an input for the fifth OR gate.
- Pin 12 (6Y) gives the output of the sixth OR gate.
- Pin 13 (6A) is used as an input for the sixth OR gate.
- Pin 14 (Vcc) is used as a positive power supply. It is used to provide the power to the IC in order to make it functional.



Figure 13 NOT Gates Pinout

Logic Diagram:

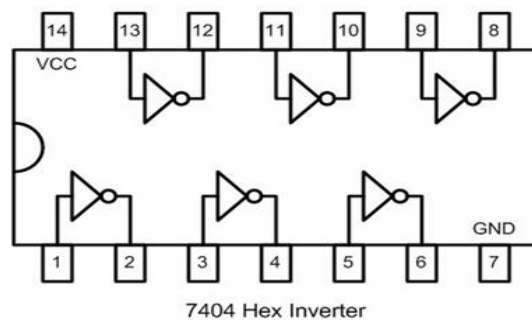


Figure 14 NOT Gates Logic Diagram

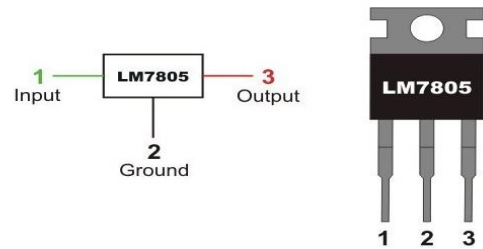


- 5V Regulator (LM7805)

Pinout:

- Pin 1 is connected to the input power source
- Pin 2 is connected to the ground
- Pin 3 is connected to the circuit

LM7805 PINOUT



ECSTUFF4U.COM

Figure 15 Regulator Pinout

Note: For further information about these components, you can find their datasheets links at the [appendix](#).

Software Design

- Full Adder

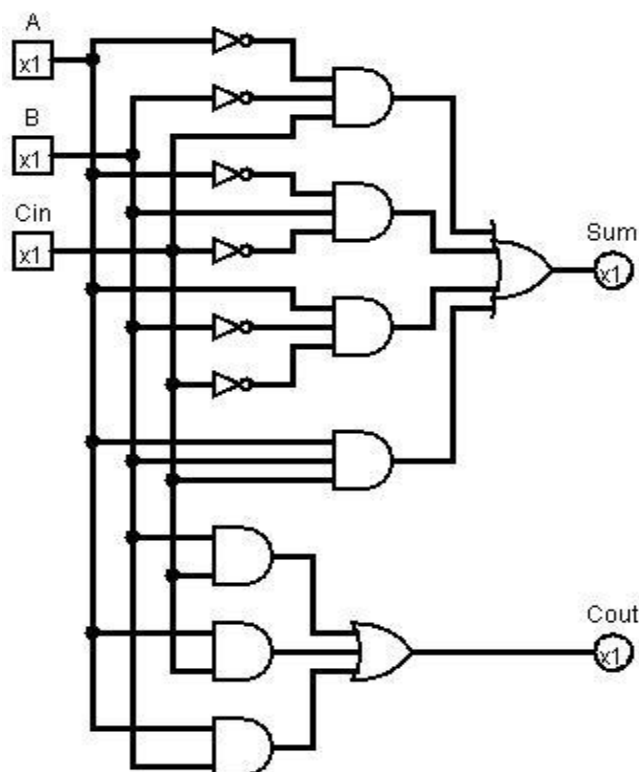


Figure 17 Full Adder Logic Diagram

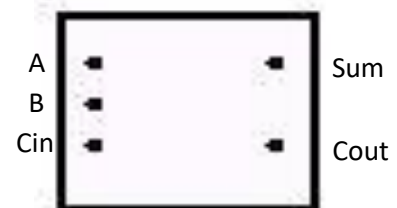


Figure 16 Full Adder Blackbox



- BCD to 7-Segment Decoder

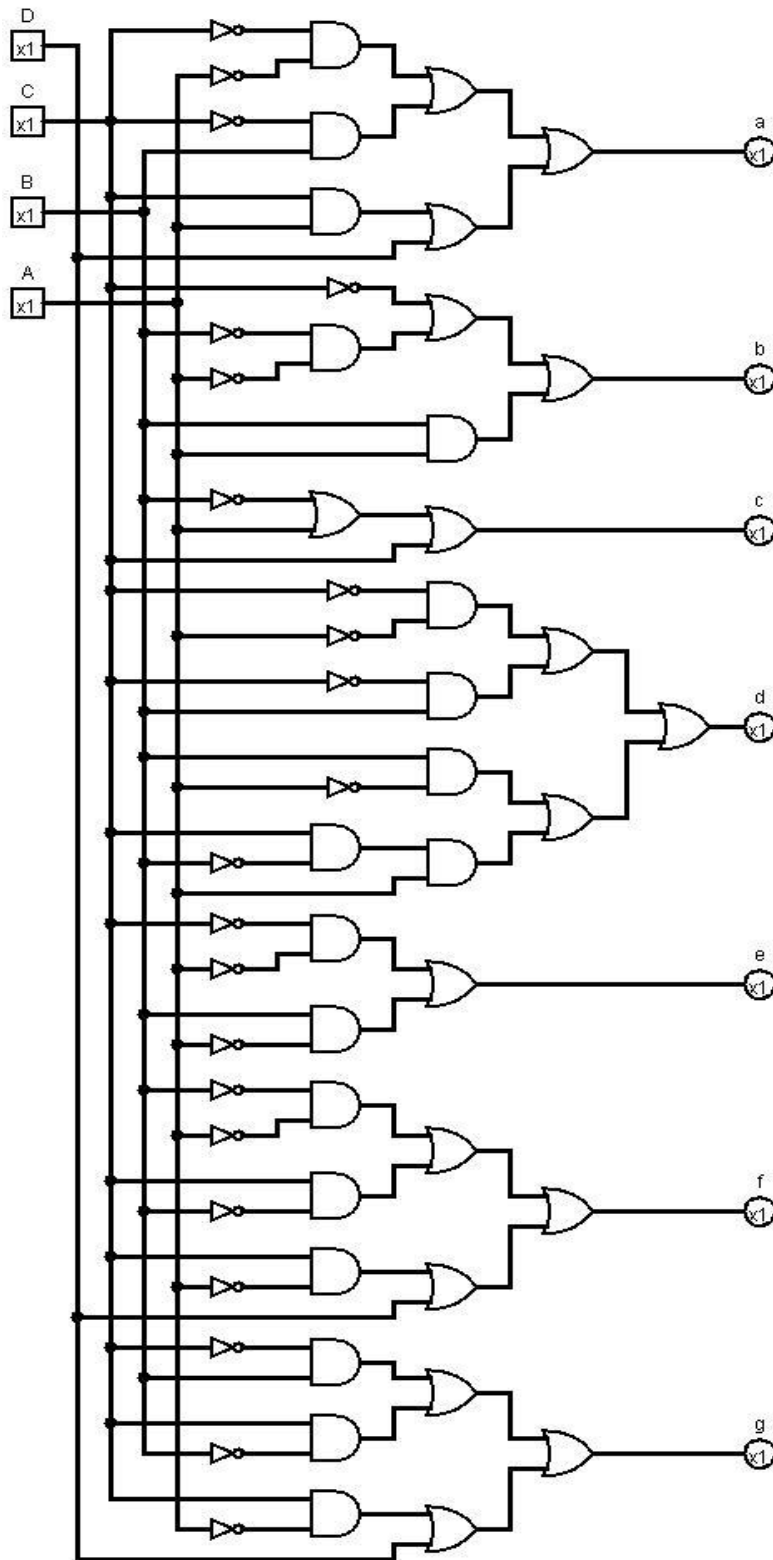


Figure 19 BCD to 7-Segment Decoder Logic Diagram

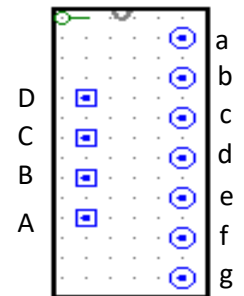


Figure 18 BCD to 7-Segment
Decoder Blackbox



• 2 to 1 Multiplexer

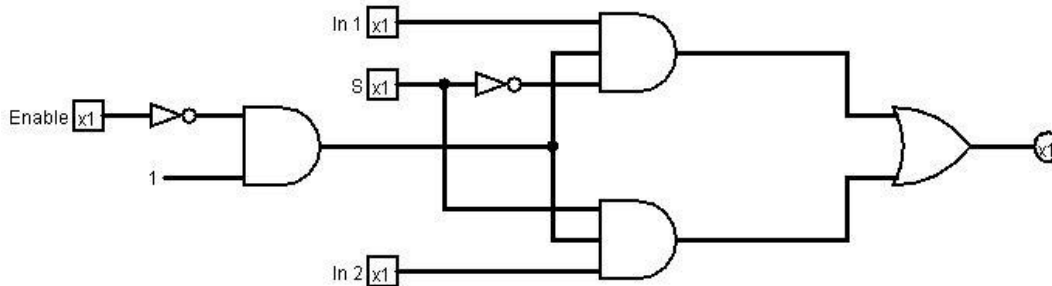


Figure 20 Mux Logic Diagram

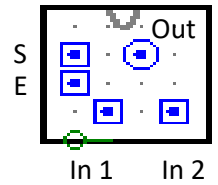
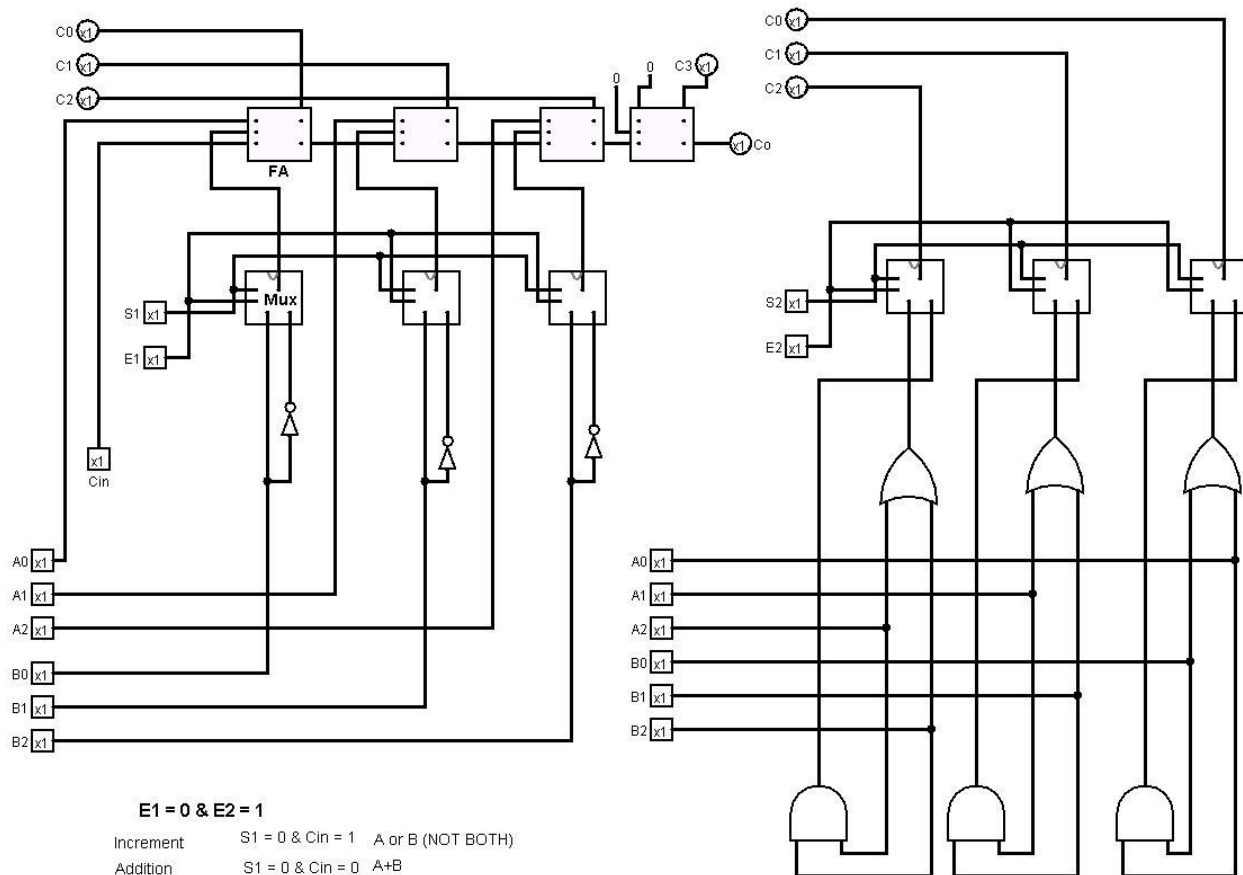


Figure 21 Mux
Blackbox

• Integrated Circuit



E1 = 0 & E2 = 1

Increment	$S1 = 0 \text{ \& } Cin = 1$	A or B (NOT BOTH)
Addition	$S1 = 0 \text{ \& } Cin = 0$	A+B
Subtraction	$S1 = 1 \text{ \& } Cin = 1$	A-B
1's Complement	$S1 = 1 \text{ \& } Cin = 0$	B & A is 0
2's Complement	$S1 = 1 \text{ \& } Cin = 1$	B & A is 0

E1 = 1 & E2 = 0

A OR B	$S2 = 0$
A AND B	$S2 = 1$

Figure 22 ALU Logic Diagram

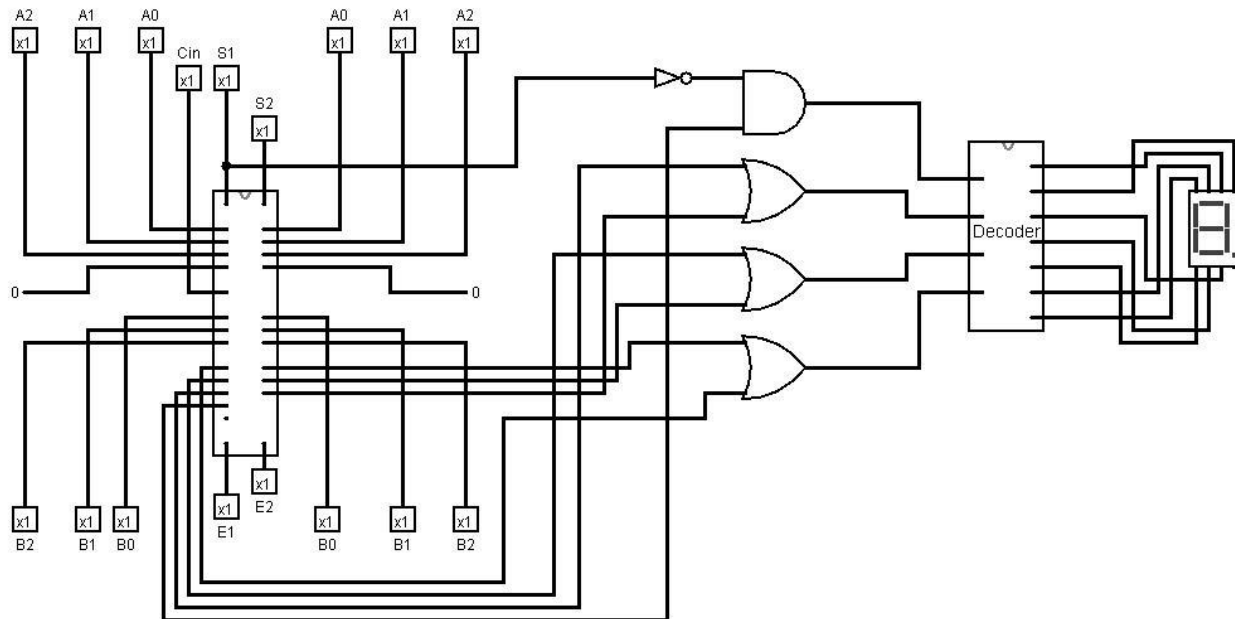


Figure 23 ALU Blackbox

Hardware Implementation

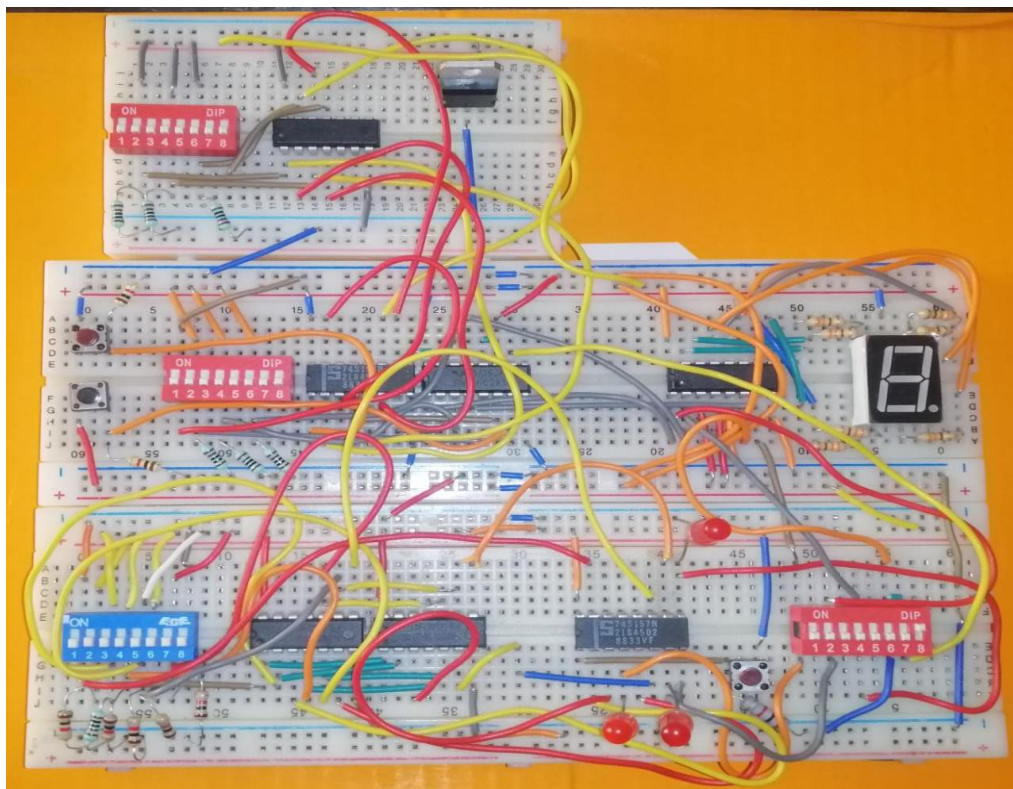


Figure 24 ALU Breadboard Implementation



Appendix

A. 4-Bit Adder (74LS283)

<https://mil.ufl.edu/4712/docs/sn74ls283rev5.pdf>

B. 2 to 1 Mux (74LS157)

<https://cdn.shopify.com/s/files/1/0672/9409/files/74HC157.pdf?v=1597483331>

C. BCD to 7-Segment Decoder (74LS47)

https://www.ti.com/lit/ds/symlink/sn5447a.pdf?ts=1631825439178&ref_url=http%253A%252F%252Fwww.google.com%252F

D. AND Gates (74LS08)

<https://www.ti.com/lit/ds/symlink/sn74ls08.pdf>

E. OR Gates (74LS32)

https://www.ti.com/lit/ds/symlink/sn54ls32-sp.pdf?ts=1631868000986&ref_url=https%253A%252F%252Fwww.google.com%252F

F. NOT Gates (74LS04)

<https://www.ti.com/lit/ds/symlink/sn74ls04.pdf>

G. 5V Regulator (LM7805)

<https://www.ecstuff4u.com/2019/09/lm7805-pinout.html>



References

- 1- <https://github.com/ardasdasdas/logisim>
- 2- <https://www.circuitstoday.com/7-segment-display-to-avr-atmega32-using-cd4511b>
- 3- <https://github.com/marceloboeira/logisim-7-segment-display-driver>
- 4- <https://www.componentsinfo.com/7805-pinout-datasheet/>
- 5- [https://techmonitor.ai/what-is/what-is-alu-4997649#:~:text=In%20computing%2C%20an%20ALU%20\(Arithmetic,couered%20through%20the%20arithmetic%20processes.](https://techmonitor.ai/what-is/what-is-alu-4997649#:~:text=In%20computing%2C%20an%20ALU%20(Arithmetic,couered%20through%20the%20arithmetic%20processes.)
- 6- [https://en.wikipedia.org/wiki/Arithmetic logic unit](https://en.wikipedia.org/wiki/Arithmetic_logic_unit)
- 7- <https://components101.com/ics/74ls32-or-gate-datasheet-pinout-and-specs>
- 8- <https://components101.com/ics/74ls83-4-bit-full-adder-ic>
- 9- [https://www.wavelengthelectronics.co.uk/news/76-eswitch-dip-switches#:~:text=A%20DIP%20switch%20is%20a,or%20circle%20\(rotary%20DIP\).](https://www.wavelengthelectronics.co.uk/news/76-eswitch-dip-switches#:~:text=A%20DIP%20switch%20is%20a,or%20circle%20(rotary%20DIP).)
- 10- <https://ieeexplore.ieee.org/document/7570930>
- 11- <https://ece.umaine.edu/wp-content/uploads/sites/203/2012/05/ALU.pdf>
- 12- https://digitalcommons.lsu.edu/cgi/viewcontent.cgi?article=3890&context=gradschool_theses