Cairo University - Faculty of Engineering
Computer Engineering Department
Computer Architecture

[Computer Architecture Project]
[CMP 301B]

Submitted by:

Name	Sec	BN
اريج رافت زاهر عبدالرحمن	1	11
اندرو تاوضروس حنا خليل	1	14
مارك مدحت عبده حنين	2	11
محمد سامى محمد محمود	2	18

Academic Year
2020-2021

Instruction format

1. Opcode of each instruction:

Instruction	Opcode
One Operand	
NOP	00000
SETC	00001
CLRC	00010
CLRC Rdst	00011
NOT Rdst	00100
INC Rdst	00101
DEC Rdst	00110
NEG Rdst	00111
OUT Rdst	01000
IN Rdst	01001
Two Operand	
MOV Rsrc, Rdst	01010
ADD Rsrc, Rdst	01011
SUB Rsrc, Rdst	01100
AND Rsrc, Rdst	01101
OR Rsrc, Rdst	01110
IADD Rdst,Imm	01111
SHL Rsrc, Imm	10000
SHR Rsrc, Imm	10001
RLC Rdst	10010
RRC Rdst	10011
Memory Operations	
PUSH Rdst	10100
POP Rdst	10101
LDM Rdst, Imm	10110
LDD Rdst, offset (Rsrc)	10111
STD Rsrc1, offset (Rsrc2)	11000
Branch and Change of Control Operations	
JZ Rdst	11001
JN Rdst	11010
JC Rdst	11011
JMP Rdst	11100
CALL Rdst	11101
RET	11110
DEC SP (transparent instruction)	11111

2. **Instruction bits details:**

One operand (NOP, SETC, CLRC, DEC SP)

Opcode 5 bits	0 27 bits

One operand (CLR, NOT, INC, DEC, NEG, OUT, IN)

Opcode 5 bits	Rdst 3 bits	Rdst 3 bits	0 21 bits

Two operands (MOV, ADD, SUB, AND, OR)

Opcode 5 bits	Rsrc 3bits	Rdst 3 bits	0 21 bits

Two operands (IADD)

Opcode 5 bits	Rdst 3 bits	Rdst 3 bits	0 5 bits
Imm 16 bits			

Two operands (SHL, SHR)

Opcode 5 bits	Rsrc 3 bits	Rsrc 3 bits	0 5 bits
Imm 16 bits			

Two operands (RLC, RRC)

Opcode 5 bits	Rdst 3 bits	Rdst 3 bits	0 21 bits

Memory (PUSH, POP)

Opcode 5 bits	Rdst 3 bits	Rdst 3 bits	0 21 bits

Memory (LDM)

Opcode 5 bits	Rdst 3 bits	Rdst 3 bits	0 5 bits
Imm 16 bits			

Memory (LDD)

Opcode 5 bits	Rsrc 3 bits	Rdst 3 bits	0 5 bits
offset 16 bits			

Memory (STD)

Opcode 5 bits	Rsrc2 3 bits	Rsrc1 3 bits	0 5 bits
offset 16 bits			

Branches and Control Operations (JZ, JN, JC, JMP, CALL)

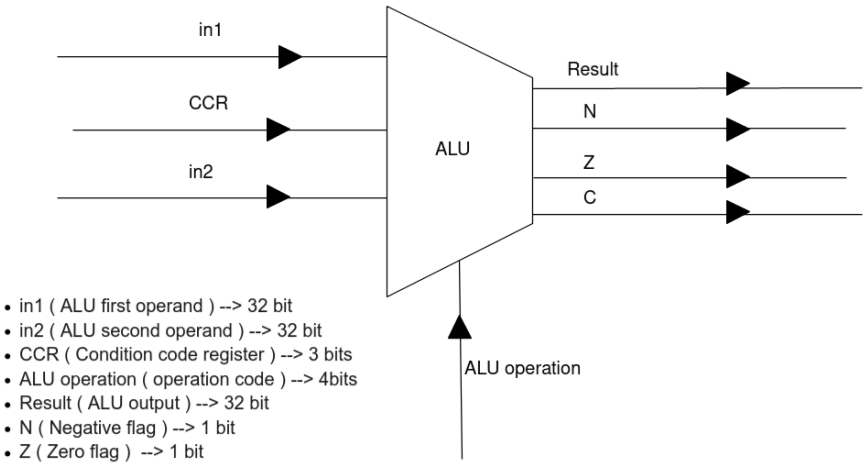
Opcode 5 bits	Rdst 3 bits	Rdst 3 bits	0 21 bits

Branches and Control Operations (RET)

Opcode 5 bits	0 27 bits

Schematic diagram of the processor

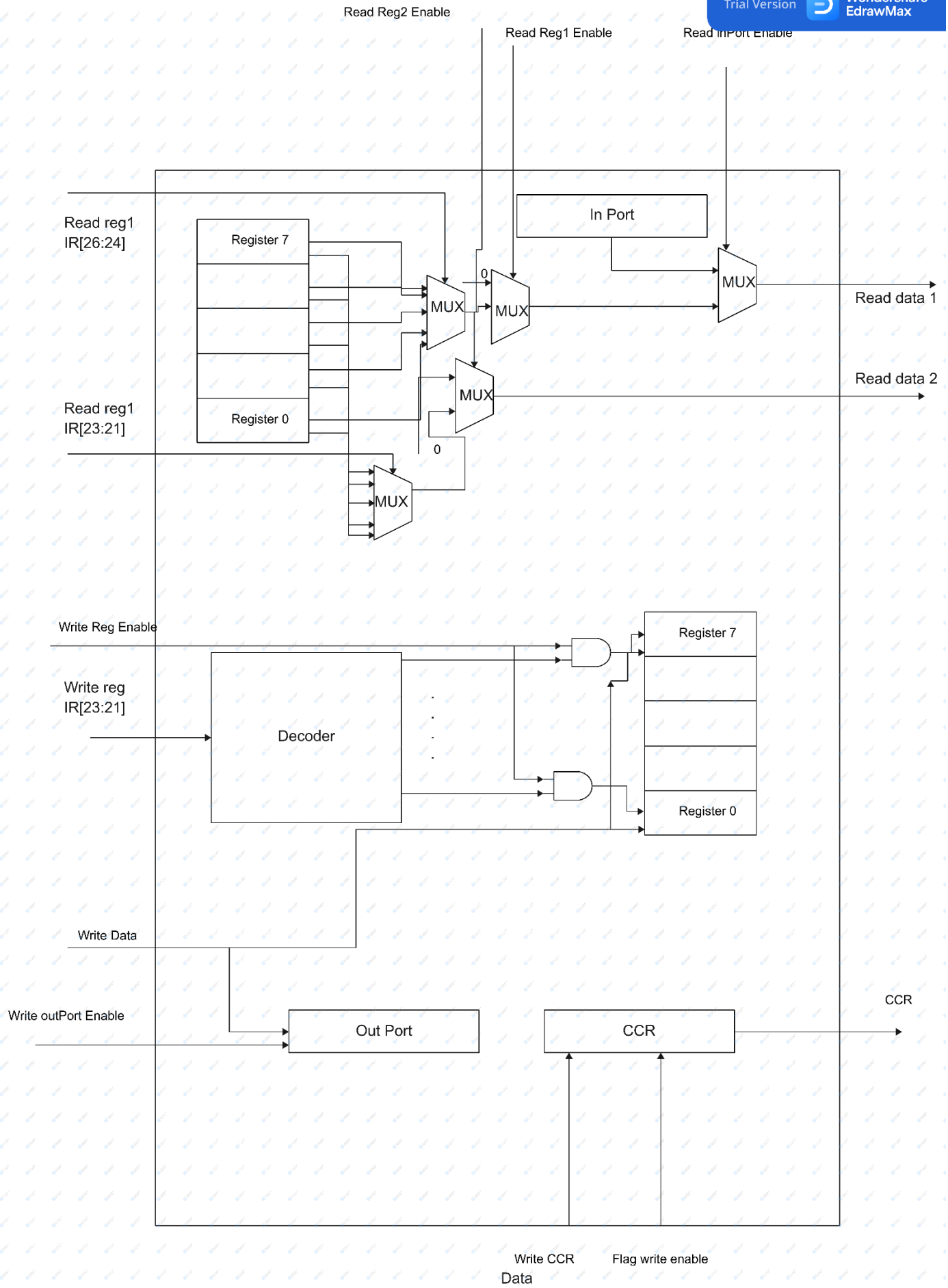
1. ALU Details



- in1 (ALU first operand) --> 32 bit
- in2 (ALU second operand) --> 32 bit
- CCR (Condition code register) --> 3 bits
- ALU operation (operation code) --> 4bits
- Result (ALU output) --> 32 bit
- N (Negative flag) --> 1 bit
- Z (Zero flag) --> 1 bit
- C (Carry flag) --> 1 bit

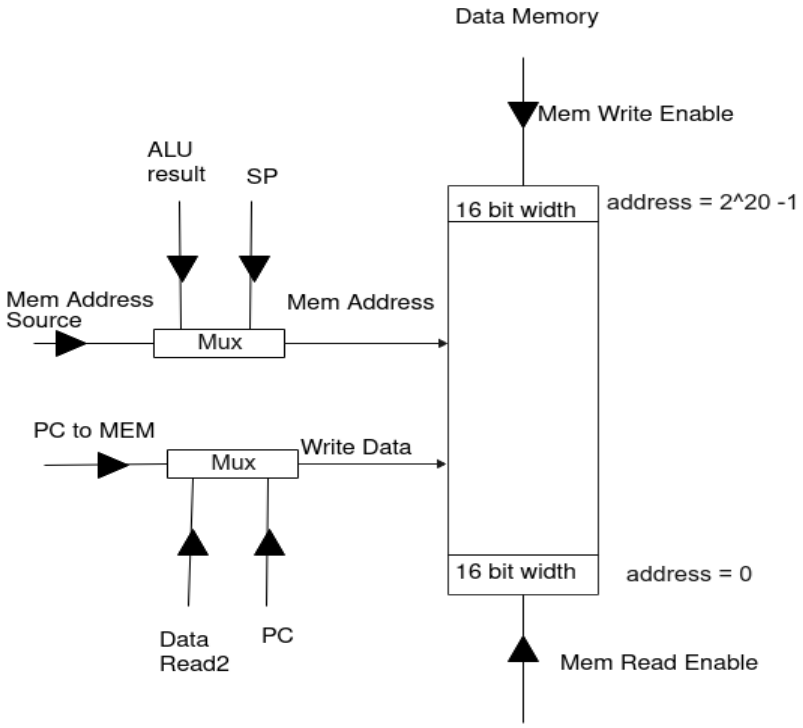
Operation	Operation Code	Description	Flags effect		
			C	N	Z
Clear	0000	Result = clear in1 = 0	C	N	1
Not	0001	Result = 1's complement of in 1	C	1/0	1/0
Inc	0010	Result = in1 +1	C	1/0	1/0
Dec	0011	Result = in1 -1	C	1/0	1/0
Neg	0100	Result = 2's complement of in1	C	1/0	1/0
Add	0101	Result = in1 + in2	1/0	1/0	1/0
Sub	0110	Result = in1 – in2	1/0	1/0	1/0
And	0111	Result = in 1 and in2	C	1/0	1/0
Or	1000	Result = in1 or in2	C	1/0	1/0
Shl	1001	Result = in1 shifted left by in2	1/0	N	Z
Shr	1010	Result = in1 shifted right by in2	1/0	N	Z
Rlc	1011	Result = {in1[30:0], CarryIn}	In1 [31]	N	Z
Rrc	1100	Result = {CarryIn, in1 [31:1]}	In1 [0]	N	Z
Select in1	1101	Result = in1	C	N	Z
Select in2	1110	Result = in2	C	N	Z
Set C	1111	Result = x (in1)	1	N	Z

2. Registers Details

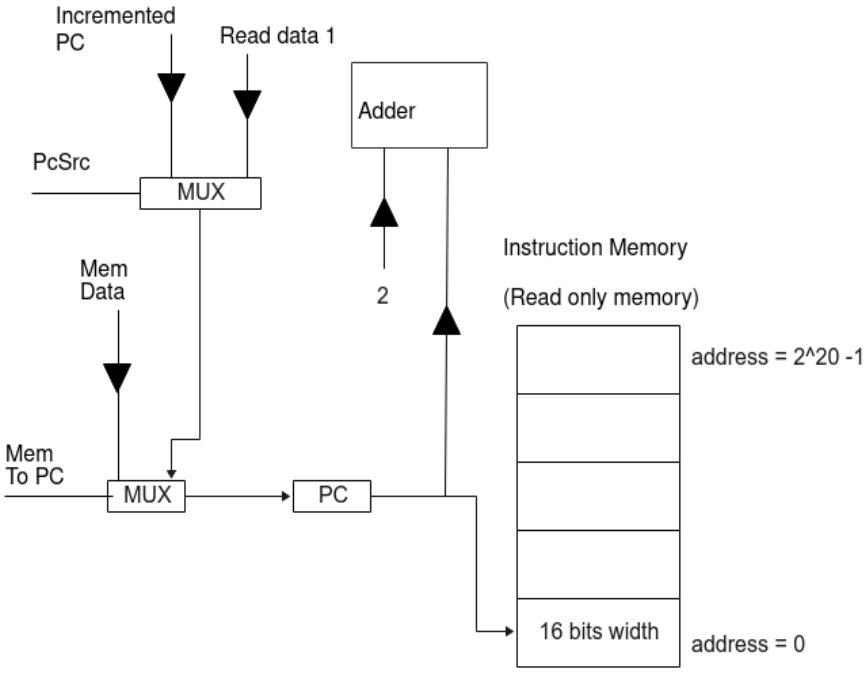


3. Memory Blocks

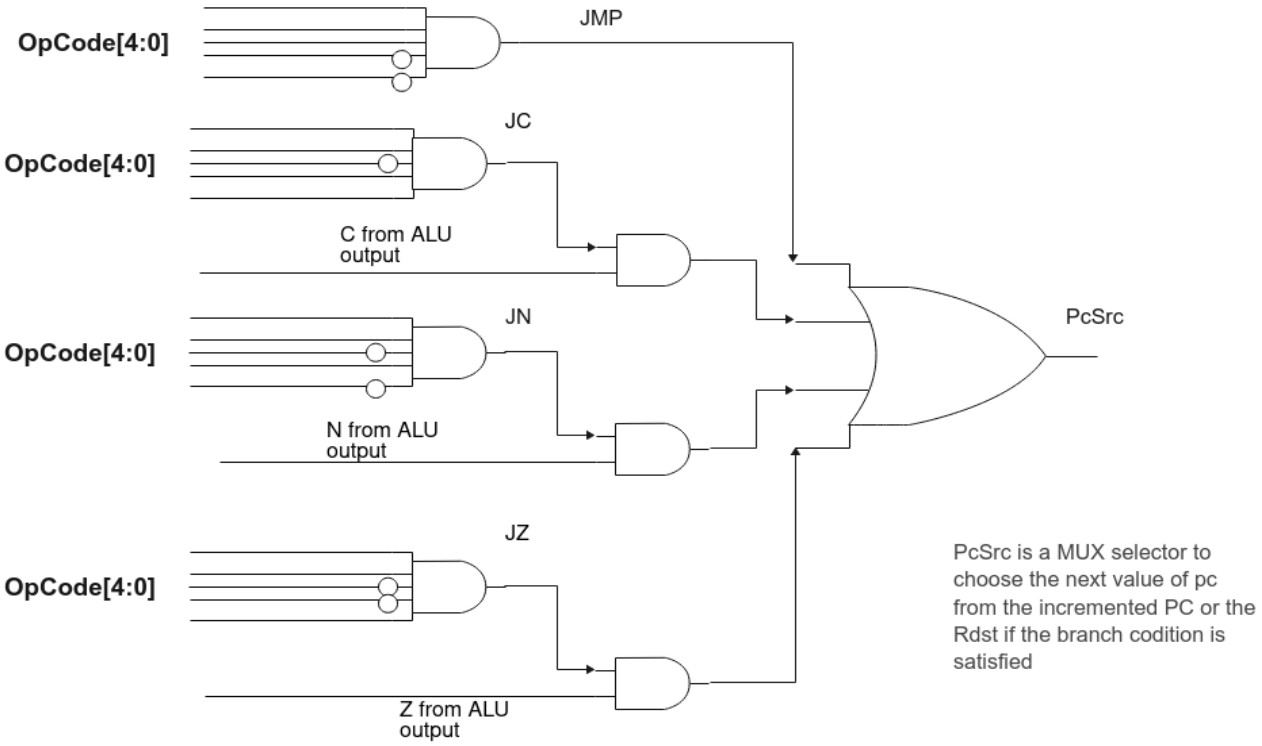
I. Data Memory



II. Instructions Memory

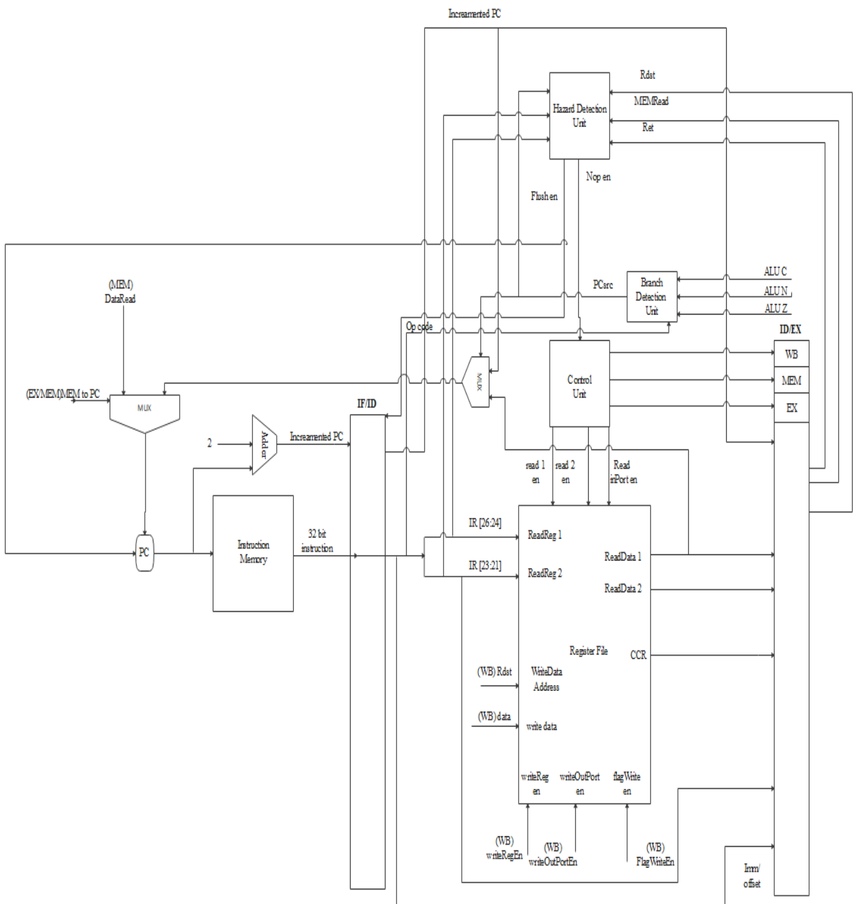


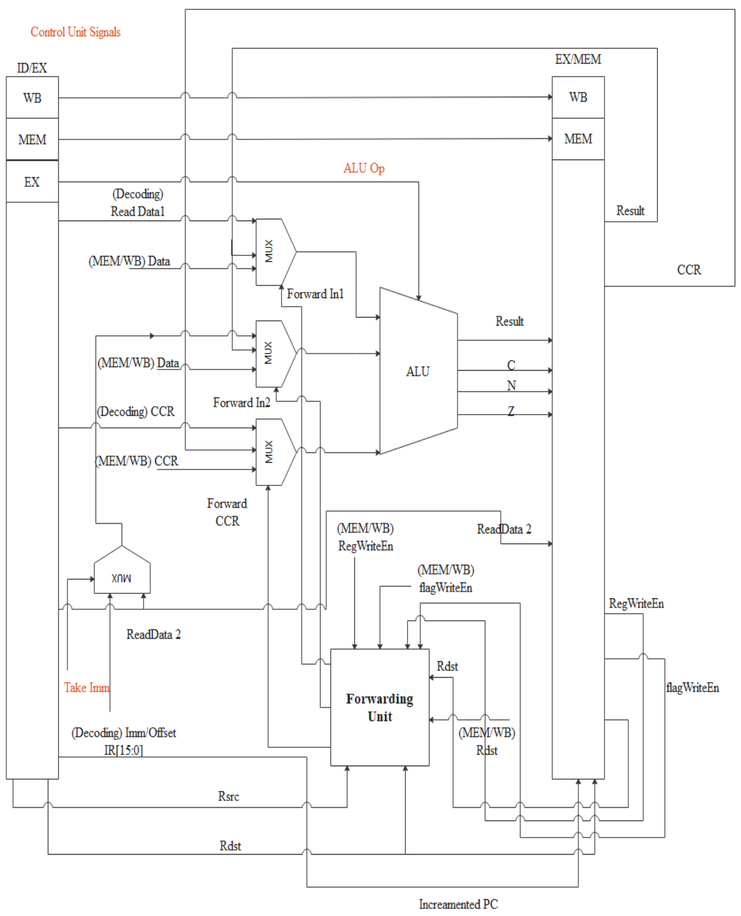
4. Branch detection

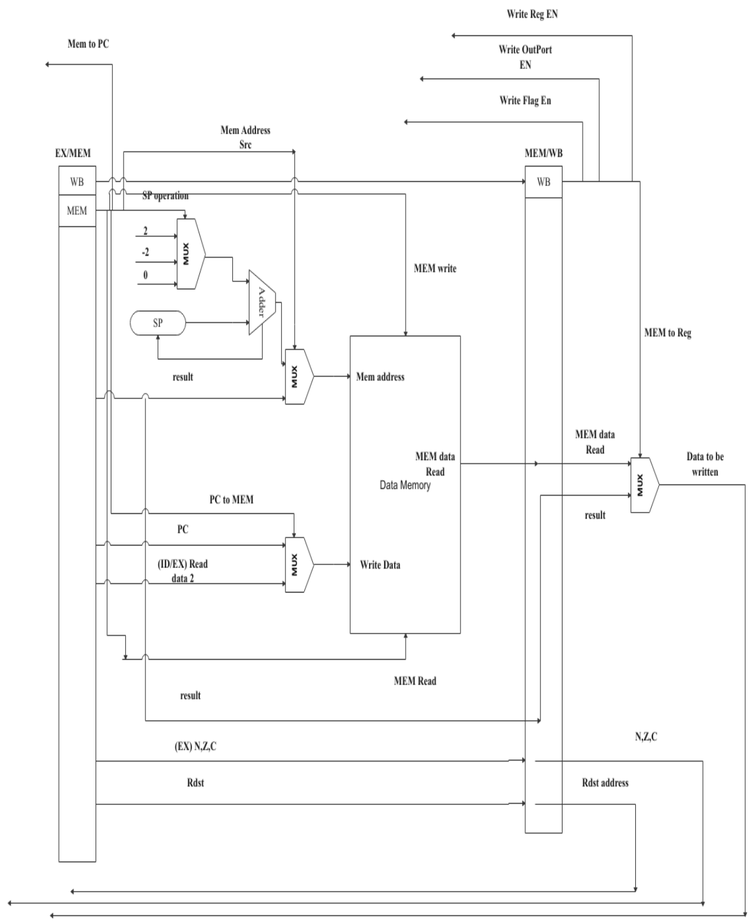


Note: This Circuit will take place in the decode stage

5. Processor Schema







6. Control Unit

Inst.	Read 1	Read 2	Write reg	Read in port	Write out port	Flag write	Take immediate	Alu Op.	Mem Read	Mem write	Mem address src (sp or address)	Mem to Reg	SP Operation (INC/DEC/NOP)	Mem to PC	Pc to Mem	RET
Nop	0	0	0	0	0	0	0	xxxx	0	0	x	x	00	0	0	0
setc	0	0	0	0	0	1	0	1111	0	0	x	x	00	0	0	0
clrc	0	0	0	0	0	1	0	0101	0	0	x	x	00	0	0	0
Clr dst	1	0	1	0	0	1	0	0000	0	0	x	0	00	0	0	0
Not dst	1	0	1	0	0	1	0	0001	0	0	x	0	00	0	0	0
Inc dst	1	0	1	0	0	1	0	0010	0	0	x	0	00	0	0	0
Dec dst	1	0	1	0	0	1	0	0011	0	0	x	0	00	0	0	0
Neg dst	1	0	1	0	0	1	0	0100	0	0	x	0	00	0	0	0
Out dst	1	0	0	0	1	0	0	1101	0	0	x	0	00	0	0	0
In dst	0	0	1	1	0	0	0	1101	0	0	x	0	00	0	0	0
Rlc dst	1	0	1	0	0	1	0	1011	0	0	x	0	00	0	0	0
Rrc dst	1	0	1	0	0	1	0	1100	0	0	x	0	00	0	0	0
Mov src,dst	1	0	1	0	0	0	0	1101	0	0	x	0	00	0	0	0
Add src,dst	1	1	1	0	0	1	0	0101	0	0	x	0	00	0	0	0
Sub src , dst	1	1	1	0	0	1	0	0110	0	0	x	0	00	0	0	0
And src,dst	1	1	1	0	0	1	0	0111	0	0	x	0	00	0	0	0
Or src,dst	1	1	1	0	0	1	0	1000	0	0	x	0	00	0	0	0
Iadd dst , imm	1	0	1	0	0	1	1	0101	0	0	x	0	00	0	0	0
Shl src,imm	1	0	1	0	0	1	1	1001	0	0	x	0	00	0	0	0
Shr src,imm	1	0	1	0	0	1	1	1010	0	0	x	0	00	0	0	0
Push dst	0	1	0	0	0	0	0	1101	0	1	0	0	00	0	0	0
SP-=2	0	0	0	0	0	0	0	xxxx	0	0	x	0	01	0	0	0
Pop dst	0	0	1	0	0	0	0	1101	1	0	0	1	10	0	0	0
Ldm dst,imm	0	0	1	0	0	0	1	1110	0	0	x	0	00	0	0	0
Ldd dst , src (offset)	1	0	1	0	0	0	1	0101	1	0	1(mem addr alu)	1	00	0	0	0
Std src1,offset src2	1	1	0	0	0	0	1	0101	0	1	1	0	00	0	0	0
Jz dst	1	0	0	0	0	0	0	xxxx	0	0	x	0	00	0	0	0
Jn dst	1	0	0	0	0	0	0	xxxx	0	0	x	0	00	0	0	0
Jc dst	1	0	0	0	0	0	0	xxxx	0	0	x	0	00	0	0	0
Jmp dst	1	0	0	0	0	0	0	xxxx	0	0	x	0	00	0	0	0
Call dst	0	0	0	0	0	0	0	Xxxx	0	1	0	0	00	0	1	0
SP-=2	0	0	0	0	0	0	0	xxxx	0	0	x	0	01	0	0	0
JMP dst	1	0	0	0	0	0	0	xxxx	0	0	x	0	00	0	0	0
ret	0	0	0	0	0	0	0	xxxx	1	0	0	0	10	1	0	1

Pipeline stages design

1. Pipeline Registers Details

2. IF/ID Register:

content	#Of bits
Incremented PC value	32 bits
fetched Instruction	32 bits
Total size	**64 bits**

3. ID/EX Register:

Content	#Of bits
Read data 1	32 bits
Read data 2	32 bits
CCR	3 bits
Offset/imm extended	32 bits
Control signals(EX) - ALU operation (4 bits) - Take immediate (1 bit)	5bits
Control signals (MEM, WB)	11 bits
Rsrc code	3 bits
Rdst code	3 bits
Incremented PC value	32 bits
Total Size	**153 bits**

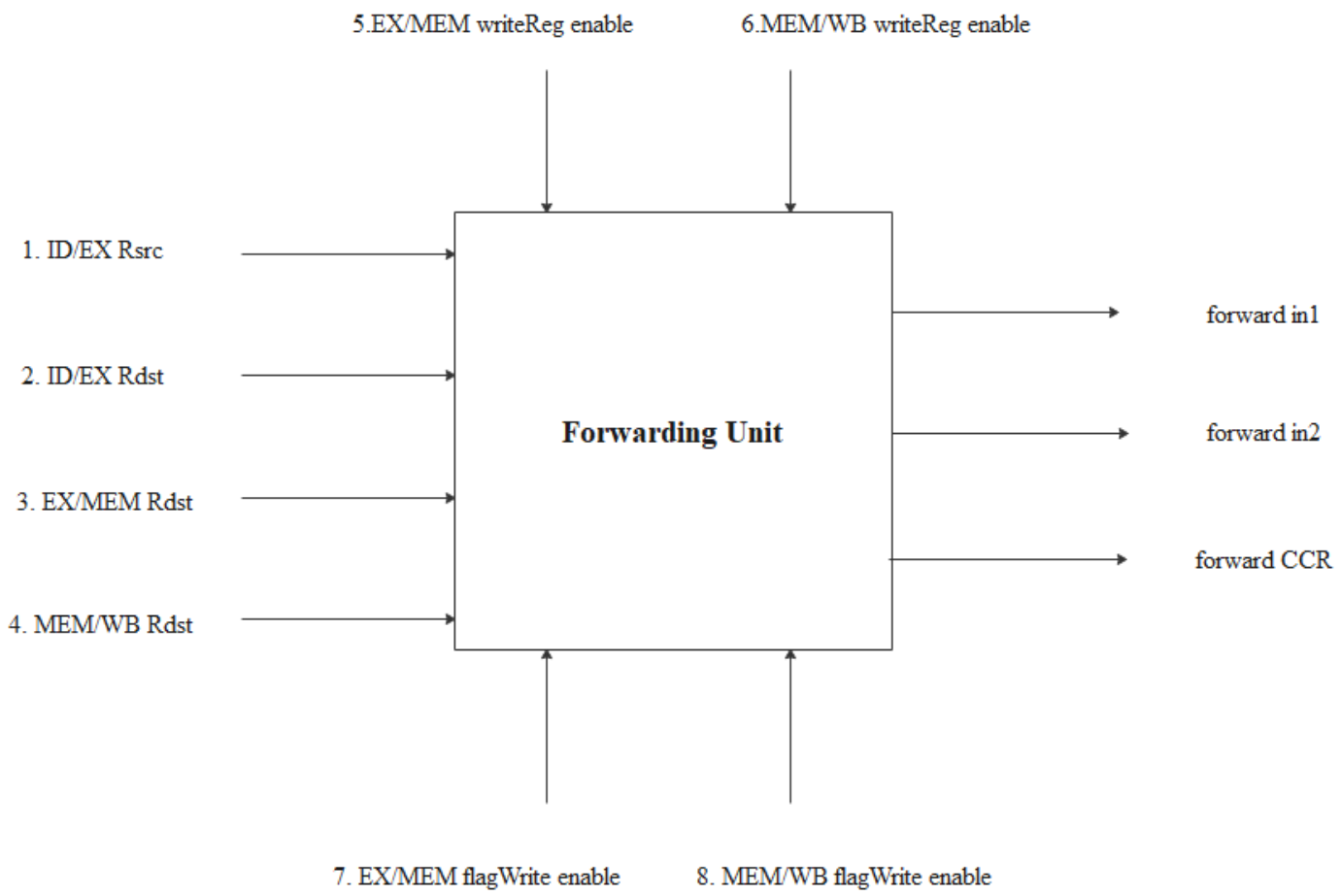
4. EX/MEM register:

Content	#Of bits
result	32 bits
(N,Z,C) from ALU	3 bits
Read data 2	32 bits
Incremented PC value	32 bits
Control signals(MEM) - MEM Write (1 bit) - MEM Read (1 bit) - SP operation (2 bits) - MEM address src (1 bit) - PC to MEM (1 bit) - MEM to PC (1 bit)	7 bits
Control signals (WB)	4 bits
Rdst	3 bits
Total Size	**113 bits**

5. MEM/WB register:

Content	**#Of bits**
result	32 bits
(N, Z, C) from ALU	3 bits
MEM data read	32 bits
Control signals(WB) - MEM to Reg (1 bit) - Write Reg Enable (1 bit) - Write flag Reg enable (1 bit) - Write Out Port enable (1 bit)	4 bits
Rdst	3 bits
Total Size	**74 bits**

2. Forwarding Unit



if 1 == 3 when 5 ==> forward 1 == 01
if 2 == 3 when 5 ==> forward 2 == 01
if 1 == 4 when (6 & !5) ==> forward 1 == 10
if 2 == 4 when (6 & !5) ==> forward 2 == 10
if 7 forward CCR == 01
if (8& !7) forward CCR == 10

3. Hazard Detection Unit