Strategic Cell Placement in EDA: Harnessing the Power of Simulated Annealing

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1. Introduction

This project is aimed at implementing a placement optimization algorithm for electronic design automation (EDA). The primary objective is to optimally place cells on a grid to minimize the Half Perimeter Wire Length (HPWL). This is achieved through a simulated annealing algorithm, a probabilistic technique to approximate the global optimum in a large search space.

The report covers detailed explanations of the project's components, including file parsing, data structure initialization, grid representation, the simulated annealing process, and GIF generation for visualization.

2. Project Overview

Core Components

1. **Data Structures:**
    a. **Cells:** Represent electronic components with a unique ID and their grid coordinates.
    b. **Nets:** Define connections between cells, holding information about connected cells and their spatial bounding box.
2. **Grid Representation:**
    a. A two-dimensional grid where each cell can be placed. The grid dimensions are determined from the input file.
3. **File Parsing:**
    a. Extracts vital information from a netlist file about the number of cells, nets, and grid dimensions, setting the stage for the optimization process.
4. **Placement Strategy:**
    a. Initially, cells are placed randomly on the grid. This placement serves as the starting point for the optimization process.
5. **Optimization Algorithm - Simulated Annealing:**
    a. Employed to iteratively improve the placement. It involves making swaps between cells and evaluating the impact on the overall wiring length (HPWL).
6. **Visualization:**
    a. The CImg library is used for generating images of the grid at different stages, offering a visual representation of the placement optimization process.

Key Functions

1. **Initial Random Placement:**
    a. Cells are initially placed at random positions on the grid.
2. **Swap Mechanism:**
    a. Cells are swapped to explore different configurations, seeking a layout that minimizes the wiring length.
3. **HPWL Calculation:**
    a. The Half Perimeter Wire Length (HPWL) for each net is computed to quantify the wiring length and guide the optimization.
4. **Simulated Annealing:**

    a. A probabilistic technique that intelligently explores the placement space, balancing between exploring new configurations and improving current ones.
5. **Visualization and Output:**
    a. Generation of grid images and a final GIF to visualize the progression of the placement optimization.

3. File Parsing

Overview

The file parsing process reads a netlist file to extract information about cells, nets, and grid dimensions, vital for initializing the grid and data structures.

Pseudocode

Parse Netlist File:

```
parseNetListFile(fileName):
   Open fileName
   Read firstLine
   parseNetListFirstLine(firstLine)
   For each line in file:
       parseNetListNetLine(line)
   Close file
```

Parse the First Line:

```
parseNetListFirstLine(firstLine):
   Split firstLine into components, nets, rows, columns
   Initialize grid with rows and columns
   Initialize cells and nets
```

Parse Net Lines:

```
parseNetListNetLine(line):
   Split line into net components
   Update net and cells with connections
```

Example Explanation

Given a sample netlist file:

```
3322 3012 220 212
```

1. **Line 1 ("3322 3012 220 212"):**
    a. Sets 3 cells, 3 nets, and a 2x2 grid.
    b. Initializes structures for cells, nets, and grid.
2. **Subsequent Lines:**
    a. Line 2 ("220"): Connects cells 0, 1, 2 to the first net.
    b. Line 3 ("212"): Connects cells 2, 0 to the second net.
    c. Line 4 ("212"): Connects cells 1, 2 to the third net.
3. **Error Handling:**
    a. Checks for file opening issues and incorrect line formats.
    b. Exits the program if errors are detected, with an error message.

4. Initial Placement Strategy

Overview

The initial placement of cells on the grid is done randomly. This randomization provides a starting point for the optimization process.

Process

Random Placement Algorithm:

```
placeInitiallyRandom():
   For each cell:
       Generate random coordinates within grid dimensions
       If the chosen position is empty:
           Place cell at these coordinates
           Mark position as occupied
       Else:
           Find another position
```

5. Swap Mechanism

The swap mechanism is a core part of the simulated annealing process, allowing the exploration of different cell configurations on the grid.

Types of Swaps

1. **Swapping Two Cells:**
    a. Cells at different positions are exchanged.
    b. Adjustments are made in the grid to reflect the new positions.
2. **Swapping Cell with Empty Space:**
    a. A cell is moved to an empty position, leaving its former position vacant.
    b. Useful for exploring configurations where cells are more spread out.

Swap Algorithm

```
swapCells(cell1, cell2):
    Save original positions of cell1 and cell2
    Exchange positions of cell1 and cell2
    Update grid to reflect new positions
    Recalculate HPWL for affected nets
```

Importance

- The swap mechanism enables the simulated annealing algorithm to effectively navigate the solution space, moving towards configurations with lower HPWL.
- It balances between making small, local changes and more significant, global rearrangements of the cells.

6. Simulated Annealing Algorithm

Function Explanation

1. **Initial Setup:**
    a. **Initial Temperature:** Set high to allow exploration of the solution space.
    b. **Final Temperature:** Set low to gradually focus on refinement rather than exploration.
    c. **Temperature Reduction:** The cooling rate determines how quickly the temperature decreases.
2. **Temperature's Role:**
    a. High temperatures allow the algorithm to accept worse solutions (increased HPWL) for exploration.
    b. As the temperature decreases, the algorithm becomes more selective, favoring solutions that improve or maintain HPWL.
3. **Iteration Process:**
    a. At each temperature level, a set number of moves (swaps) are tried.
    b. Each move's impact on HPWL is calculated.
4. **Move Acceptance:**
    a. If a move reduces HPWL, it's accepted.

b. If HPWL increases, the move is accepted with a probability depending on the current temperature and the HPWL change. This probability decreases as the temperature drops.

5. **Cooling Down:**
    a. After a set number of moves at a given temperature, the temperature is reduced.
    b. The process continues until the final temperature is reached.

Simulated Annealing Algorithm in Pseudocode

```
simulateAnnealing(initialHPWL, coolingRate):
    Set currentTemperature to a high value
    Set finalTemperature to a low value
    While currentTemperature > finalTemperature:
        For each move in a predefined number of moves:
            Perform a swap
            Calculate new HPWL
            If HPWL is improved:
                Accept the swap
            Else:
                Calculate acceptance probability
                Accept swap based on probability
        Reduce currentTemperature by coolingRate
```

7. Output Analysis of the Simulated Annealing Process

Initial and Final Grid States

- **Initial Grid:** Shows a random placement of cells ('numbered') and empty spaces ('----'), reflecting the starting point of the optimization process.
- **Final Grid:** Demonstrates a more optimized arrangement with cells often clustered and more empty spaces along the edges.

Empty Cells on the Edges

- This pattern arises as the algorithm moves cells closer together to minimize the total wire length, especially for connected cells, leaving the peripheries less occupied.

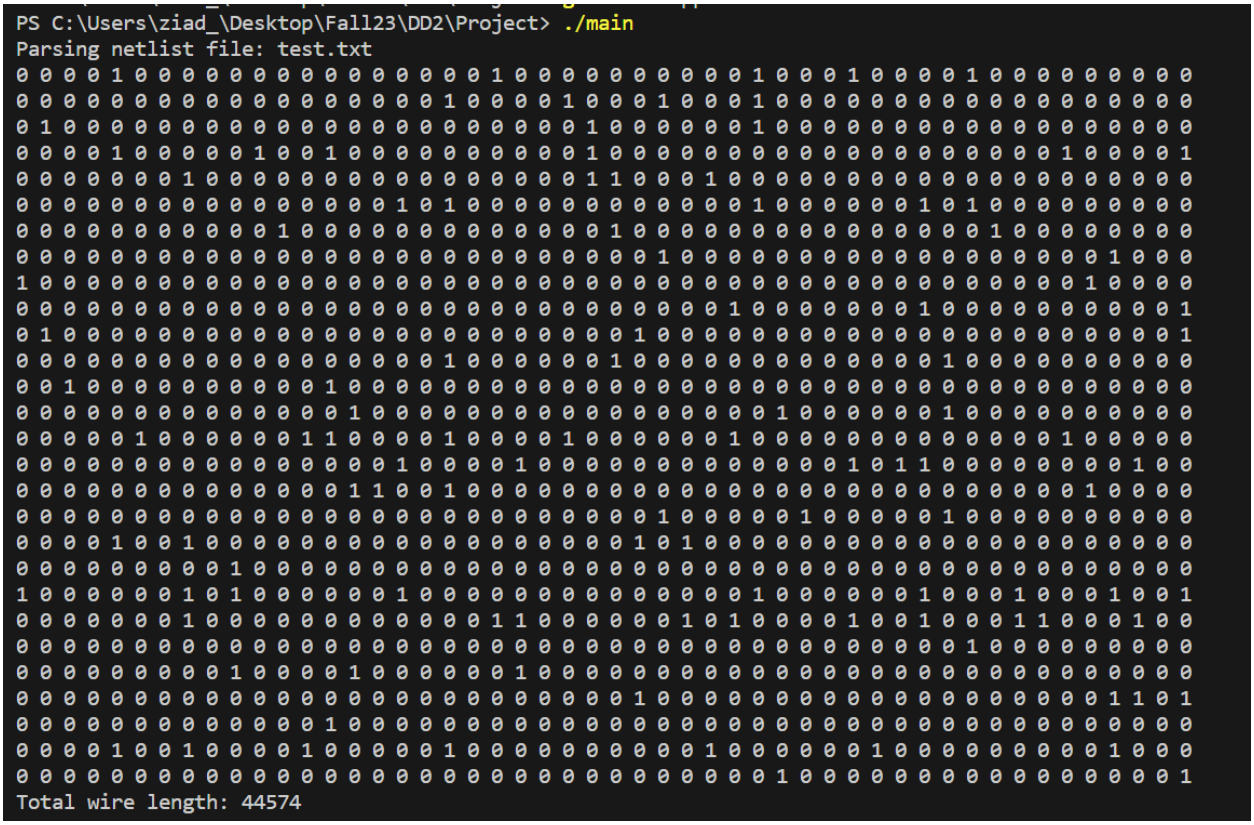
Changes in Wire Length

- The output displays a significant reduction in wire length from the initial to the final state, showcasing the effectiveness of the simulated annealing in optimizing the grid layout for shorter wiring.

Execution Time and `-O3` Flag

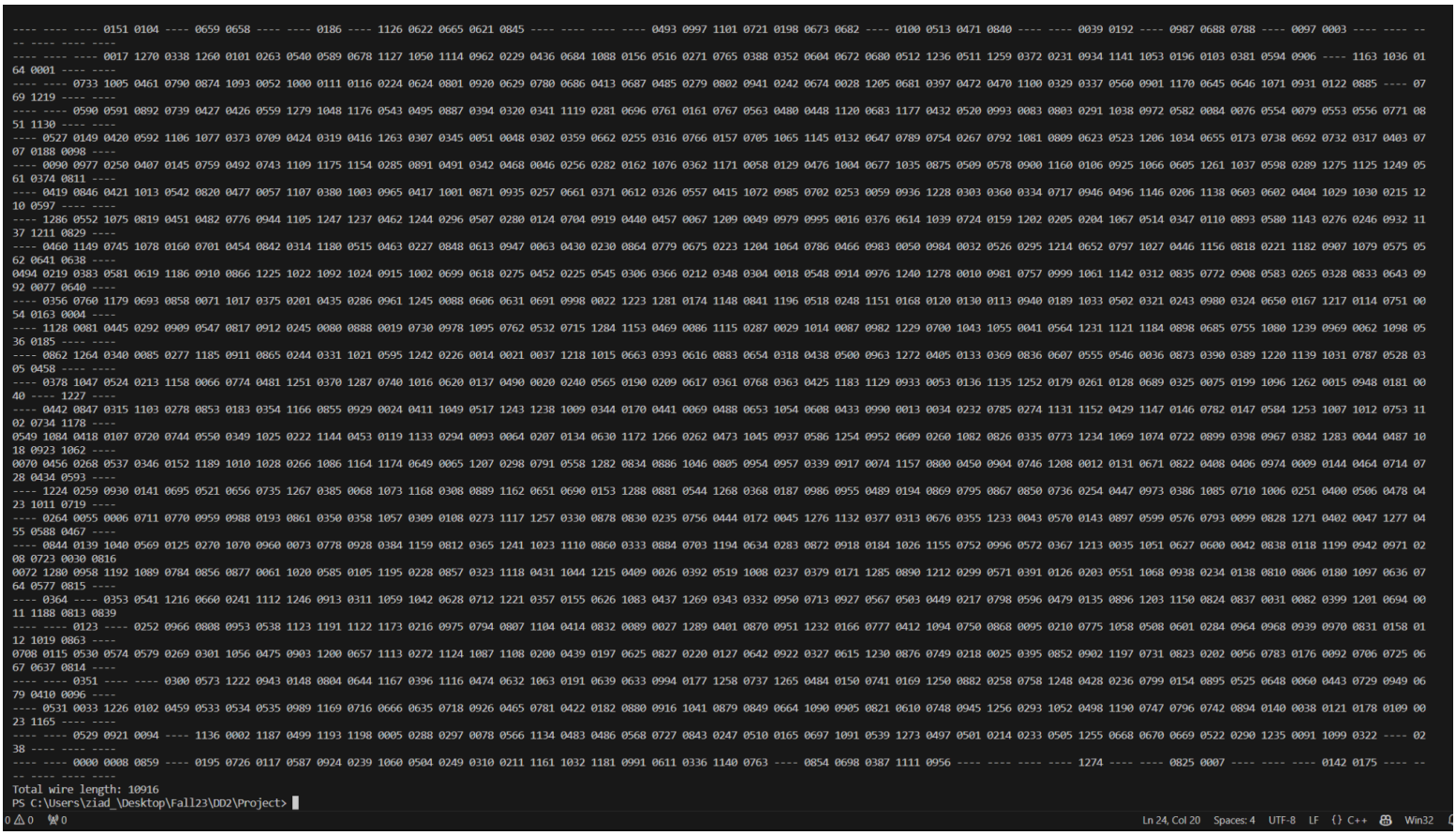
- The 8-second execution time illustrates the efficiency of the algorithm, enhanced by the `-O3` optimization flag in g++, which accelerates computation-intensive tasks in the annealing process.

Output Example



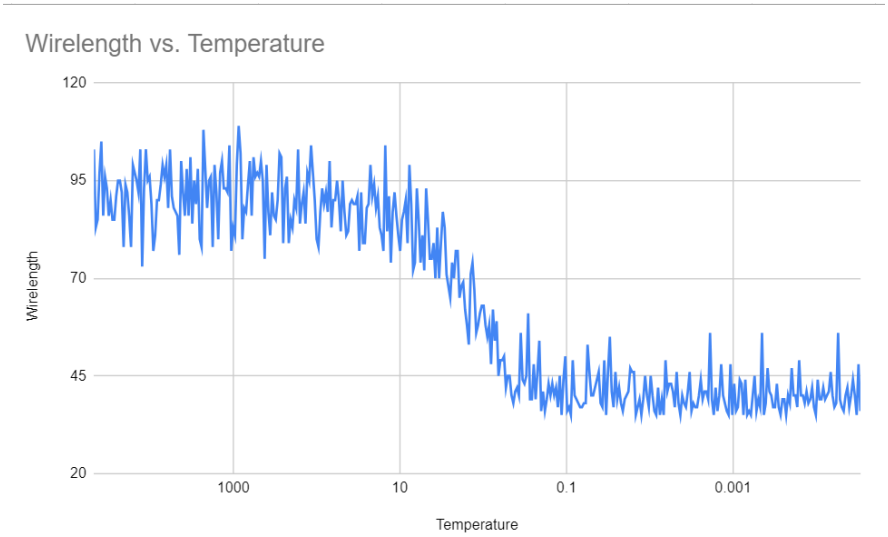
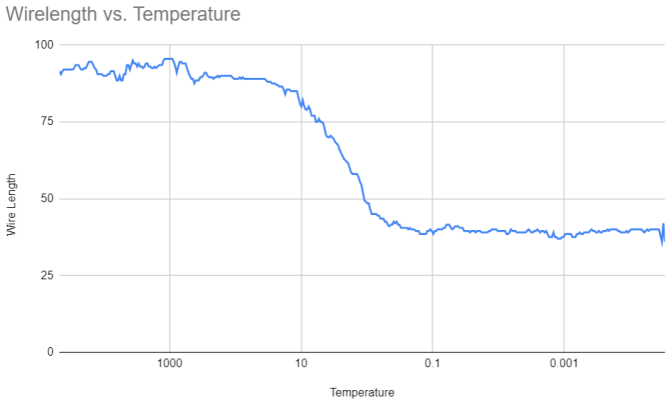
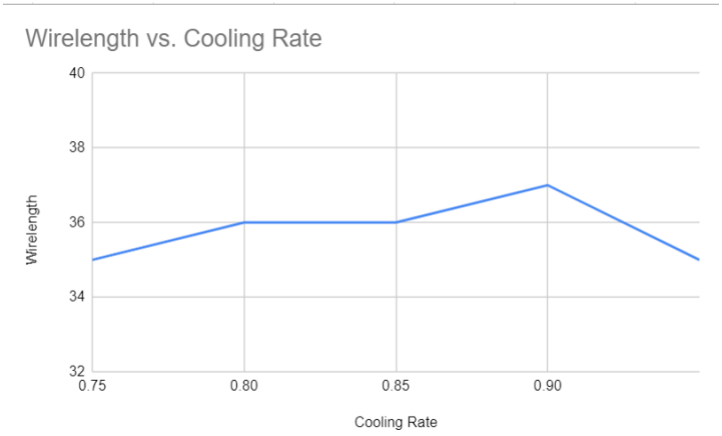
- The following output is the output of simulated annealing on the netlist file t3.

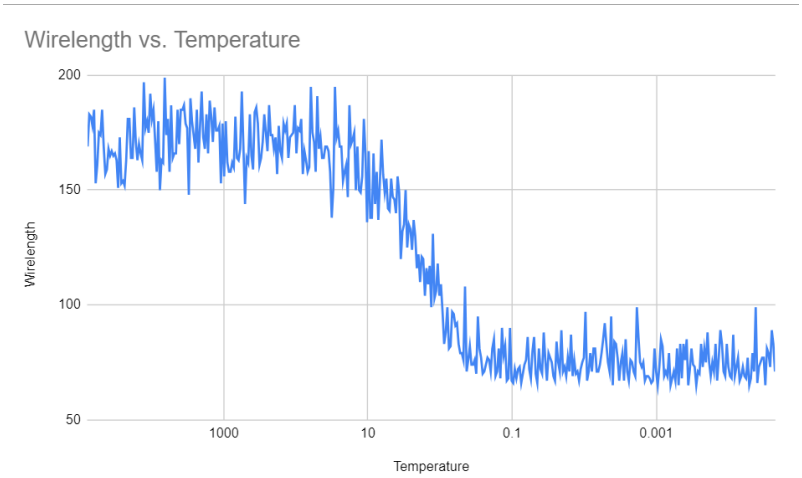
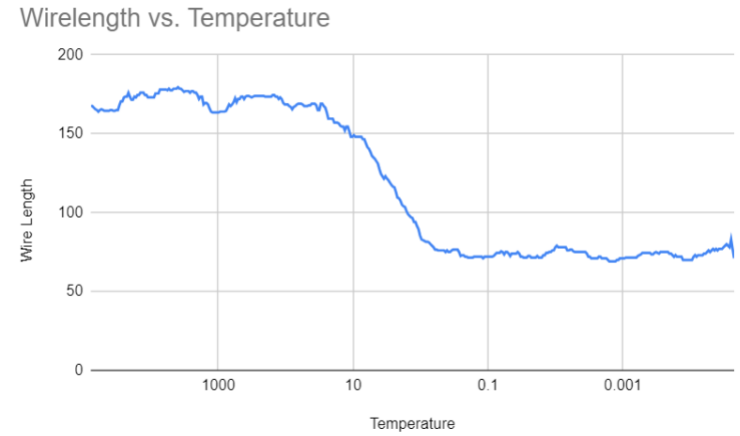
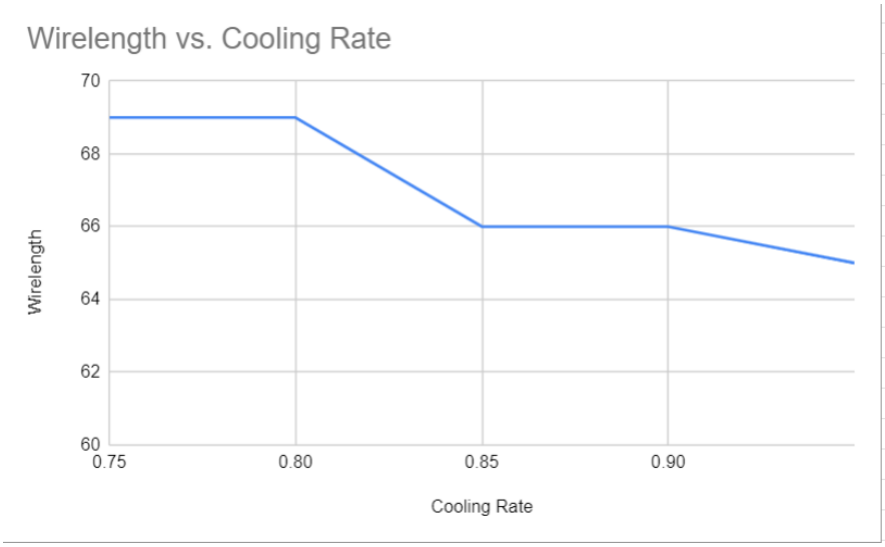
  This is the initial random placement of the grid. 1 represents a cell containing a block and 0 represents an empty cell. The initial total wire length is 44,574

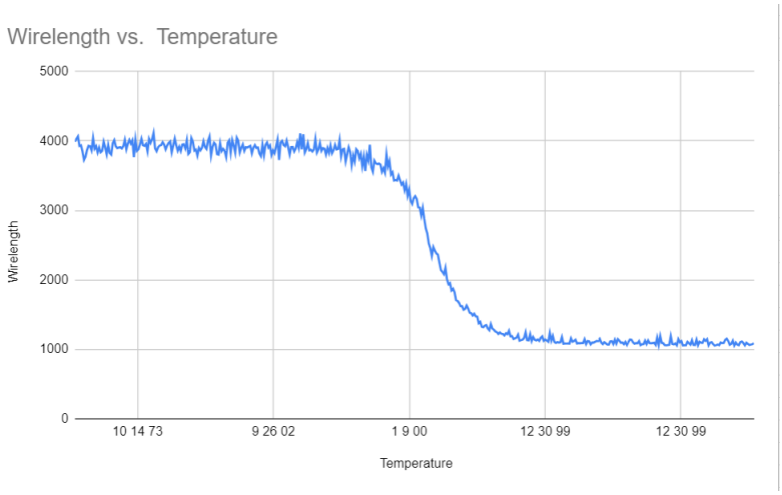
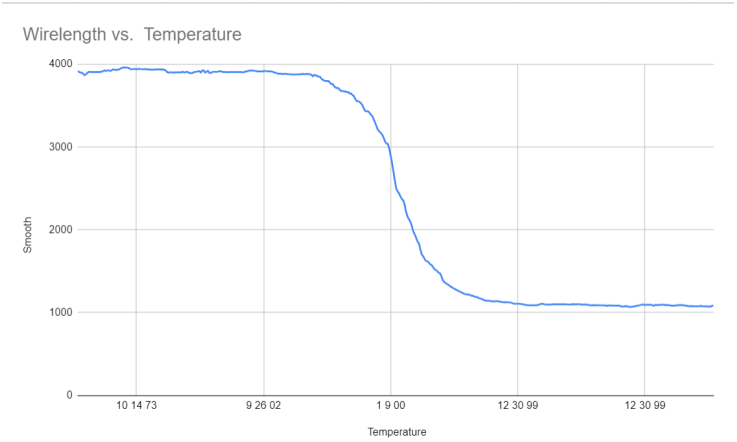
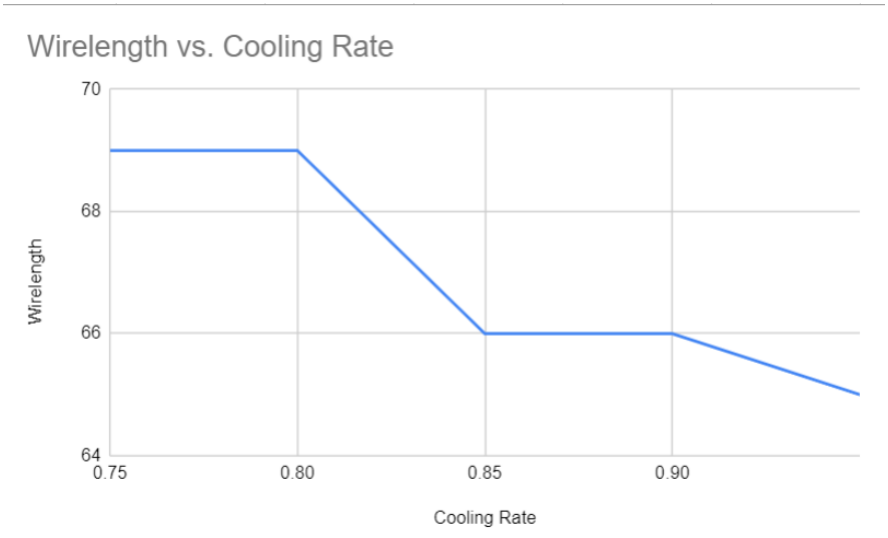


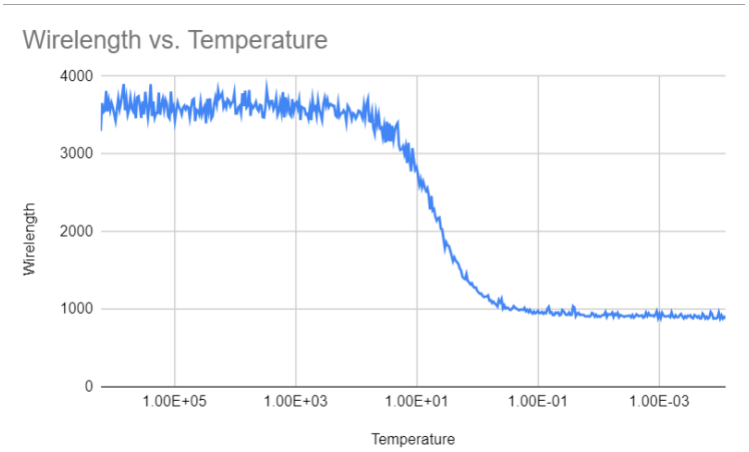
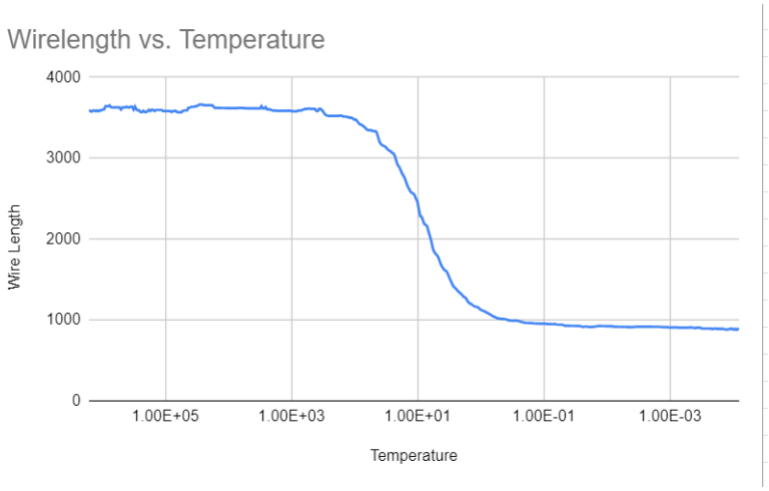
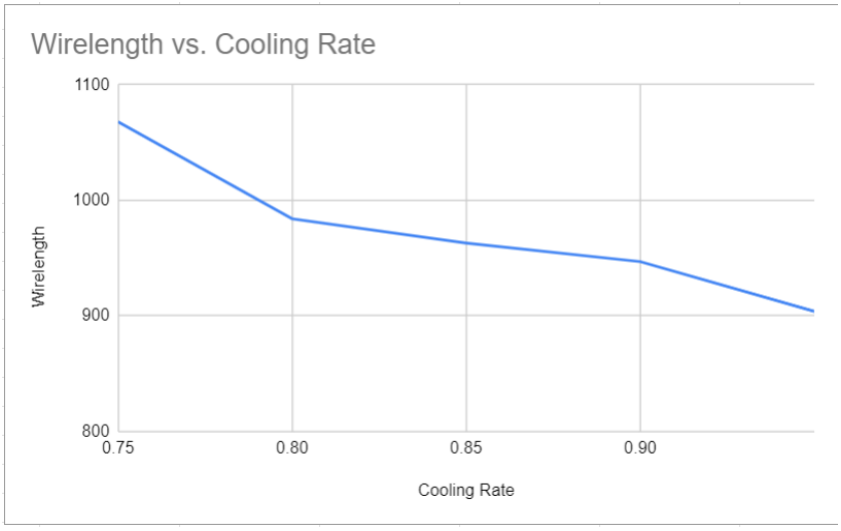
This is the output after running SA. The corners are empty, the wire length is 10,916.

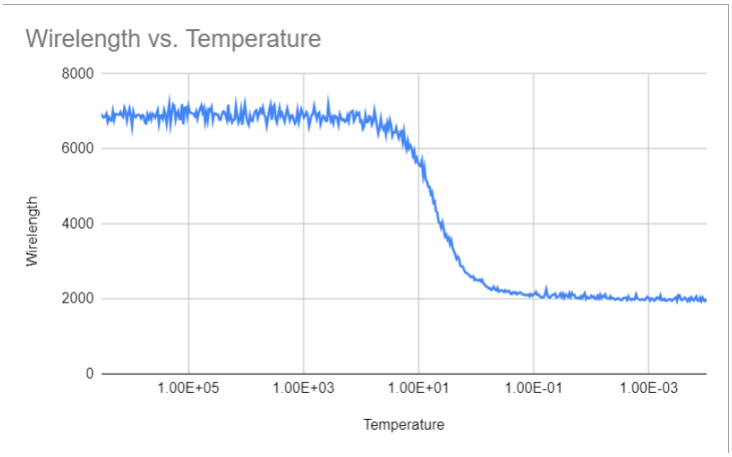
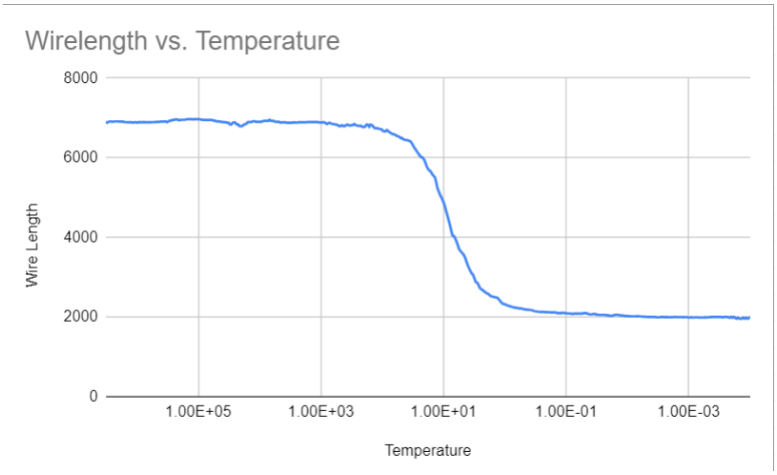
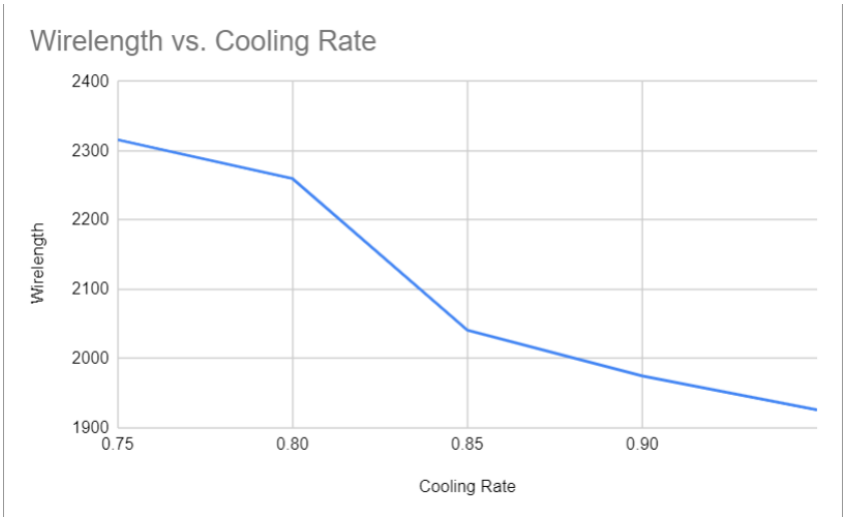
Graphs

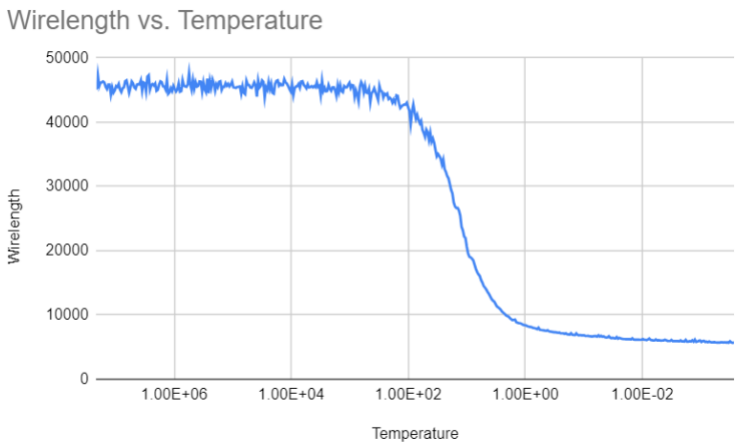
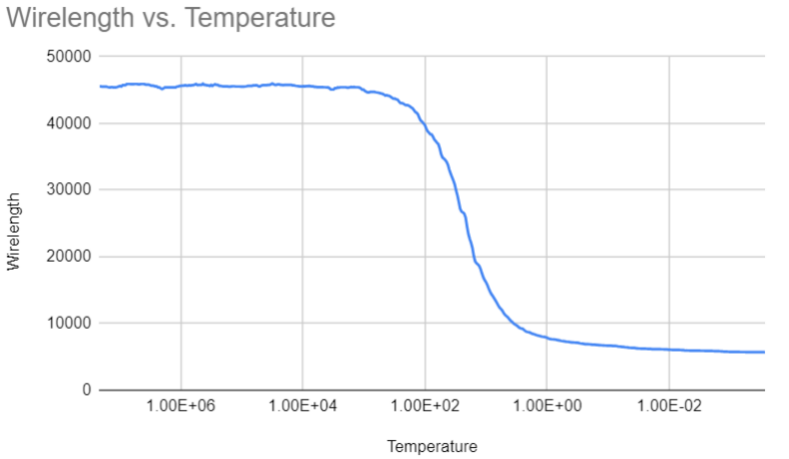
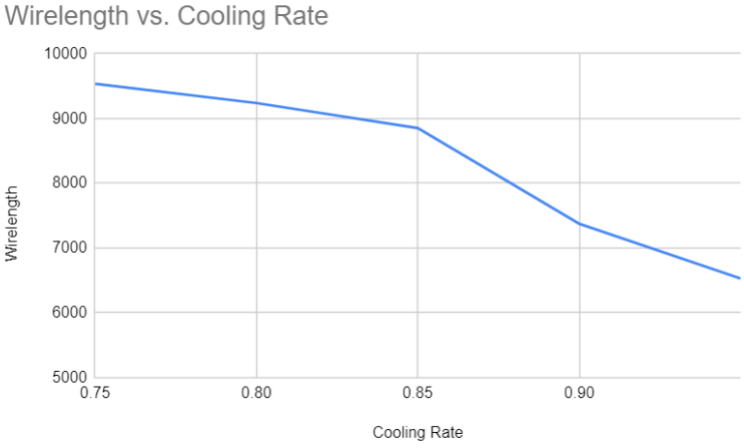
d0	
WL vs Temp	
Smoothed WL vs Temp	
WL vs Cooling Rate	

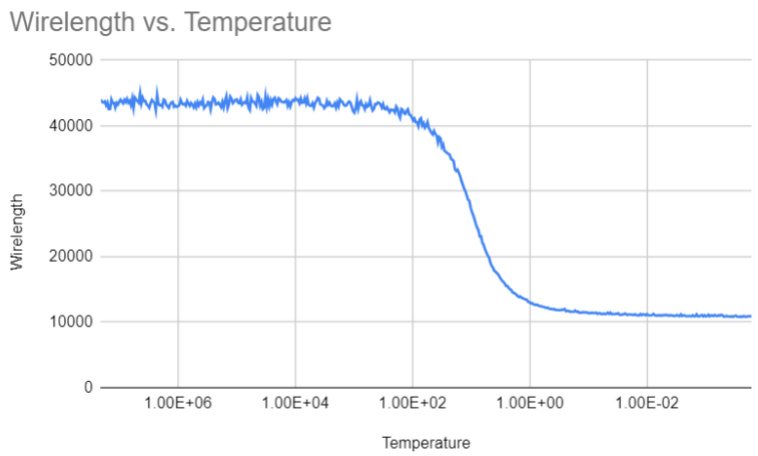
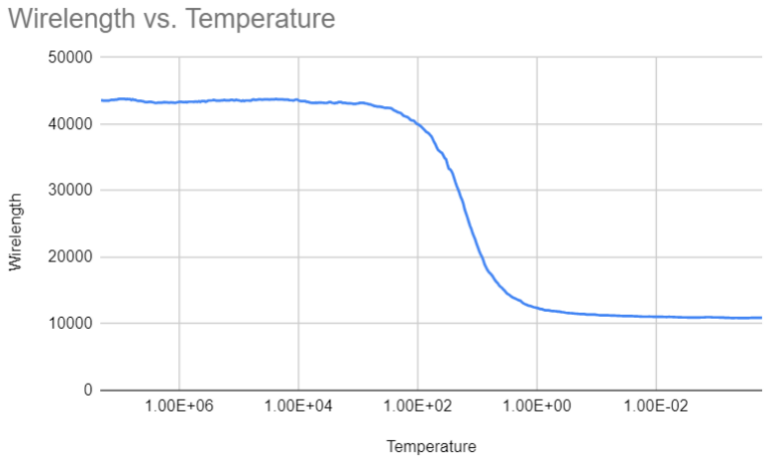
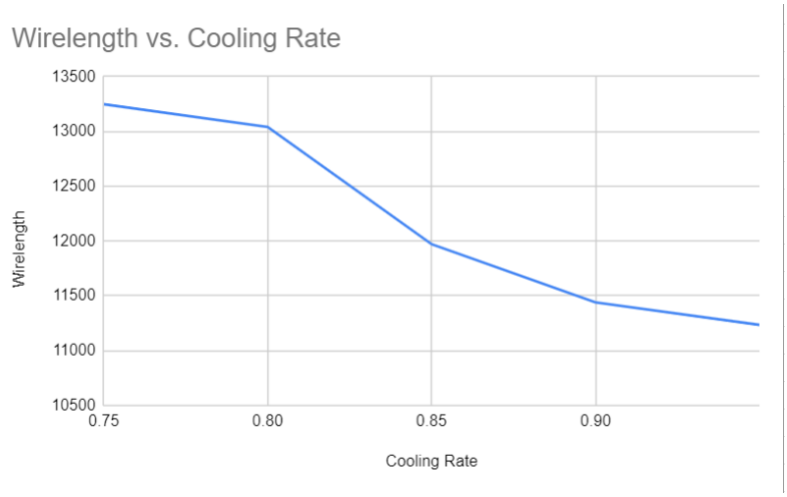
d1	
WL vs Temp	
Smoothed WL vs Temp	
WL vs Cooling Rate	

d2	
WL vs Temp	
Smoothed WL vs Temp	
WL vs Cooling Rate	

d3	
WL vs Temp	
Smoothed WL vs Temp	
WL vs Cooling Rate	

t1	
WL vs Temp	
Smoothed WL vs Temp	
WL vs Cooling Rate	

t2	
WL vs Temp	
Smoothed WL vs Temp	
WL vs Cooling Rate	

t3	
WL vs Temp	
Smoothed WL vs Temp	
WL vs Cooling Rate	

Conclusion

As we can see from the graphs, as the temperature decreases, the wire length decreases. This is expected because each iteration the temperature is multiplied by the cooling rate, and each iteration the wire length is decreased. Moreover, as we increase the cooling rate, the wire length decreases. This is because the temperature converges to the final temperature slower when the cooling rate is higher.