Active-HDL PDF Export
MOHAMED_TAHA_SALAH_192000280 workspace

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Active-HDL Student Edition
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Contents

2 ALU

2.1 FA.vhd

```
--------------------------------------------------------------------------------
--
--
-- Title       : FA
-- Design      : MOHAMED TAHA
-- Author      : Mohamed Khattab
-- Company     : Egyptian Chinese University
--
--------------------------------------------------------------------------------
--
--
-- File        : C:\My_Designs\ALU_MOHAMED_TAHA\MOHAMED TAHA\src\FA.vhd
-- Generated   : Thu Mar  3 17:50:35 2022
-- From        : interface description file
-- By          : Itf2Vhdl ver. 1.22
--
--------------------------------------------------------------------------------
--
--
-- Description :
--
--------------------------------------------------------------------------------
--

--{{ Section below this comment is automatically maintained
--   and may be overwritten
--{entity {FA} architecture {FA}}

library IEEE;
use IEEE.std_logic_1164.all;

entity FA is
     port(
          A : in STD_LOGIC;
          B : in STD_LOGIC;
          CIN : in STD_LOGIC;
          S : out STD_LOGIC;
          COUT : out STD_LOGIC
          );
end FA;

--}} End of automatically maintained section

architecture FA of FA is
begin

    -- enter your statements here --
    S <= A Xor B Xor CIN;
    COUT <= ((A xor B) and CIN) or (A and B);

end FA;
```

2.2 nbitadder.vhd

```
--------------------------------------------------------------------------------
--
-- Title       : \16 bit addsub\
```

```
-- Design      : MOHAMED TAHA
-- Author      : Mohamed Khattab
-- Company     : Egyptian Chinese University
--
-------------------------------------------------------------------------------
--
--
-- File        : C:\My_Designs\ALU_MOHAMED_TAHA\MOHAMED TAHA\src\16 bit addsu
b.vhd
-- Generated   : Sat Mar  5 21:26:07 2022
-- From        : interface description file
-- By          : Itf2Vhdl ver. 1.22
--
-------------------------------------------------------------------------------
--
--
-- Description :
--
-------------------------------------------------------------------------------
--

--{{ Section below this comment is automatically maintained
--   and may be overwritten
--{entity {\16 bit addsub\} architecture {\16 bit addsub\}}

library IEEE;
use IEEE.std_logic_1164.all;

entity \add_sub\ is
    generic(
          n : Integer :=16
    );
     port(
         CIN : in STD_LOGIC;
         A : in STD_LOGIC_VECTOR(n-1 downto 0);
         B : in STD_LOGIC_VECTOR(n-1 downto 0);
         S : out STD_LOGIC_VECTOR(n-1 downto 0);
         COUT : out STD_LOGIC
         );
end \add_sub\;

architecture \Add_sub_model\ of \add_sub\ is
component FA is
     port(
         A : in STD_LOGIC;
         B : in STD_LOGIC;
         CIN : in STD_LOGIC;
         S : out STD_LOGIC;
         COUT : out STD_LOGIC
         );
end component;
signal temp: std_logic_vector(n downto 0);
begin
temp(0) <= CIN;
Loop1 : for i in 0 to n-1 generate
    adder: FA port map (A(i),B(i),temp(i),S(i),temp(i+1));
end generate;
COUT <= temp(n);

end \Add_sub_model\;
```

2.3 PartA.vhd

```
 ----------------------------------------------------------------------------
---
--
-- Title       : PartA
-- Design      : MOHAMED TAHA
-- Author      : Mohamed Khattab
-- Company     : Egyptian Chinese University
--
----------------------------------------------------------------------------
--
--
-- File        : C:\My_Designs\ALU_MOHAMED_TAHA\MOHAMED TAHA\src\PartA.vhd
-- Generated   : Thu Mar  3 18:22:14 2022
-- From        : interface description file
-- By          : Itf2Vhdl ver. 1.22
--
----------------------------------------------------------------------------
--
--
-- Description :
--
----------------------------------------------------------------------------
--

--{{ Section below this comment is automatically maintained
--   and may be overwritten
--{entity {PartA} architecture {PartA}}

library IEEE;
use IEEE.std_logic_1164.all;

entity PartA is
    generic(
     n:Integer :=16
    );
     port(
         CIN : in STD_LOGIC;
         A : in STD_LOGIC_VECTOR(n-1 downto 0);
         B : in STD_LOGIC_VECTOR(n-1 downto 0);
         S : in STD_LOGIC_VECTOR(1 downto 0);
         F : out STD_LOGIC_VECTOR(n-1 downto 0);
          COUT : out std_logic
         );
end PartA;

--}} End of automatically maintained section

architecture \PartA_modle\ of PartA is
component \add_sub\ is
    generic(
          n : Integer :=16
    );
     port(
         CIN : in STD_LOGIC;
         A : in STD_LOGIC_VECTOR(n-1 downto 0);
         B : in STD_LOGIC_VECTOR(n-1 downto 0);
         S : out STD_LOGIC_VECTOR(n-1 downto 0);
         COUT : out STD_LOGIC
         );
end component;
signal t,c,e,o,h,j:std_logic_vector(n-1 downto 0);
```

```
signal p,d,g,i,k:STD_LOGIC;
begin
      e <= not B;
    add1 : \add_sub\ port map(CIN,A,x"0000",t,p);
    add2 : \add_sub\ port map(CIN,A,B,c,d);
    add3 : \add_sub\ port map('1',A,e,o,g);
    add4 : \add_sub\ port map(CIN,o,x"1111",h,i);
    add5 : \add_sub\ port map('0',A,x"1111",j,k);
F <= t when S = "00" else c when S = "01" else h when S ="10" and CIN = '0' e
lse o when S ="10" and CIN = '1' else
j when S = "11" and CIN = '0' else x"0000" when S = "11" and CIN = '1' ;

COUT <= p when S = "00" else d when S = "01" else i when S ="10" and CIN = '0
' else g when S ="10" and CIN = '1' else
k when S = "11" and CIN = '0' else '0' when S = "11" and CIN = '1' ;

end \PartA_modle\;
```

2.4 PartB.vhd

```
--------------------------------------------------------------------------------
--
--
-- Title       : ALU
-- Design      : MOHAMED TAHA
-- Author      : Mohamed Khattab
-- Company     : Egyptian Chinese University
--
--------------------------------------------------------------------------------
--
--
-- File        : c:\My_Designs\ALU_MOHAMED_TAHA\MOHAMED TAHA\src\ALU.vhd
-- Generated   : Mon Feb 28 11:30:28 2022
-- From        : interface description file
-- By          : Itf2Vhdl ver. 1.22
--
--------------------------------------------------------------------------------
--
--
-- Description :
--
--------------------------------------------------------------------------------
--

--{{ Section below this comment is automatically maintained
--   and may be overwritten
--{entity {ALU} architecture {ALU}}

library IEEE;
use IEEE.std_logic_1164.all;

entity PartB is
    generic(
     n:Integer :=16
    );
     port(

          A : in STD_LOGIC_VECTOR(n-1 downto 0);
          B : in STD_LOGIC_VECTOR(n-1 downto 0);
          S : in STD_LOGIC_VECTOR(1 downto 0);
          F : out STD_LOGIC_VECTOR(n-1 downto 0)
```

```
        );
end PartB;

--}} End of automatically maintained section

architecture PartB_model of PartB is
begin

    -- enter your statements here --
F <= (A and B) when S = "00" else
           (A or B) when S = "01" else
           (A xor B) when S = "10" else
           (not A) when S = "11" ;


end PartB_model;
```

2.5 PartC.vhd

```
--------------------------------------------------------------------------------
--
--
-- Title       : PartC
-- Design      : ALU
-- Author      : Mohamed Khattab
-- Company     : Egyptian Chinese University
--
--------------------------------------------------------------------------------
--
--
-- File        : C:\My_Designs\ALU_MOHAMED_TAHA_192000280\ALU\src\PartC.vhd
-- Generated   : Sun Mar  6 18:55:16 2022
-- From        : interface description file
-- By          : Itf2Vhdl ver. 1.22
--
--------------------------------------------------------------------------------
--
--
-- Description :
--
--------------------------------------------------------------------------------
--

--{{ Section below this comment is automatically maintained
--   and may be overwritten
--{entity {PartC} architecture {PartC}}

library IEEE;
use IEEE.std_logic_1164.all;

entity PartC is
    generic(
     n:Integer :=16
    );
     port(
         A : in STD_LOGIC_VECTOR(n-1 downto 0);
         CIN :in Std_logic;
         S : in STD_LOGIC_VECTOR(1 downto 0);
         F : out STD_LOGIC_VECTOR(n-1 downto 0)
         );
end PartC;
```

```
--}} End of automatically maintained section

architecture PartC of PartC is
begin

F <= '0' & A(n-1 downto 1) when S ="00" else
    A(0) & A(n-1 downto 1) when S ="01" else
     CIN & A(n-1 downto 1) when S ="10" else
   A(n-1) & A(n-1 downto 1) when S="11";

end PartC;
```

2.6 PartD.vhd

```
----------------------------------------------------------------------------
--
--
-- Title       : PartD
-- Design      : ALU
-- Author      : Mohamed Khattab
-- Company     : Egyptian Chinese University
--
----------------------------------------------------------------------------
--
--
-- File        : C:\My_Designs\ALU_MOHAMED_TAHA_192000280\ALU\src\PartD.vhd
-- Generated   : Sun Mar  6 20:52:22 2022
-- From        : interface description file
-- By          : Itf2Vhdl ver. 1.22
--
----------------------------------------------------------------------------
--
--
-- Description :
--
----------------------------------------------------------------------------
--

--{{ Section below this comment is automatically maintained
--   and may be overwritten
--{entity {PartD} architecture {PartD}}

library IEEE;
use IEEE.std_logic_1164.all;

entity PartD is
    generic(
     n:Integer :=16
    );
     port(
         CIN : in STD_LOGIC;
         A : in STD_LOGIC_VECTOR(n-1 downto 0);
         S : in STD_LOGIC_VECTOR(1 downto 0);
         F : out STD_LOGIC_VECTOR(n-1 downto 0)
         );
end PartD;

--}} End of automatically maintained section

architecture PartD of PartD is
begin
```

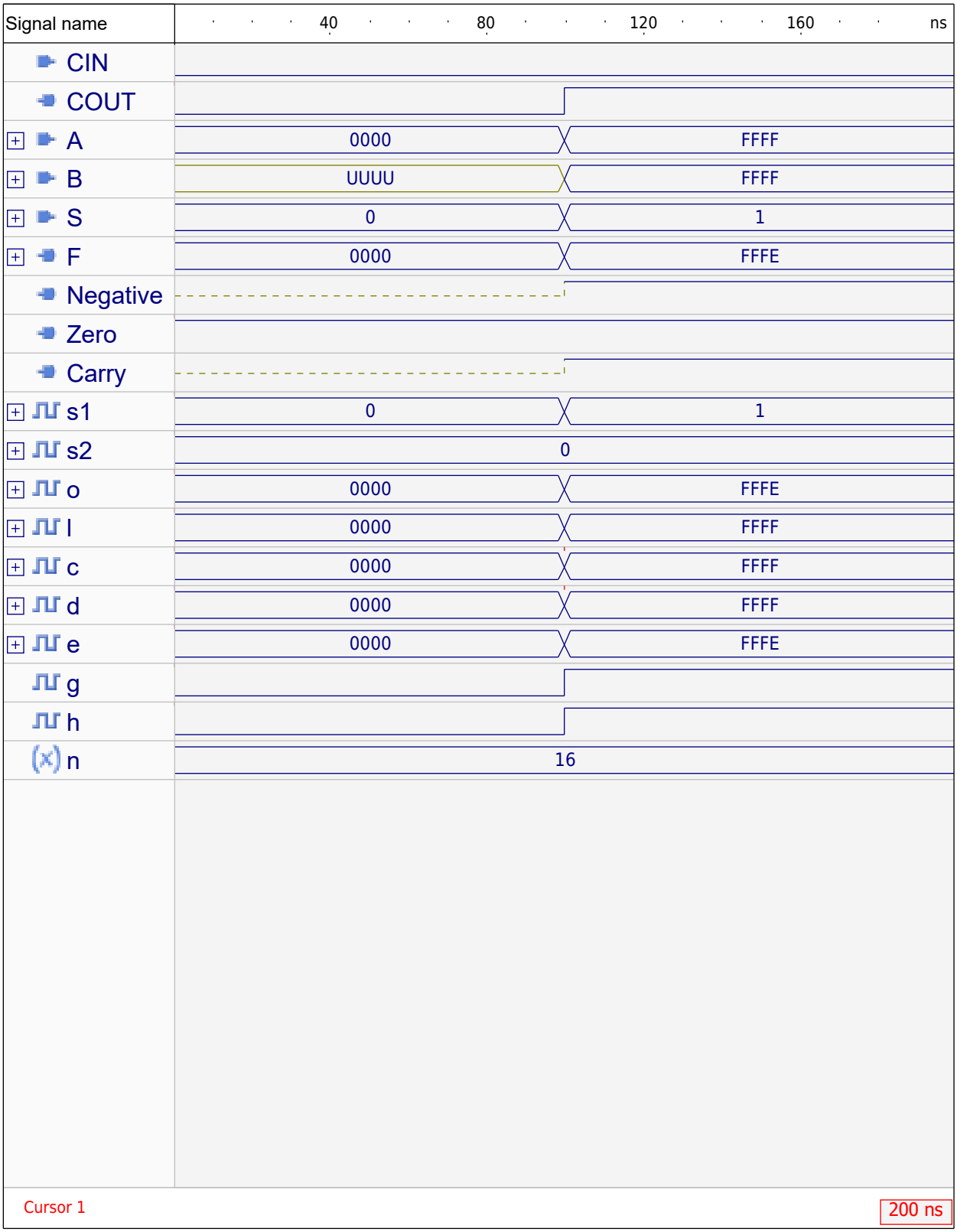
```
     F <= A(14 downto 0) & '0' when S ="00" else
          A(14 downto 0) & A(n-1) when S ="01" else
          A(14 downto 0) & CIN when S ="10" else
          x"0000" when S ="11" ;


end PartD;
```

2.7 ALU.vhd

```
----------------------------------------------------------------------------
--
--
-- Title       : ALU
-- Design      : ALU
-- Author      : Mohamed Khattab
-- Company     : The Egyptian Chinese University
--
----------------------------------------------------------------------------
--
--
-- File        : C:\My_Designs\MOHAMED_TAHA_SALAH_192000280\ALU\src\ALU.vhd
-- Generated   : Mon Mar 14 11:55:49 2022
-- From        : interface description file
-- By          : Itf2Vhdl ver. 1.22
--
----------------------------------------------------------------------------
--
--
-- Description :
--
----------------------------------------------------------------------------
--

--{{ Section below this comment is automatically maintained
--   and may be overwritten
--{entity {ALU} architecture {ALU}}

library IEEE;
use IEEE.std_logic_1164.all;

entity ALU is
    generic(
     n:Integer :=16
    );
     port(
          CIN : in STD_LOGIC;
          COUT : out STD_LOGIC;
          A : in STD_LOGIC_VECTOR(n-1 downto 0);
          B : in STD_LOGIC_VECTOR(n-1 downto 0);
          S : in STD_LOGIC_VECTOR(3 downto 0);
          F : out STD_LOGIC_VECTOR(n-1 downto 0);
          Negative : out std_logic;
          Zero : out std_logic;
          Carry : out std_logic
          );
end ALU;

--}} End of automatically maintained section

architecture ALU of ALU is
```

```
component PartA is
    generic(
     n:Integer :=16
    );
     port(
         CIN : in STD_LOGIC;
         A : in STD_LOGIC_VECTOR(n-1 downto 0);
         B : in STD_LOGIC_VECTOR(n-1 downto 0);
         S : in STD_LOGIC_VECTOR(1 downto 0);
         F : out STD_LOGIC_VECTOR(n-1 downto 0);
          COUT : out std_logic
         );
end component;
component PartB is
    generic(
     n:Integer :=16
    );
     port(

         A : in STD_LOGIC_VECTOR(n-1 downto 0);
         B : in STD_LOGIC_VECTOR(n-1 downto 0);
         S : in STD_LOGIC_VECTOR(1 downto 0);
         F : out STD_LOGIC_VECTOR(n-1 downto 0)
         );
end component;
component PartC is
    generic(
     n:Integer :=16
    );
     port(
         A : in STD_LOGIC_VECTOR(n-1 downto 0);
         CIN :in std_logic;
         S : in STD_LOGIC_VECTOR(1 downto 0);
         F : out STD_LOGIC_VECTOR(n-1 downto 0)
         );
end component;
component PartD is
    generic(
     n:Integer :=16
    );
     port(
         CIN : in STD_LOGIC;
         A : in STD_LOGIC_VECTOR(n-1 downto 0);
         S : in STD_LOGIC_VECTOR(1 downto 0);
         F : out STD_LOGIC_VECTOR(n-1 downto 0)
         );
end component;
signal s1 ,s2 : std_logic_vector(1 downto 0);
signal o,l,c,d,e : std_logic_vector(n-1 downto 0);
signal g,h : std_logic;
begin
s1 <= S(1 downto 0);
s2 <= S(3 downto 2);

ParA : PartA port map (CIN,A,B,s1,o,g);
ParB : PartB port map (A,B,s1,l);
ParC : PartC port map (A,CIN,s1,c);
ParD : PartD port map (CIN,A,s1,d);
e <= o when s2 ="00" else l when s2 ="01" else c when s2 ="10" else d when s2
 ="11";
h <= g when s2 ="00";
Negative <= '1' when e(n-1) ='1';
Zero <= '1' when e = x"0000";
```

```
Carry <= '1' when h ='1';
F <= e ;
COUT <= h;
end ALU;
```


Signal name
40
80
120
160
ns
CIN
COUT
A
0000
FFFF
B
UUUU
FFFF
S
0
1
F
0000
FFFE
Negative
Zero
Carry
s1
0
1
s2
0
o
0000
FFFE
I
0000
FFFF
c
0000
FFFF
d
0000
FFFF
e
0000
FFFE
g
h
n
16
Cursor 1
200 ns