



FPGA FLOW ASSIGNMENT

Mohamed Haysam Afify



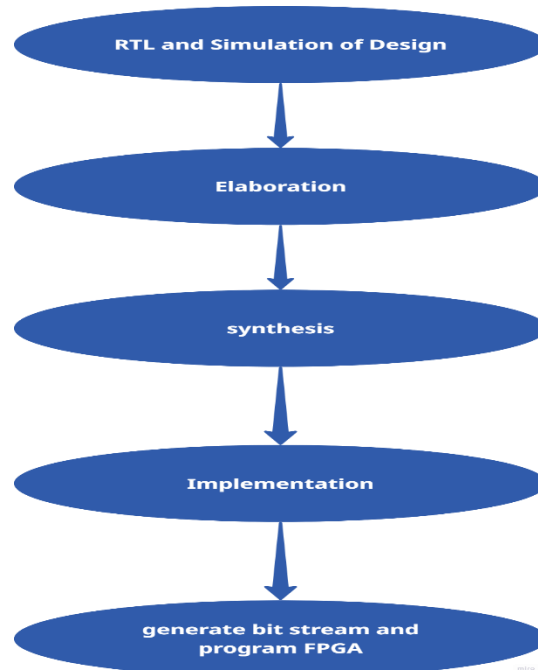
Objective :

Implement a 3-bit counter driven by a 1 Hz clock signal. The clock originates from the internal oscillator, passes through a PLL that outputs an 8 MHz signal, and is then divided down to 1 Hz using a clock divider.

FPGA Type:

We will choose xc7z020clg484-2 speed grade (moderate).

steps to follow:



1-RTL and simulation

1. Verilog code for 3bit counter
2. Add a PLL IP with 8MHZ frequency

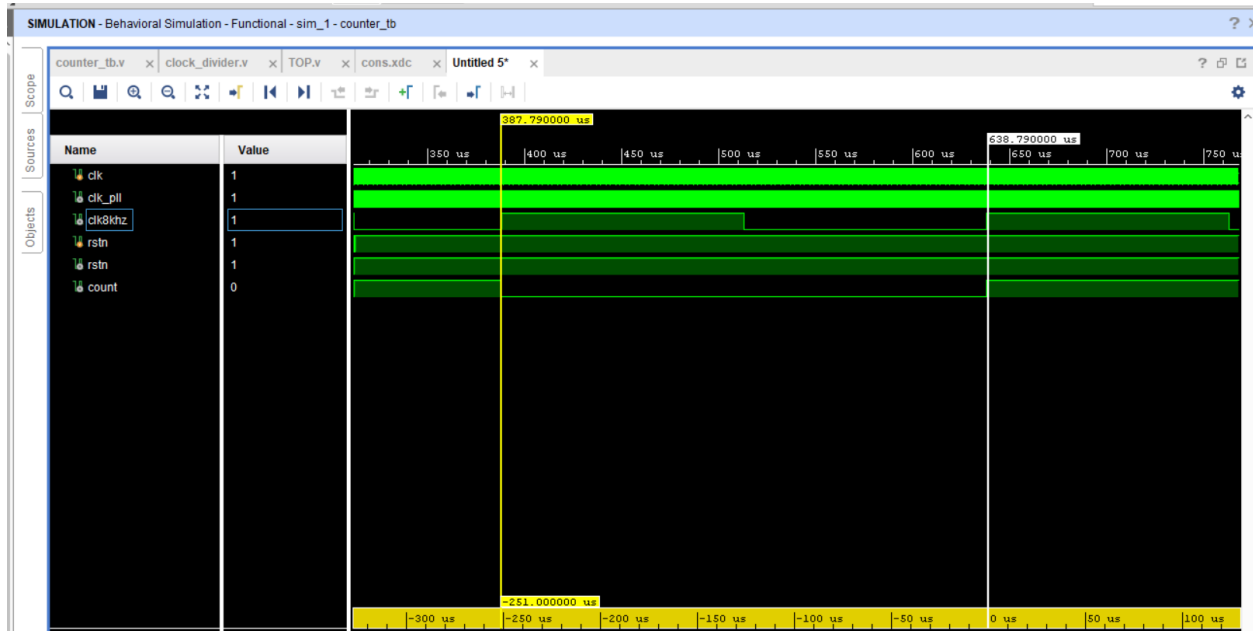
The screenshot shows the Vivado IP configuration window for a component named `clk_wiz_0`. The "Output Clocks" tab is selected, showing a table of output clock configurations. The table has columns for Output Clock, Port Name, Output Freq (MHz) Requested, Actual, Phase (degrees) Requested, Actual, and Duty Cycle Requested. The first row, `clk_out1`, is checked and shows a requested frequency of 8 MHz and an actual frequency of 8.000 MHz. The other rows are unchecked and show a requested frequency of 100.000 MHz and an actual frequency of N/A. The "USE CLOCK SEQUENCING" checkbox is unchecked. The "Clocking Feedback" section is empty.

Output Clock	Port Name	Output Freq (MHz) Requested	Actual	Phase (degrees) Requested	Actual	Duty Cycle Requested
<input checked="" type="checkbox"/> clk_out1	clk_out1	8	8.000	0.000	0.000	50.000
<input type="checkbox"/> clk_out2	clk_out2	100.000	N/A	0.000	N/A	50.000
<input type="checkbox"/> clk_out3	clk_out3	100.000	N/A	0.000	N/A	50.000
<input type="checkbox"/> clk_out4	clk_out4	100.000	N/A	0.000	N/A	50.000
<input type="checkbox"/> clk_out5	clk_out5	100.000	N/A	0.000	N/A	50.000
<input type="checkbox"/> clk_out6	clk_out6	100.000	N/A	0.000	N/A	50.000

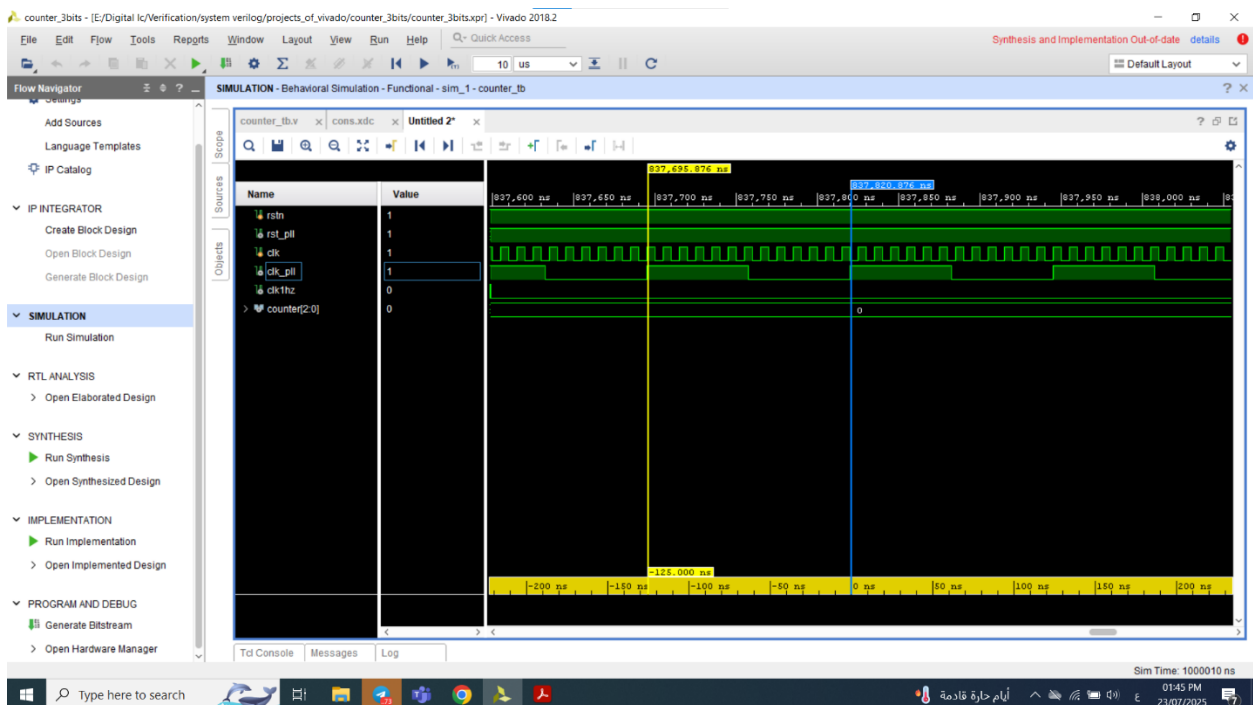
3. Verilog code for TOP and Testbench

simulation :

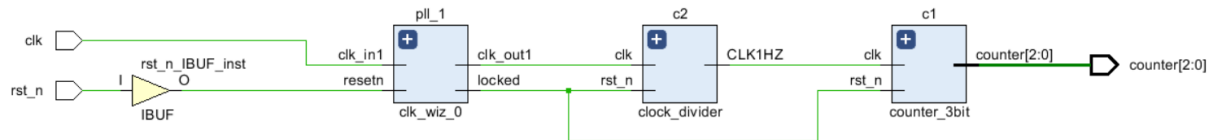
convert freq from 8MHZ to 4kHz to test functionality of divider



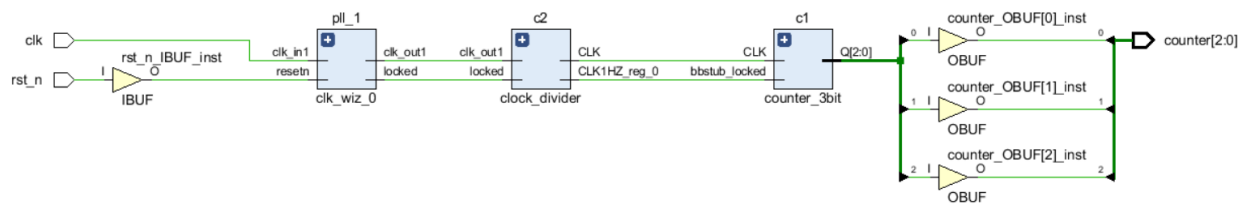
Simulation with 1HZ clk



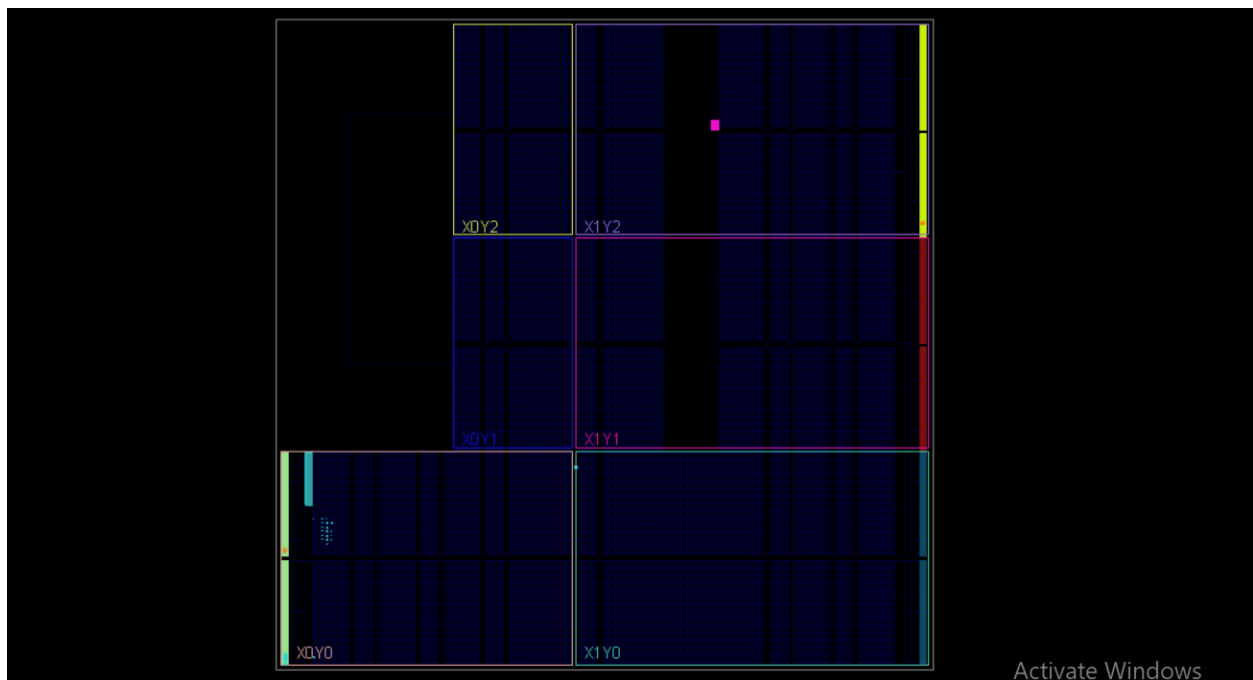
2-Elaborated design



3-Synthesis



4-Implementation



5-bitstream and program FPGA

