FPGA FLOW ASSIGNMENT

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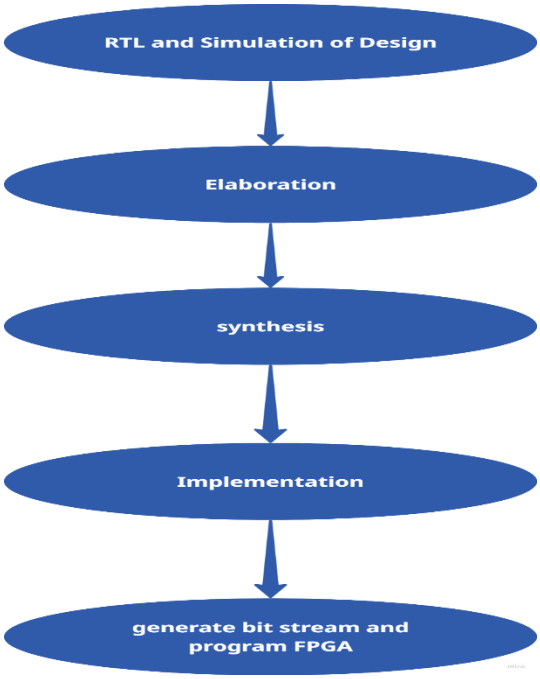
Objective :

Implement a 3-bit counter driven by a 1 Hz clock signal. The clock originates from the internal oscillator, passes through a PLL that outputs an 8 MHz signal, and is then divided down to 1 Hz using a clock divider.

FPGA Type:

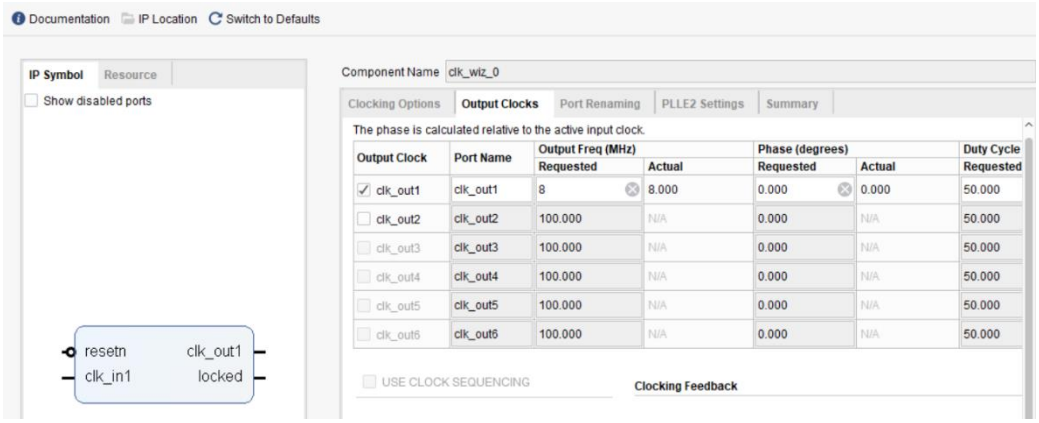
We will choose xc7z020clg484-2 speed grade (moderate).

steps to follow:



1-RTL and simulation

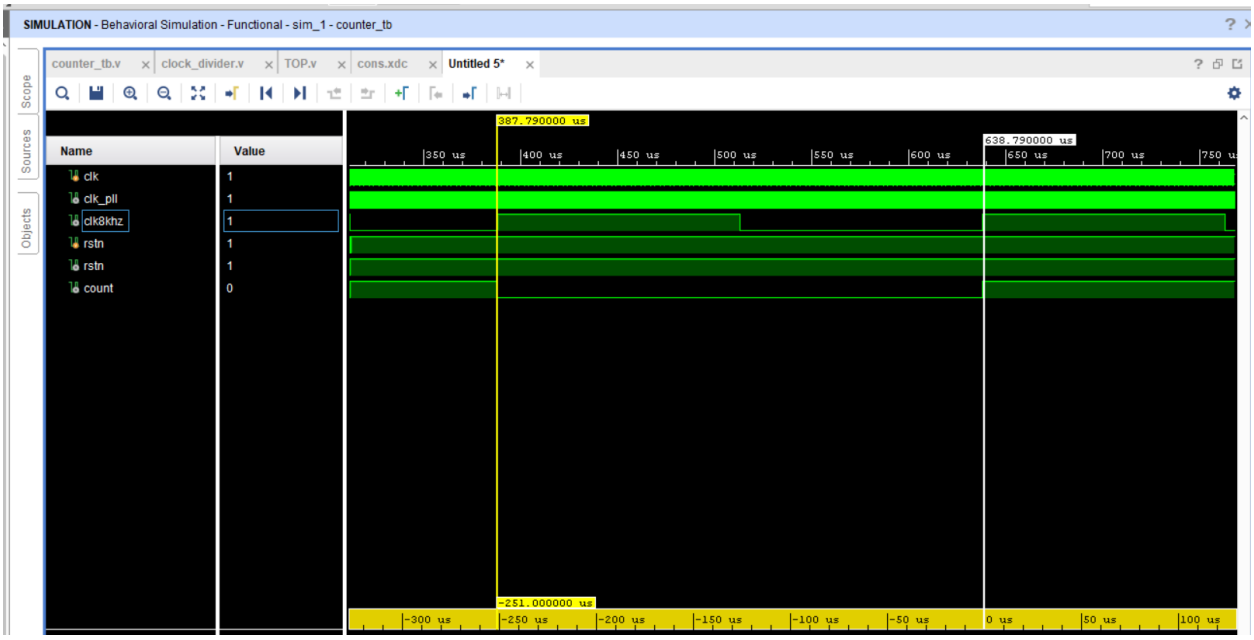
1. Verilog code for 3bit counter
2. Add a PLL IP with 8MHZ frequency



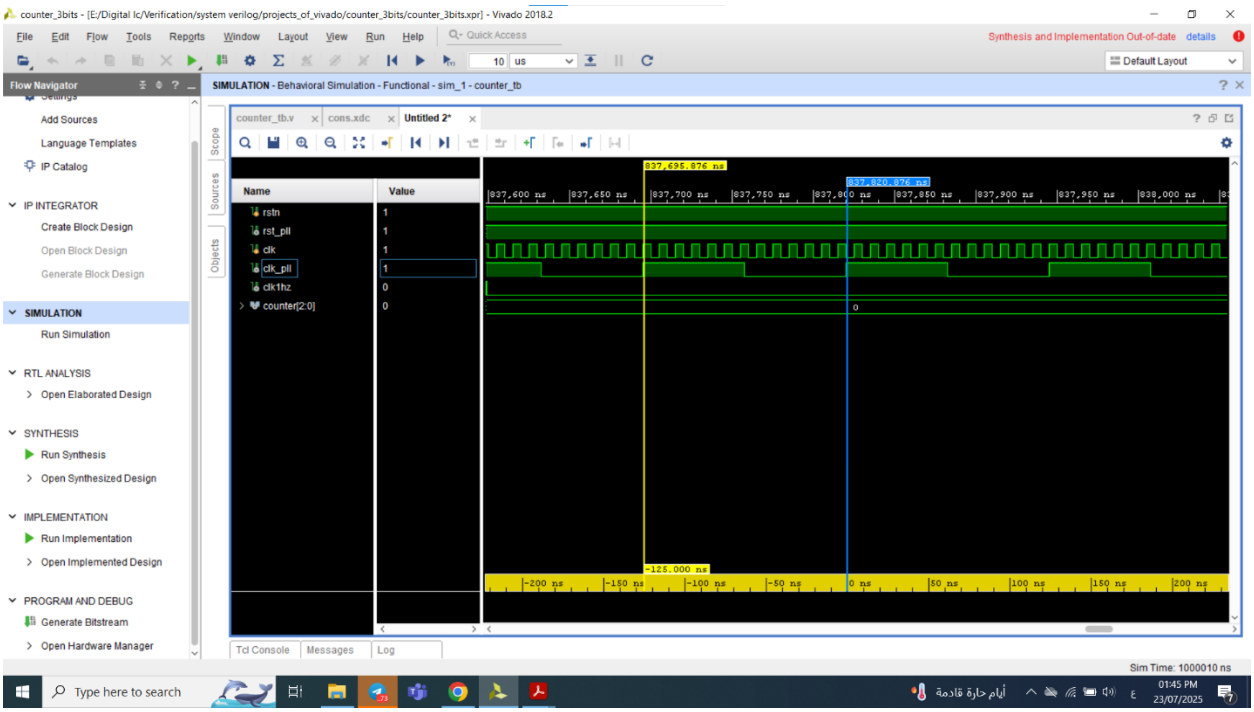
3. Verilog code for TOP and Testbench

simuation :

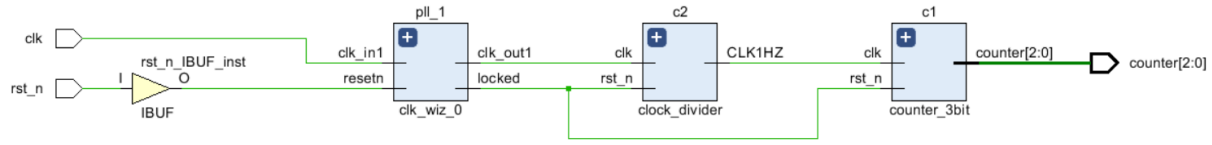
convert freq from 8MHZ to 4kHZ to test functionality of divider



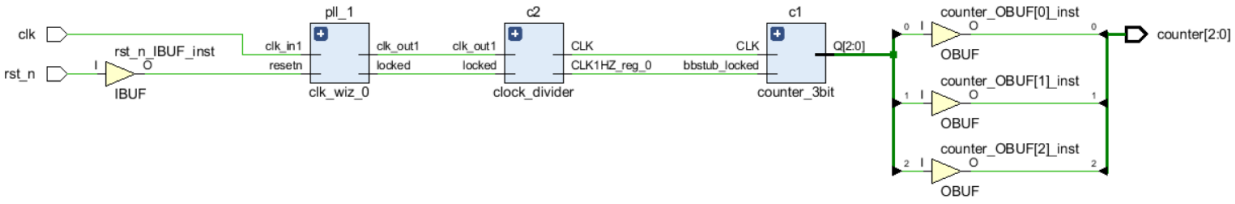
Simulation with 1HZ clk



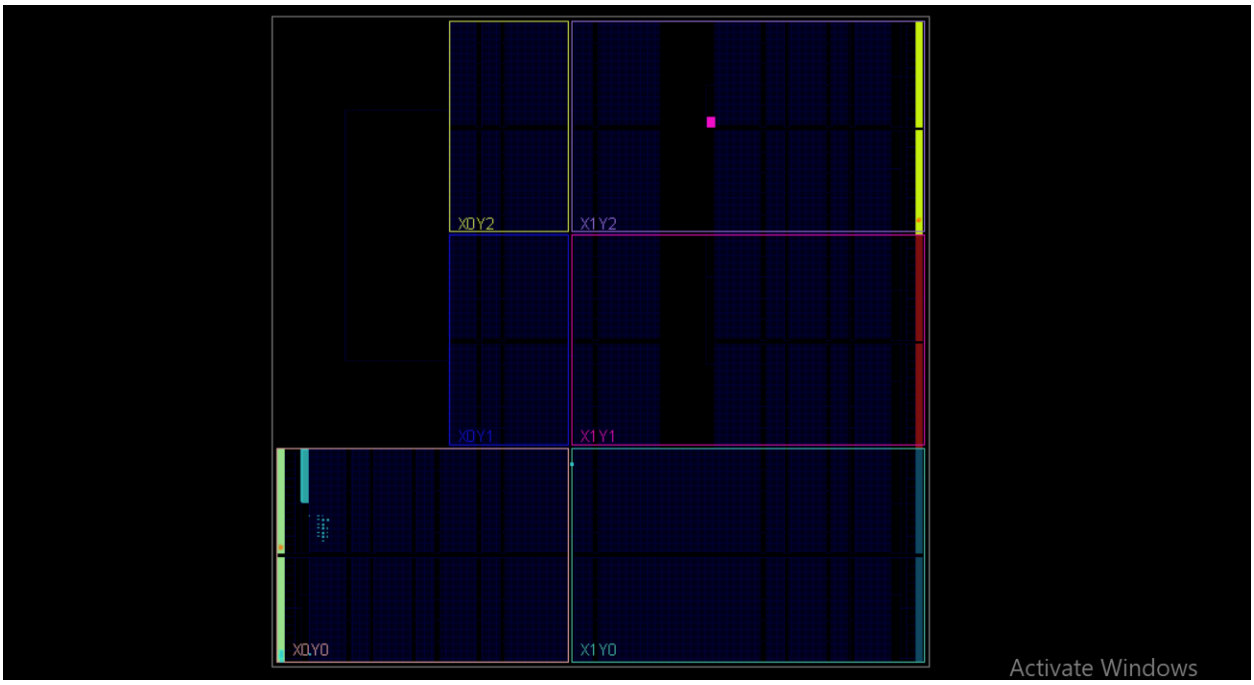
2-Elborated design



3-Synthesis



4-Implementation



5-bitstream and program FPGA