



Final Project Internship

PnR Flow Digital Tx System

Prepared by:

Mohamed Moataz Sallam

Username: asicint25momoataz

Supervised by:

Eng. Bassant Samir

August 22, 2025

Contents

	Page Page
1 PnR Flow Using Compile for Timing	5
1.1 Compiling	5
1.2 Setup Data	8
1.3 Floor Plan	8
1.4 Power Plan	9
1.5 Placement	10
1.6 CTS	12
1.7 Routing	13
1.8 Chip Finishing	14
1.9 StarRC and Prime Time	16
1.10 Note	20
2 PnR Flow Using Compile for Area	21
2.1 Compiling	21
2.2 Setup Data	23
2.3 Floor Plan	24
2.4 Power Plan	24
2.5 Placement	25
2.6 CTS	27
2.7 Routing	28
2.8 Chip Finishing	29
2.9 StarRC and Prime Time	30
2.10 Note	36
3 PnR Flow Using Compile for Power	37
3.1 Compiling	37
3.2 Setup Data	39
3.3 Floor Plan	40
3.4 Power Plan	40
3.5 Placement	41
3.6 CTS	44
3.7 Routing	45
3.8 Chip Finishing	46
3.9 StarRC and Prime Time	47
3.10 Note	52

List of Figures

1.1	compile for timing	5
1.2	path slacks	5
1.3	schematic of design	6
1.4	Number of setup and hold violation in qor report	6
1.5	size cells to reduce the cell delay	6
1.6	After applying size cells affect in qor report	6
1.7	Modification of the error in constraint	7
1.8	Total area and design rule in qor report	7
1.9	Modification of common.tcl to start PnR for timing trial	8
1.10	Data setup of timing trial ndm	8
1.11	Floor planning in timing trail	9
1.12	power planning for timing trail	9
1.13	Modification of power planning script as spacificed in floor plan	9
1.14	placement stage	10
1.15	cell density of timing trail	10
1.16	pin density of timing trail	11
1.17	Report global timing after placment	11
1.18	CTS highlights clock tree	12
1.19	Report global timing after CTS	12
1.20	Routing stage	13
1.21	Report global timing after route	13
1.22	Chip Finishing Stage output	14
1.23	DRC I Faced	14
1.24	Modification in chip finishing script to solve shorts DRCs from fillers	14
1.25	Another type of shorts	15
1.26	Report of LVS after appylying above fix	15
1.27	StarRC cmd modification	16
1.28	Global time before eco fix in Prime time	17
1.29	insert buffer to fix hold	17
1.30	Global time after fix hold and setup in Prime time	18
1.31	inspect worst path	18
1.32	timing delay calculation schematic	19
1.33	Report delay calculation for timing	19
1.34	output reports location	20
1.35	Timing NDM location	20
1.36	synthesis output for timing and its location	20
1.37	work directory for timing	20
2.1	compile for area	21
2.2	Area schematic	21

2.3	Area QoR report	22
2.4	Modifiacation in common.tcl in Area	23
2.5	Area data setup	23
2.6	Floor planning for Area	24
2.7	Power planning for Area	24
2.8	Placement stage in Area	25
2.9	cell density for area	25
2.10	pin density for area	26
2.11	Report Global timing placment	26
2.12	CTS for area	27
2.13	Report Global timing CTS for area	27
2.14	Route Area	28
2.15	Report Global timing Route for Area	28
2.16	chip finishing for Area	29
2.17	Modification in power plan for DRCs	29
2.18	Modification in chip finishing script for DRCs fix	29
2.19	DRCs Before fix	30
2.20	DRCs After fix	30
2.21	StarRC Area setup	31
2.22	Area Global time before applying eco fix	32
2.23	Applying insert buffer to hold fixing	32
2.24	remove cell to setup fixing	33
2.25	Histogram before fix	33
2.26	Histogram after fix	34
2.27	Area delay calculation	34
2.28	Delay calculation report .jpeg	35
2.29	Area outputs	36
2.30	Nmd Area location	36
2.31	Synthesis outputs for area and its location	36
2.32	work directory for area	36
3.1	compile for power	37
3.2	compile for power schematic	37
3.3	compile for power QoR report	38
3.4	Modification in common.tcl for power	39
3.5	compile for power QoR report	39
3.6	Floorplanning for power	40
3.7	power planning for power	41
3.8	placment for power	41
3.9	power cell denisty	42
3.10	power pin denisty	42
3.11	power placment global timing	43
3.12	power CTS Highlight	44
3.13	Power CTS global timing	44
3.14	power routing	45
3.15	Power routing global timing	45
3.16	power chip finishing	46
3.17	power drc fix	46

3.18 StarRC power setup	47
3.19 Global timing before fix eco	48
3.20 insert buffer fixing method	49
3.21 Global timing After fixing	49
3.22 Histogram AFTER FIX	50
3.23 POWER inspect worst path	50
3.24 schematic delay calculation	51
3.25 Report delay calculation	51
3.26 Power outputs location	52
3.27 POWER NDM location	52
3.28 synthesis outputs for power and its location	52
3.29 work directory for power	52

Chapter 1

PnR Flow Using Compile for Timing

1.1 Compiling

This suggests the design process is likely targeting a scenario where timing closure (meeting speed requirements) is critical, and area is moderately important, but power consumption is not a concern—possibly for a prototype, a design where power is managed externally, or a scenario where the technology library inherently has low power characteristics.

```
compile -exact_map -map_effort high -area_effort medium -power_effort none
```

Figure 1.1: compile for timing

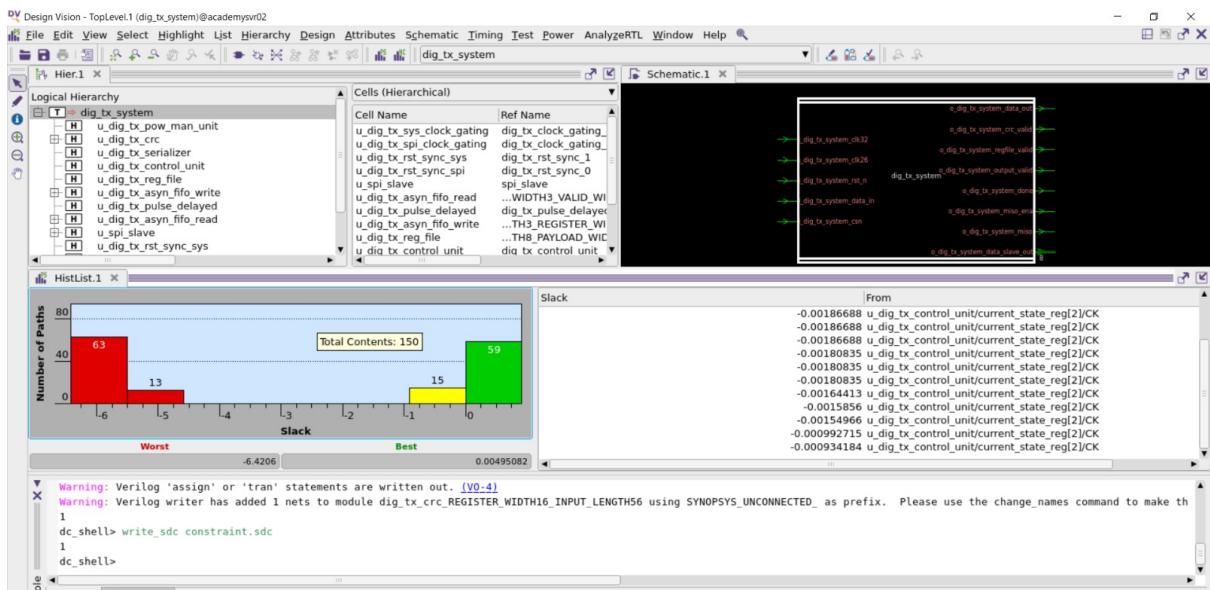


Figure 1.2: path slacks

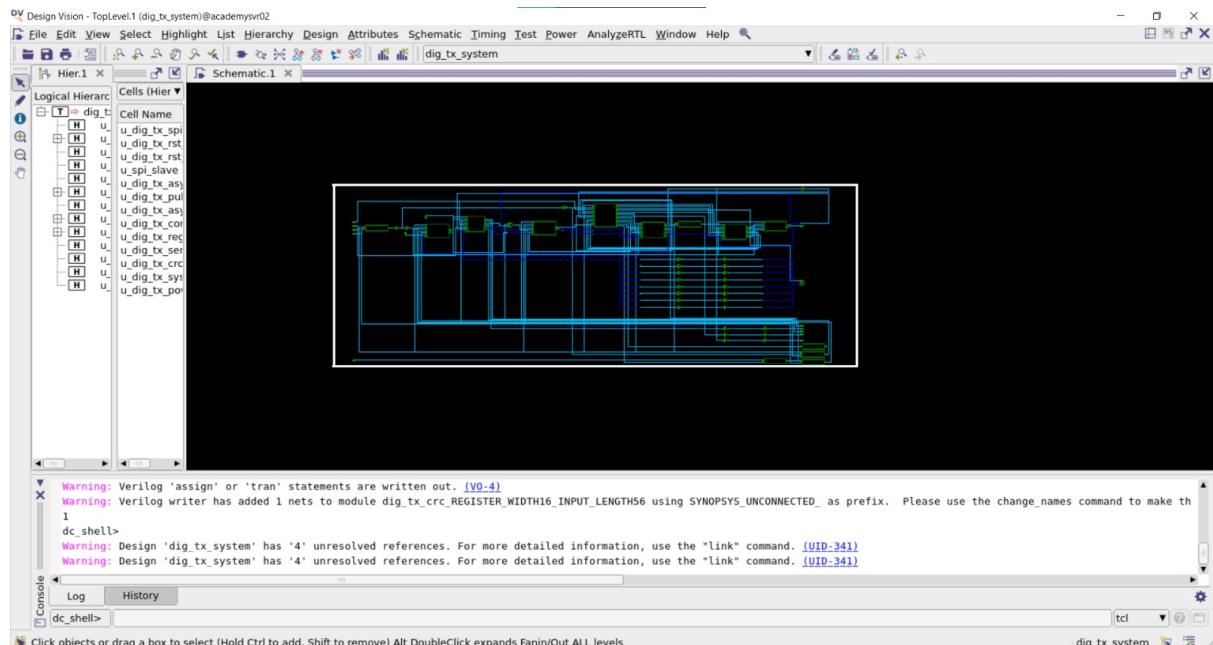


Figure 1.3: schematic of design

Design WNS: 6.42 TNS: 105.40 Number of Violating Paths: 132

Design (Hold) WNS: 0.12 TNS: 21.52 Number of Violating Paths: 334

Figure 1.4: Number of setup and hold violation in qor report

```
dc_shell> size_cell u_dig_tx_reg_file/U51 SAEDLVT14_NR2_MM_12
{u_dig_tx_reg_file/U51}
dc_shell> report_timing -max_paths 10 > ./output/${DESIGN_NAME}_timing_time_reports.log
dc_shell> size_cell u_dig_tx_control_unit/U32 SAEDLVT14_ND2_CDC_4
{u_dig_tx_control_unit/U32}
dc_shell> report_timing -max_paths 10 > ./output/${DESIGN_NAME}_timing_time_reports.log
dc_shell> size_cell u_dig_tx_reg_file/U41 SAEDLVT14_ND2_CDC_4
{u_dig_tx_reg_file/U41}
dc_shell> report_timing -max_paths 10 > ./output/${DESIGN_NAME}_timing_time_reports.log
dc_shell> report_qor > ./output/${DESIGN_NAME}_qor_time_reports.log
dc_shell>
```

Figure 1.5: size cells to reduce the cell delay

Design WNS: 6.42 TNS: 88.53 Number of Violating Paths: 99

Design (Hold) WNS: 0.12 TNS: 21.64 Number of Violating Paths: 336

Figure 1.6: After applying size cells affect in qor report

```
set_driving_cell -library saedl4lvt -base_tt0p8v25c -lib_cell SAEDLVT14_BUF_S_20 -pin X [all_inputs]
set_load 50 [all_outputs]
```

Figure 1.7: Modification of the error in constraint

Area

```
-----
Combinational Area:      458.474400
Noncombinational Area:   391.963205
Buf/Inv Area:           127.205999
Total Buffer Area:       46.31
Total Inverter Area:    84.85
Macro/Black Box Area:   0.000000
Net Area:               1046.442871
-----
Cell Area:              850.437605
Design Area:             1896.880476
```

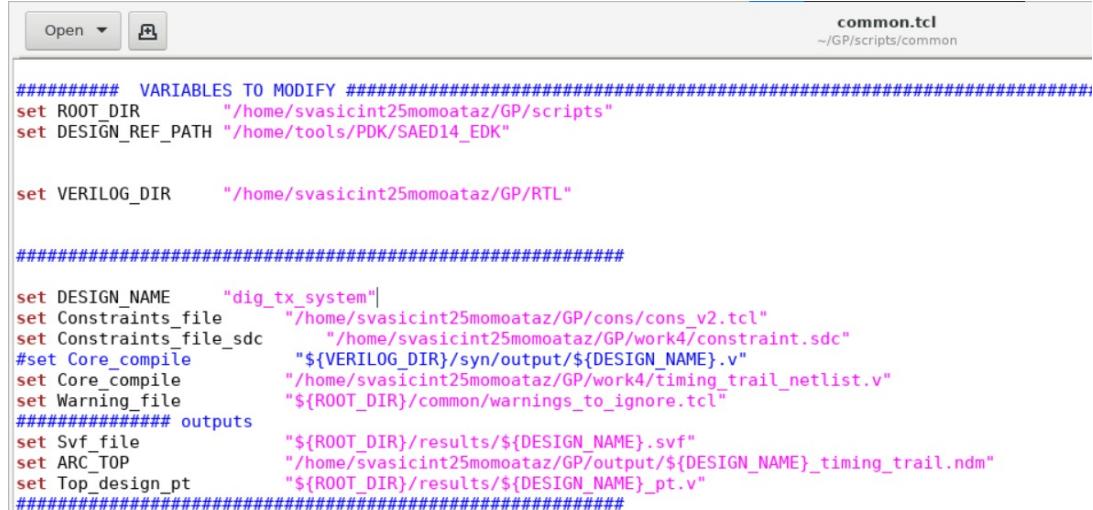
Design Rules

```
-----
Total Number of Nets:    1812
Nets With Violations:   15
Max Trans Violations:   15
Max Cap Violations:    15
-----
```

Figure 1.8: Total area and design rule in qor report

1.2 Setup Data

Data setup in PnR aims to create a robust and consistent starting point that allows the tool to transform the logical netlist into a physical layout while adhering to the design's functional and performance requirements.



```

common.tcl
~/GP/scripts/common

#####
##### VARIABLES TO MODIFY #####
#####
set ROOT_DIR      "/home/svasicint25momoataz/GP/scripts"
set DESIGN_REF_PATH "/home/tools/PDK/SAED14_EDK"

set VERILOG_DIR      "/home/svasicint25momoataz/GP/RTL"

#####
##### DESIGN DEFINITION #####
#####
set DESIGN_NAME      "dig_tx_system"
set Constraints_file      "/home/svasicint25momoataz/GP/cons/cons_v2.tcl"
set Constraints_file_sdc      "/home/svasicint25momoataz/GP/work4/constraint.sdc"
#set Core_compile      "${VERILOG_DIR}/syn/output/${DESIGN_NAME}.v"
set Core_compile      "/home/svasicint25momoataz/GP/work4/timing_trail_netlist.v"
set Warning_file      "${ROOT_DIR}/common/warnings_to_ignore.tcl"
#####
##### OUTPUTS #####
#####
set Svf_file      "${ROOT_DIR}/results/${DESIGN_NAME}.svf"
set ARC_TOP      "/home/svasicint25momoataz/GP/output/${DESIGN_NAME}_timing_trail.ndm"
set Top_design_pt      "${ROOT_DIR}/results/${DESIGN_NAME}_pt.v"
#####
#####

```

Figure 1.9: Modification of common.tcl to start PnR for timing trial

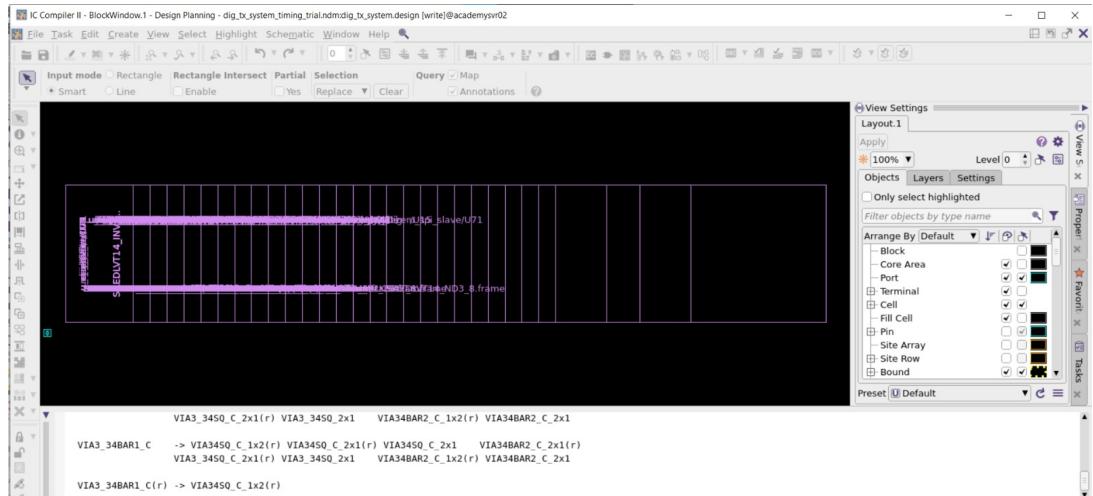


Figure 1.10: Data setup of timing trial ndm

1.3 Floor Plan

Floorplanning in PnR aims to establish a high-level physical structure that balances area, timing, power, and routability, setting the stage for successful downstream implementation and optimization in the physical design flow.

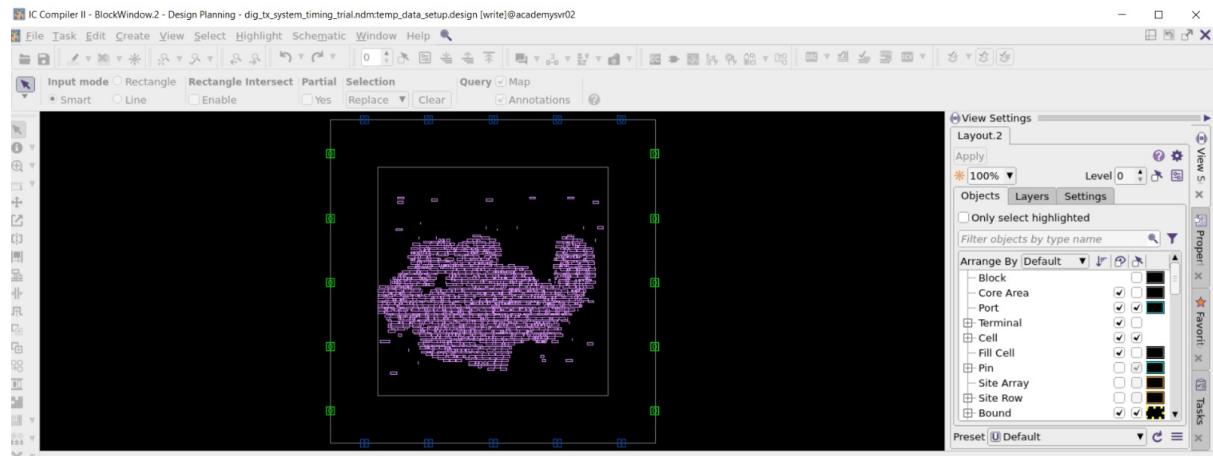


Figure 1.11: Floor planning in timing trail

1.4 Power Plan

power planning in PnR aims to create a well-designed PDN that ensures reliable operation, meets power and performance targets, and supports the overall physical design flow

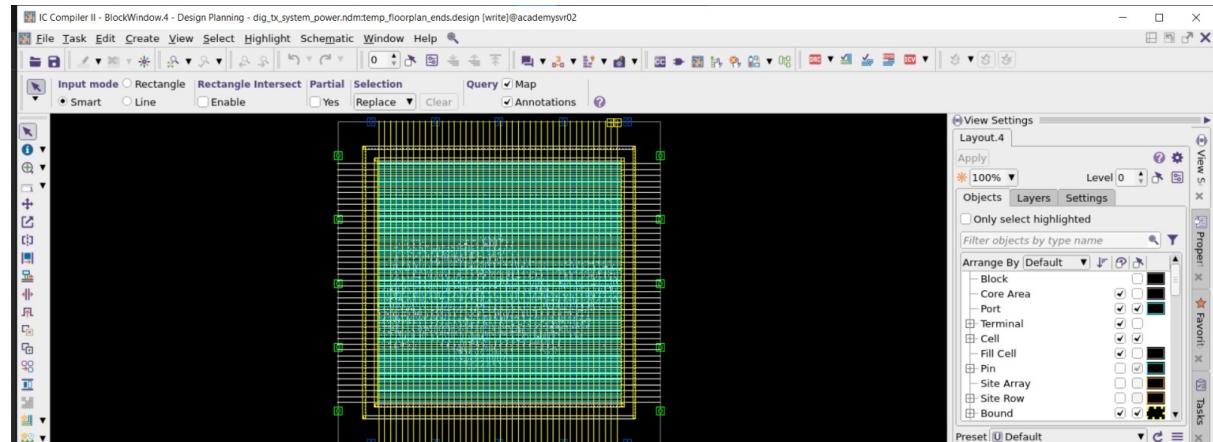


Figure 1.12: power planning for timing trail

```
create_pg_ring_pattern \
    ring_pattern \
    -vertical_layer M7 -horizontal_layer M6 \
    -vertical_width 1 -horizontal_width 1 \
    -vertical_spacing 3 -horizontal_spacing 3
```

Figure 1.13: Modification of power planning script as specified in floor plan

1.5 Placement

The placement stage in PnR aims to optimize the physical locations of cells and macros to meet timing constraints and reduce wire lengths. It manages congestion and balances area utilization for efficient silicon use. It supports power distribution by aligning with the power grid to minimize IR drop. The stage respects the design hierarchy, facilitating further optimization. Overall, it lays a strong foundation for successful routing and timing closure.

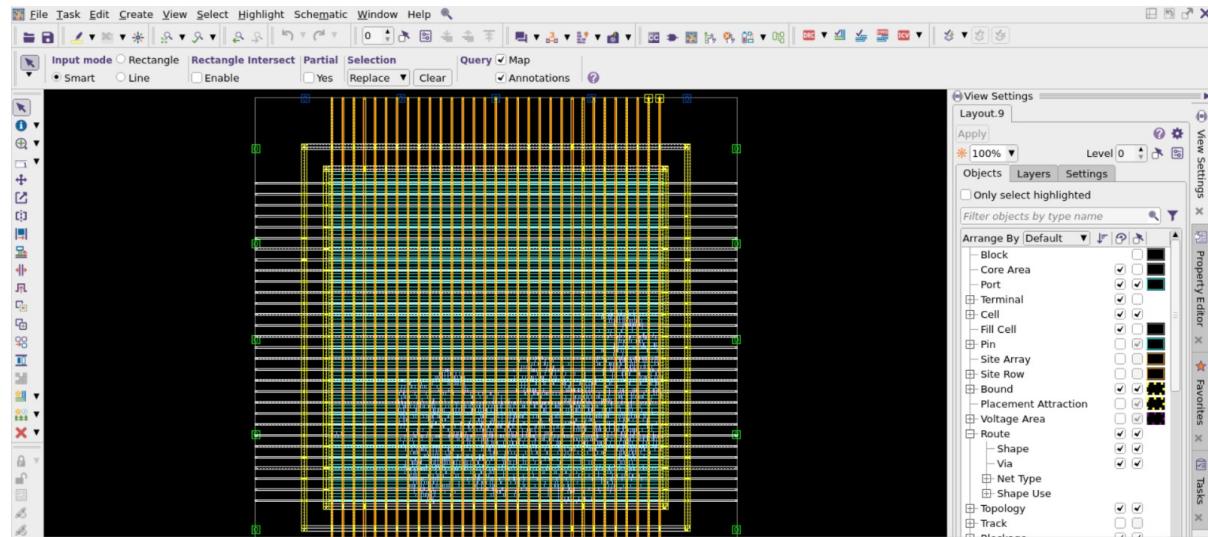


Figure 1.14: placement stage

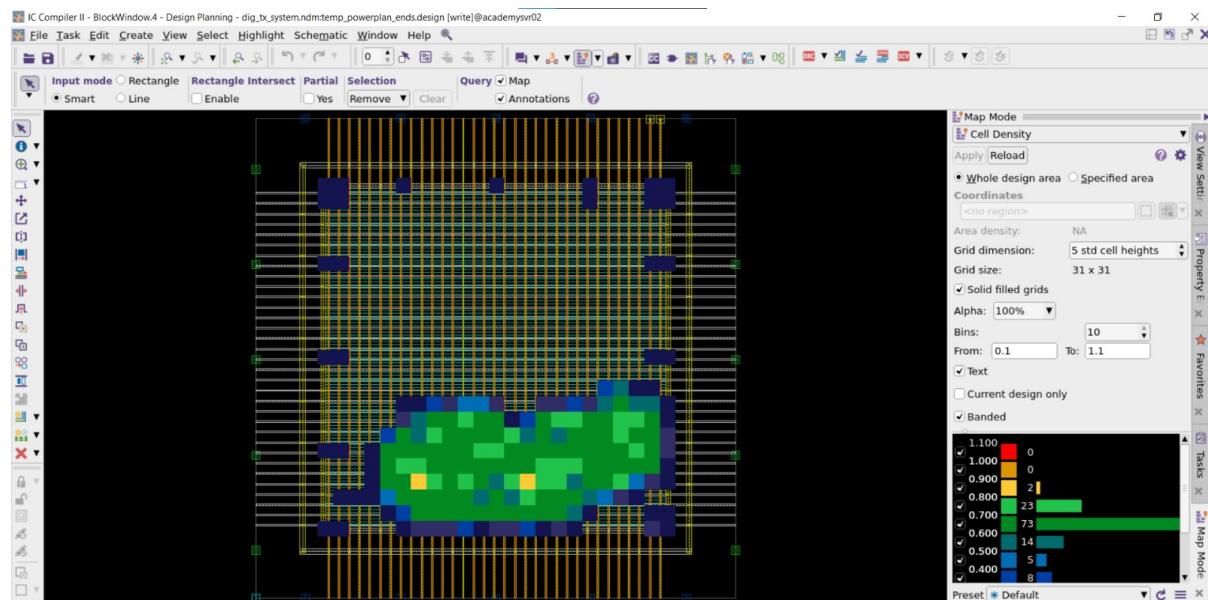


Figure 1.15: cell density of timing trail

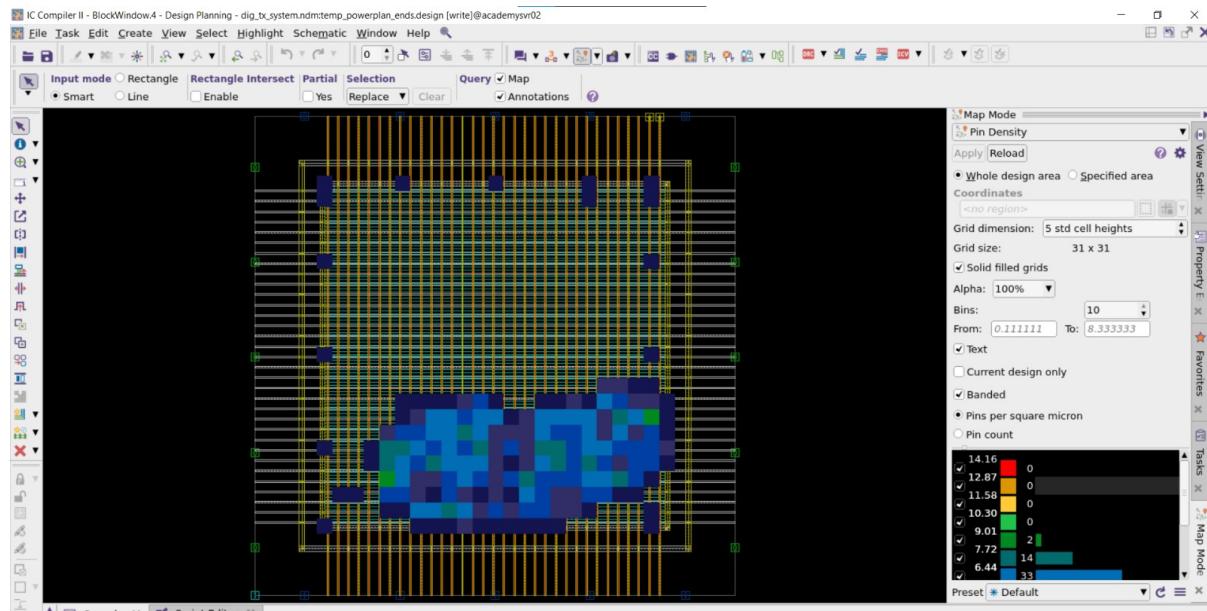


Figure 1.16: pin density of timing trail

```
*****
Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Tue Aug 19 14:50:42 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-7.050	0.000	-0.044	-7.050	-6.224
TNS	-91.894	0.000	-0.742	-84.928	-6.224
NUM	42	0	27	14	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.192	-0.192	0.000	0.000	0.000
TNS	-38.896	-38.896	0.000	0.000	0.000
NUM	368	368	0	0	0

Figure 1.17: Report global timing after placement

1.6 CTS

The goal of Clock Tree Synthesis (CTS) in the PnR process is to design and implement an efficient clock distribution network to deliver clock signals to all sequential elements with minimal skew and latency. It optimizes timing by ensuring clock signals arrive within specified constraints, supporting setup and hold time requirements. CTS reduces power consumption by minimizing clock buffer usage and optimizing clock tree topology. It manages congestion by strategically placing clock buffers and inverters to avoid routing conflicts. Ultimately, it ensures reliable clocking for synchronous operation across the IC design.

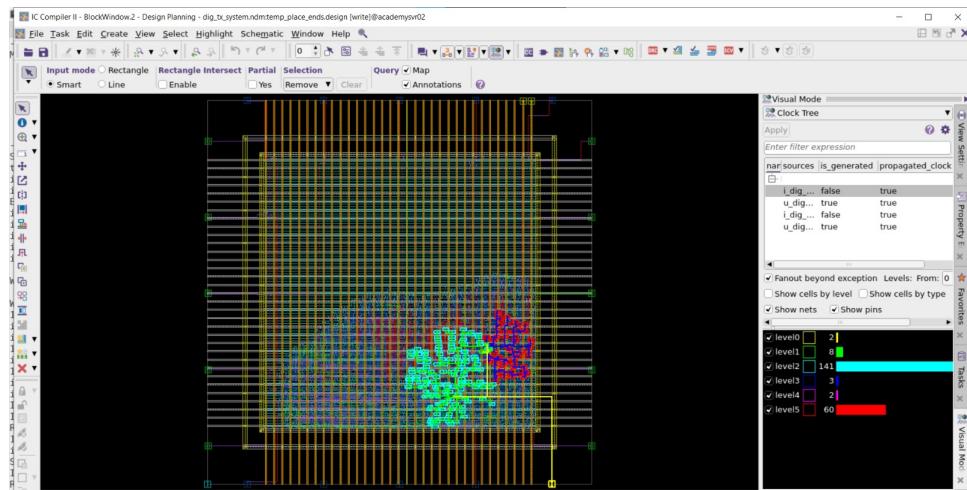


Figure 1.18: CTS highlights clock tree

```
*****
Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Tue Aug 19 15:04:31 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-6.952	0.000	-0.095	-6.952	-6.235
TNS	-92.787	0.000	-2.046	-84.507	-6.235
NUM	42	0	27	14	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.149	-0.149	0.000	0.000	0.000
TNS	-0.429	-0.429	0.000	0.000	0.000
NUM	14	14	0	0	0

1

Figure 1.19: Report global timing after CTS

1.7 Routing

The goal of the routing stage in the PnR process is to create physical connections between placed cells and blocks using metal layers, ensuring all nets are properly interconnected. It optimizes signal integrity by minimizing crosstalk, resistance, and capacitance while meeting timing constraints. Routing reduces congestion by efficiently utilizing available routing resources and avoiding design rule violations. It supports power and clock networks by integrating with the power grid and clock tree synthesis results. Ultimately, it ensures a manufacturable layout that achieves timing closure and functional correctness.

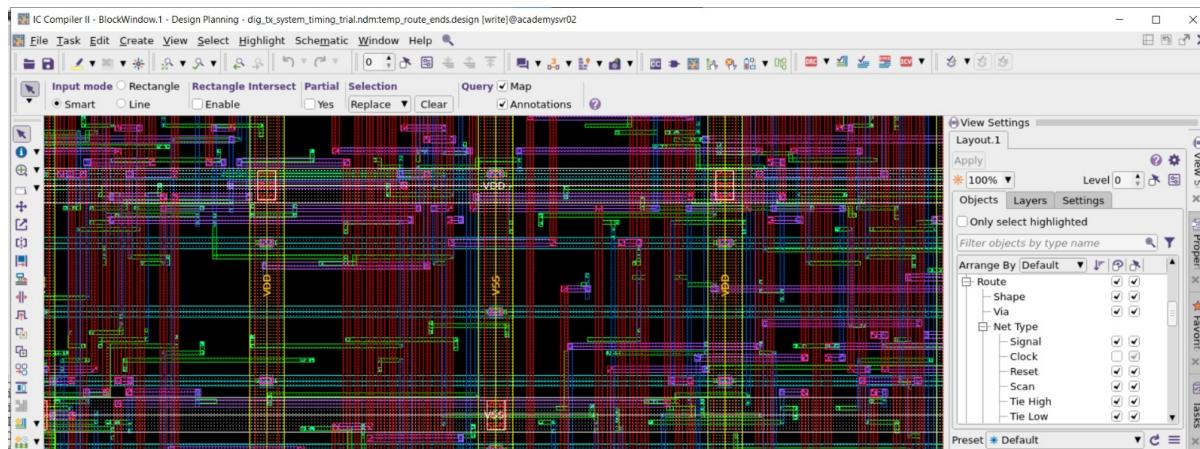


Figure 1.20: Routing stage

```
*****
Report : global timing
      -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Wed Aug 19 15:07:27 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-6.908	0.000	-0.088	-6.908	-6.188
TNS	-91.925	0.000	-1.775	-83.961	-6.188
NUM	42	0	27	14	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.148	-0.148	0.000	0.000	0.000
TNS	-0.443	-0.443	0.000	0.000	0.000
NUM	28	28	0	0	0

Figure 1.21: Report global timing after route

1.8 Chip Finishing

The goal of chip finishing is to finalize the IC layout for manufacturing by ensuring all design rules are met and the design is ready for tape-out. It optimizes the layout through post-routing steps like timing analysis, power optimization, and design rule checking (DRC) to achieve sign-off criteria. It resolves any remaining issues, such as antenna effects, metal fill, and parasitic extraction, to ensure manufacturability and reliability. The stage verifies performance through final timing, power, and signal integrity analysis to meet specifications. Ultimately, it prepares a GDSII file for fabrication, marking the completion of the physical design process i faced some of DRCs i solved some of them by remove filler and another by remove nets and use command route eco -open nets driven to true to solve this shorts as shown in fig 24 and 25 .

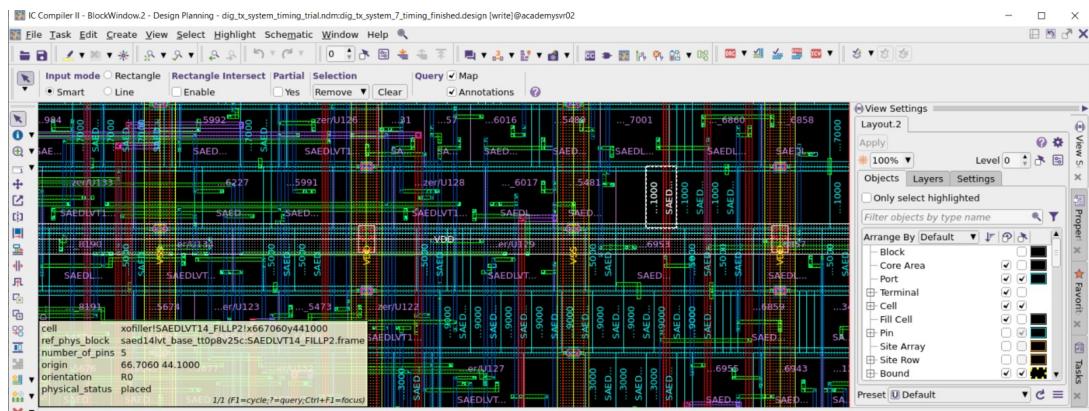


Figure 1.22: Chip Finishing Stage output

```
=====
Maximum number of violations is set to 1000
Abort checking when more than 1000 violations are found
All violations might not be found.
=====
Total number of input nets is 3754.
Total number of short violations is 7.
Total number of open nets is 1.
Open nets are VDD |
Total number of floating route violations is 0.

Elapsed = 0:00:03, CPU = 0:00:03
1
```

Figure 1.23: DRC I Faced

```
connect_pg_net -automatic

remove_stdcell_fillers_with_violation
```

Figure 1.24: Modification in chip finishing script to solve shorts DRCs from fillers

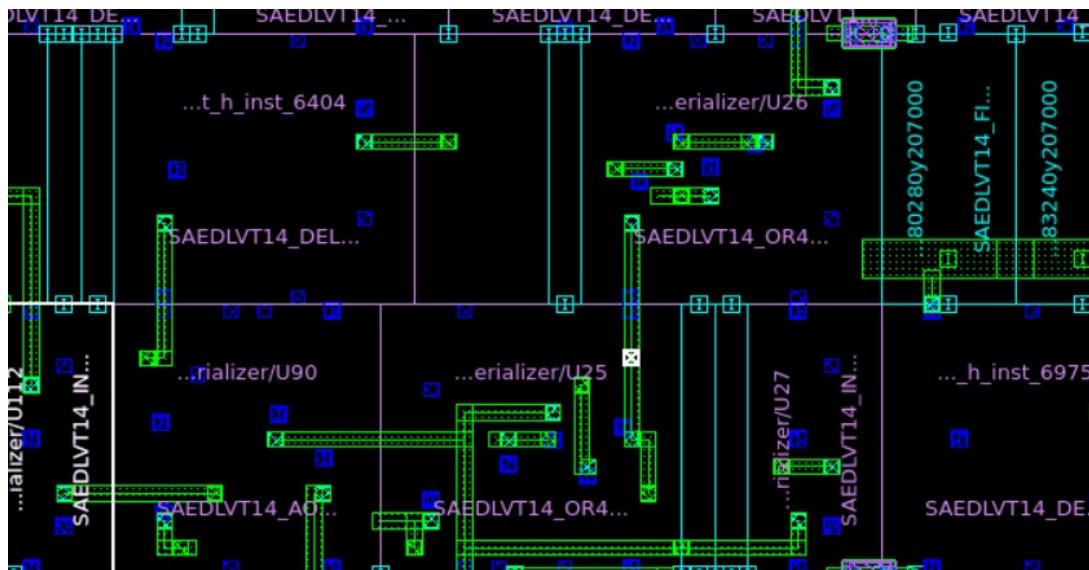


Figure 1.25: Another type of shorts

```

dig_tx_system.lvs.rpt
~/GP/PnR_timing_OUTPUTS_Trial

*step7_finishing.tcl      dig_tx_system.lvs.rpt      flow.tcl      step6_route.tcl

Information: Using 1 threads for LVS
[Check Short] Stage 1 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 1-2 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 2 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 2-2 Elapsed = 0:00:01, CPU = 0:00:01
[Check Short] Stage 3 Elapsed = 0:00:01, CPU = 0:00:01
[Check Short] End Elapsed = 0:00:01, CPU = 0:00:01
[Check Net] Init Elapsed = 0:00:01, CPU = 0:00:01
Warning: Port VDD have no valid pin shapes. Skip this port. (RT-203)
Warning: Port VSS have no valid pin shapes. Skip this port. (RT-203)
[Check Net] 10% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 20% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 30% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 40% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 50% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 60% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 70% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 80% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 90% Elapsed = 0:00:02, CPU = 0:00:02
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[0][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[1][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[2][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[3][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[4][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[5][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[6][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
[Check Net] All nets are submitted.
[Check Net] 100% Elapsed = 0:00:02, CPU = 0:00:02
Information: Detected open violation for Net VDD. BBox: (0.0000 0.0000)(92.1940 91.8000). (RT-585)
Total number of input nets is 3754.
Total number of short violations is 0.
Total number of open nets is 1.
Open nets are VDD.
Total number of floating route violations is 0.

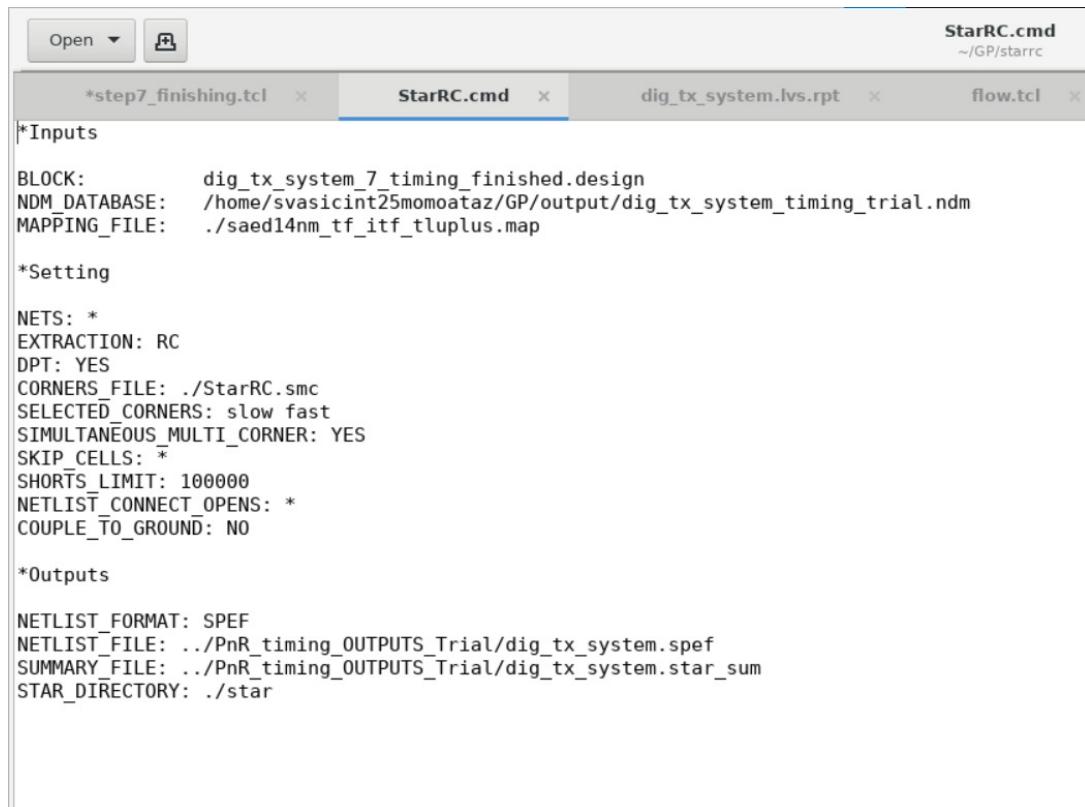
Elapsed = 0:00:02, CPU = 0:00:02

```

Figure 1.26: Report of LVS after applying above fix

1.9 StarRC and Prime Time

StarRC, a parasitic extraction tool by Synopsys, aims to accurately extract parasitic capacitance, resistance, and inductance from the routed IC layout. It supports post-layout analysis by providing precise RC data to optimize timing, power, and signal integrity. Its goal is to ensure the extracted netlist reflects real-world electrical behavior for reliable simulation and sign-off. It facilitates design closure by identifying parasitic-related issues early in the flow. Ultimately, it prepares the design for manufacturing by integrating with timing and power analysis tools and PrimeTime, a static timing analysis (STA) tool by Synopsys, aims to verify that the IC design meets timing constraints across all operating conditions. It analyzes setup and hold times using extracted parasitics to ensure timing closure before sign-off. Its goal is to identify and resolve timing violations, optimizing performance and reliability of the design. It supports multi-corner and multi-mode analysis to account for process, voltage, and temperature variations. Ultimately, it ensures the design is functionally correct and ready for tape-out.



```

StarRC.cmd
~/GP/starrc

*step7_finishing.tcl  ×   StarRC.cmd  ×   dig_tx_system.lvs.rpt  ×   flow.tcl  ×

*Inputs
BLOCK:      dig_tx_system_7_timing_finished.design
NDM_DATABASE: /home/svasicint25momoataz/GP/output/dig_tx_system_timing_trial.ndm
MAPPING_FILE: ./saed14nm_tf_itf_tluplus.map

*Setting
NETS: *
EXTRACTION: RC
DPT: YES
CORNERS_FILE: ./StarRC.smc
SELECTED_CORNERS: slow fast
SIMULTANEOUS_MULTI_CORNER: YES
SKIP_CELLS: *
SHORTS_LIMIT: 100000
NETLIST_CONNECT_OPENS: *
COUPLE_TO_GROUND: NO

*Outputs
NETLIST_FORMAT: SPEF
NETLIST_FILE: ../PnR_timing_OUTPUTS_Trial/dig_tx_system.spef
SUMMARY_FILE: ../PnR_timing_OUTPUTS_Trial/dig_tx_system.star_sum
STAR_DIRECTORY: ./star

```

Figure 1.27: StarRC cmd modification

```

*****
Report : global_timing
  -format { narrow }
Design : dig_tx_system
Version: W-2024.09-SP5
Date   : Wed Aug 20 16:20:18 2025
*****


Setup violations
-----
      Total  reg->reg  in->reg  reg->out  in->out
-----
WNS      -5.63      0.00     -0.09     -5.63     -5.18
TNS      -75.45     0.00    -1.82    -68.45     -5.18
NUM       42          0        27        14         1
-----


Hold violations
-----
      Total  reg->reg  in->reg  reg->out  in->out
-----
WNS      -0.15     -0.15      0.00      0.00      0.00
TNS      -0.71     -0.71      0.00      0.00      0.00
NUM       37          37        0          0          0
-----
```

Figure 1.28: Global time before eco fix in Prime time

```

pt_shell> insert buffer -new_cell_names "clk_buf_captur4e14" -new_net_names "clk_net_d33elayed14" [get_pins u_dig_tx_asyn_fifo_write/fifom/fifo_reg[1][5]/D] [get_lib_cells */SAEDLVT14_BUF_1]
Information: Removing HyperScale Annotations from pin for buffer insertion. Annotations won't be re-added if the buffer is removed later
Warning: HyperScale annotation at pin u_dig_tx_asyn_fifo_write/fifom/fifo_reg[1][5]/D is not removed because it is not connected to driving port. (NED-079)
Information: Invalidating logical update. (PTE-139)
Information: Invalidating logical update. (PTE-139)
Information: Inserted 'clk_buf_captur4e14' at 'u_dig_tx_asyn_fifo_write/fifom/fifo_reg[1][5]/D' with 'saedlvt_base_tt0p8v25c/SAEDLVT14_BUF_1'. (NED-046)
nt shallis report timing -delay tune min -max nathe 5
```

Figure 1.29: insert buffer to fix hold

```

1
pt_shell> report_global_timing
*****
Report : global_timing
  -format { narrow }
Design : dig_tx_system
Version: W-2024.09-SP5
Date   : Wed Aug 20 19:46:47 2025
*****


Setup violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
WNS      -5.79      0.00     -0.09     -5.79     -5.18
TNS     -75.66      0.00    -1.82    -68.66     -5.18
NUM       42          0        27        14         1
-----
```

No hold violations found.

Figure 1.30: Global time after fix hold and setup in Prime time

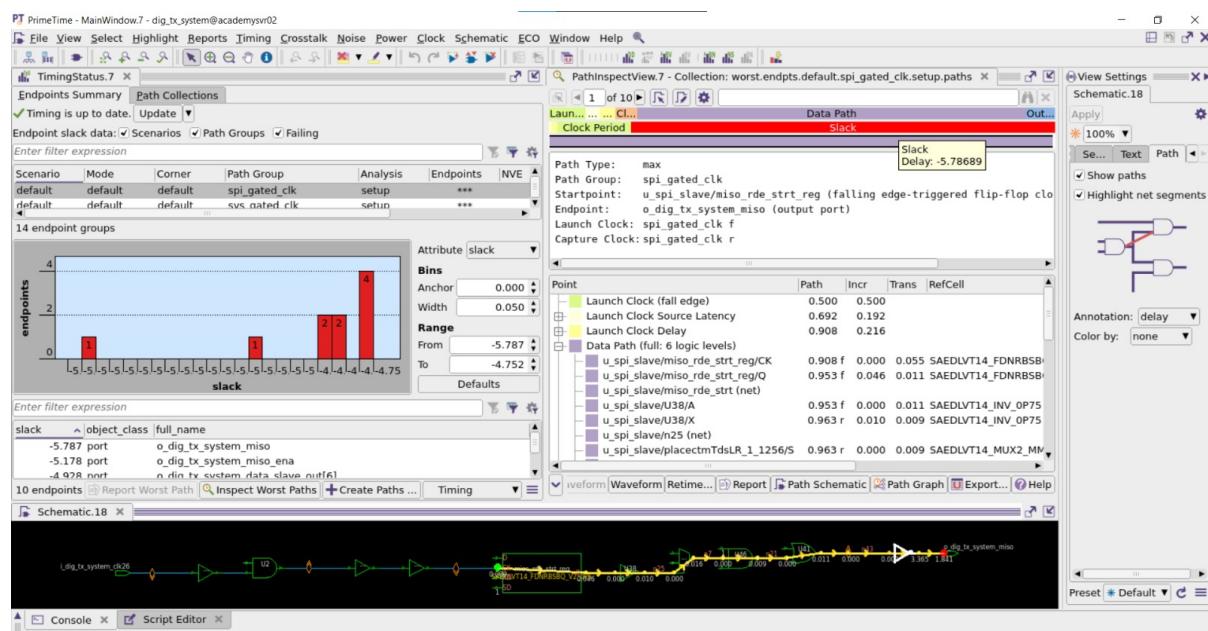


Figure 1.31: inspect worst path

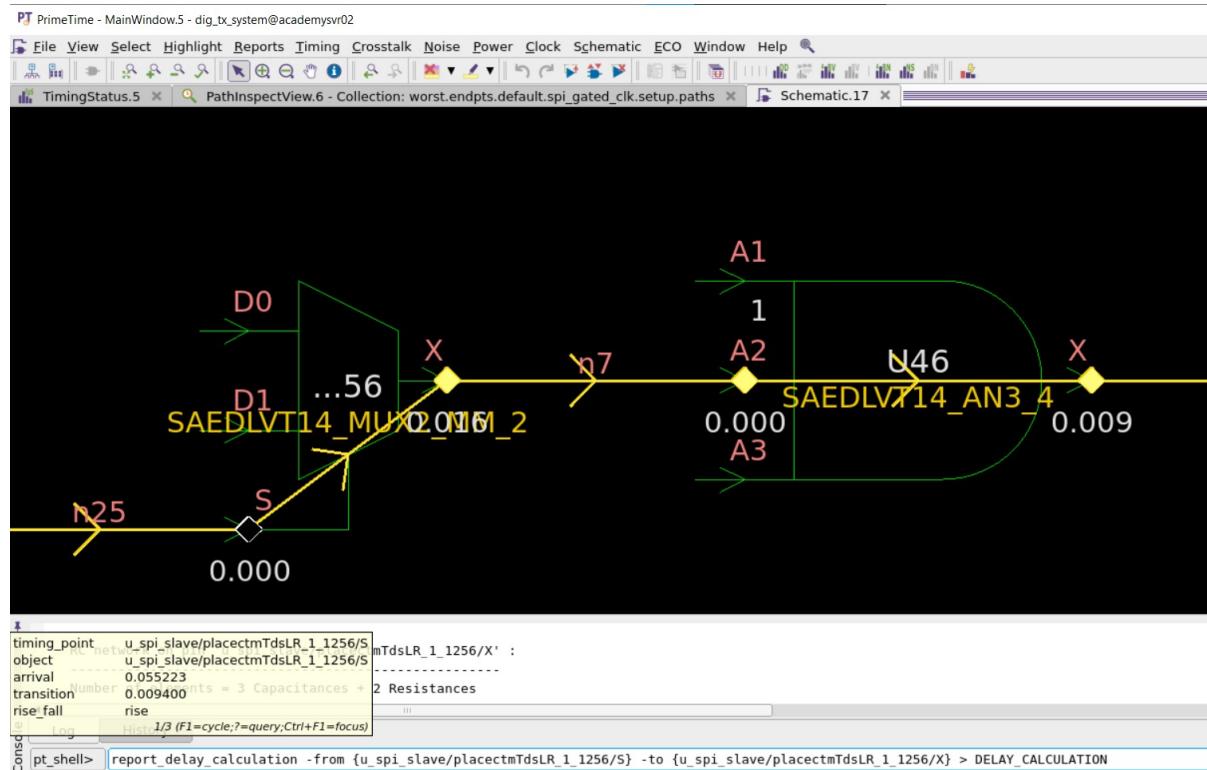


Figure 1.32: timing delay calculation schematic

```
*****
Report : delay_calculation
Design : dig_tx_system
Version: W-2024.09-SP5
Date   : Wed Aug 20 18:04:17 2025
*****  
  

From pin: u_spi_slave/placectmTdsLR_1_1256/S
To pin:  u_spi_slave/placectmTdsLR_1_1256/X
Main Library Units: 1ns 1pF 1kOhm  
  

Library: 'saedlvt_base_tt0p8v25c'
Library Units: 1ns 1pF 1kOhm
Library Cell: 'SAEDLVT14_MUX2_MM_2'
arc sense:           positive_unate
arc type:           cell  
  

RC network on pin 'u_spi_slave/placectmTdsLR_1_1256/X' :
-----  

Number of elements = 3 Capacitances + 2 Resistances
Total capacitance = 0.002234 pF
Total capacitance = 0.002234 (in library unit)
Total resistance = 0.033232 Kohm  
  

Rise          Fall
-----  

Input transition time = 0.009400    0.009383 (in library unit)
Effective capacitance = 0.002234    0.002234 (in pF)
Effective capacitance = 0.002234    0.002234 (in library unit)
Drive resistance     = 0.001000    0.001000 (in Kohm)
Output transition time = 0.004956    0.004995 (in library unit)
Cell delay          = 0.012437    0.012236 (in library unit)  
  

From pin: u_spi_slave/placectmTdsLR_1_1256/S
To pin:  u_spi_slave/placectmTdsLR_1_1256/X
Main Library Units: 1ns 1pF 1kOhm  
  

Library: 'saedlvt_base_tt0p8v25c'
Library Units: 1ns 1pF 1kOhm
Library Cell: 'SAEDLVT14_MUX2_MM_2'
arc sense:           positive_unate
arc SDF condition: D0==1'b0&&D1==1'b1
```

Figure 1.33: Report delay calculation for timing

1.10 Note

All the reports generating from compile for timing trail in this path and netlist in work directory

```
/home/svasicint25momoataz/GP/PnR_timing_OUTPUTS_Trial.
```

Figure 1.34: output reports location

```
/home/svasicint25momoataz/GP/output/dig_tx_system_timing_trial.ndm
```

Figure 1.35: Timing NDM location

```
## reporting and output
report_timing > ../output/${DESIGN_NAME}_timing_power_reports.log
report_qor > ../output/${DESIGN_NAME}.qor_power_reports.log
report_area -hierarchy > ../output/${DESIGN_NAME}_area_power_reports.log
report_power -hierarchy > ../output/${DESIGN_NAME}_power_power_reports.log
```

Figure 1.36: synthesis output for timing and its location

```
[svasicint25momoataz@academysvr02 work4]$ pwd
/home/svasicint25momoataz/GP/work4
```

Figure 1.37: work directory for timing

Chapter 2

PnR Flow Using Compile for Area

2.1 Compiling

The compile strategy aims to synthesize the RTL design into a gate-level netlist with a balanced mapping effort. It prioritizes high area optimization to minimize silicon usage by selecting efficient cell combinations. The medium mapping effort ensures a reasonable trade-off between runtime and optimization for timing and logic structure. Power optimization is ignored, indicating it's not a focus, possibly for designs where power is managed externally. Overall, it targets a compact layout with acceptable timing, suitable for area-constrained applications.

```
compile -map_effort medium -area_effort high -power_effort none
```

Figure 2.1: compile for area

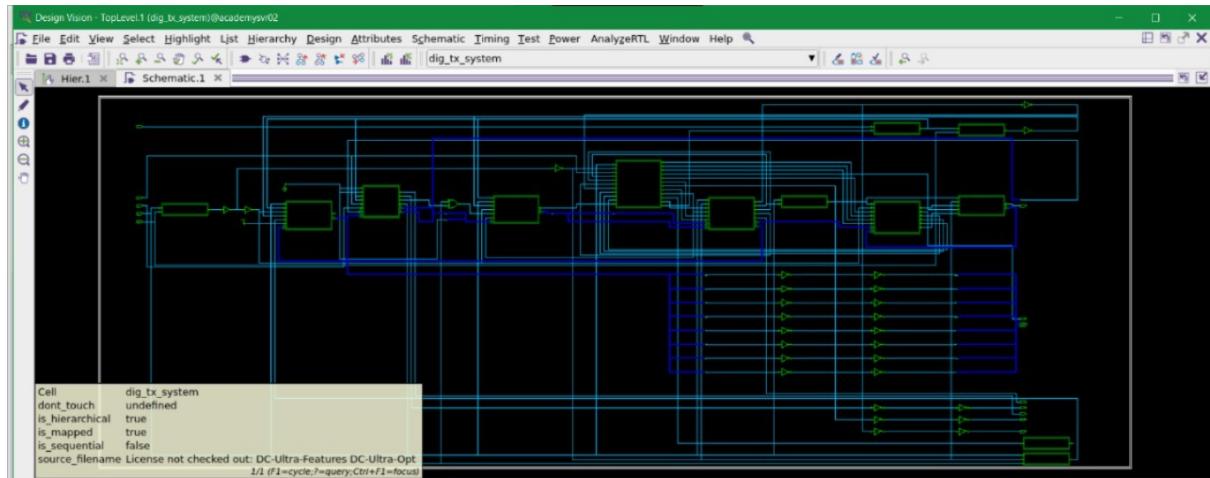


Figure 2.2: Area schematic

Area

```
-----  
Combinational Area:      452.036400  
Noncombinational Area:   392.806805  
Buf/Inv Area:           123.254399  
Total Buffer Area:       45.91  
Total Inverter Area:    82.94  
Macro/Black Box Area:   0.000000  
Net Area:               1040.905167  
-----  
Cell Area:               844.843205  
Design Area:              1885.748372
```

Design Rules

```
-----  
Total Number of Nets:     1796  
Nets With Violations:   15  
Max Trans Violations:   15  
Max Cap Violations:    15  
-----
```

Hostname: academysvr02

Compile CPU Statistics

```
-----  
Resource Sharing:          0.83  
Logic Optimization:        7.21  
Mapping Optimization:      16.55  
-----  
Overall Compile Time:     42.58  
Overall Compile Wall Clock Time: 43.64  
-----
```

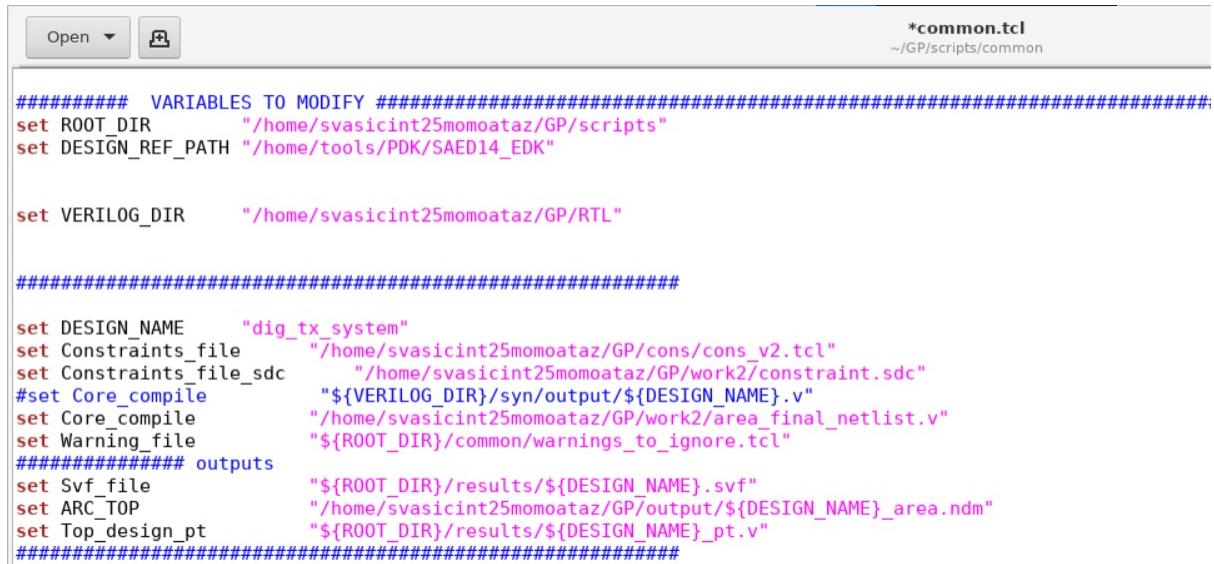
Design WNS: 6.41 TNS: 110.97 Number of Violating Paths: 200

Design (Hold) WNS: 0.12 TNS: 21.29 Number of Violating Paths: 331

Figure 2.3: Area QoR report

2.2 Setup Data

The goal of data setup in PnR is to compile and validate all essential design data, including netlists, technology libraries, and constraints. It ensures accurate definition of timing, power, and area constraints to steer the physical design process. The setup provides initial parasitic estimates and floorplan details for precise optimization. It minimizes iterations by aligning with performance targets, facilitating design closure. Ultimately, it establishes a robust foundation for successful placement, routing, and sign-off stages.



```
*common.tcl
~/GP/scripts/common

#####
# VARIABLES TO MODIFY #####
set ROOT_DIR      "/home/svasicint25momoataz/GP/scripts"
set DESIGN_REF_PATH "/home/tools/PDK/SAED14_EDK"

set VERILOG_DIR      "/home/svasicint25momoataz/GP/RTL"

#####
set DESIGN_NAME      "dig_tx_system"
set Constraints_file      "/home/svasicint25momoataz/GP/cons/cons_v2.tcl"
set Constraints_file_sdc      "/home/svasicint25momoataz/GP/work2/constraint.sdc"
#set Core_compile      "${VERILOG_DIR}/syn/output/${DESIGN_NAME}.v"
set Core_compile      "/home/svasicint25momoataz/GP/work2/area_final_netlist.v"
set Warning_file      "${ROOT_DIR}/common/warnings_to_ignore.tcl"
#####
# outputs
set Svf_file      "${ROOT_DIR}/results/${DESIGN_NAME}.svf"
set ARC_TOP      "/home/svasicint25momoataz/GP/output/${DESIGN_NAME}_area.ndm"
set Top_design_pt      "${ROOT_DIR}/results/${DESIGN_NAME}_pt.v"
#####


```

Figure 2.4: Modifiacation in common.tcl in Area

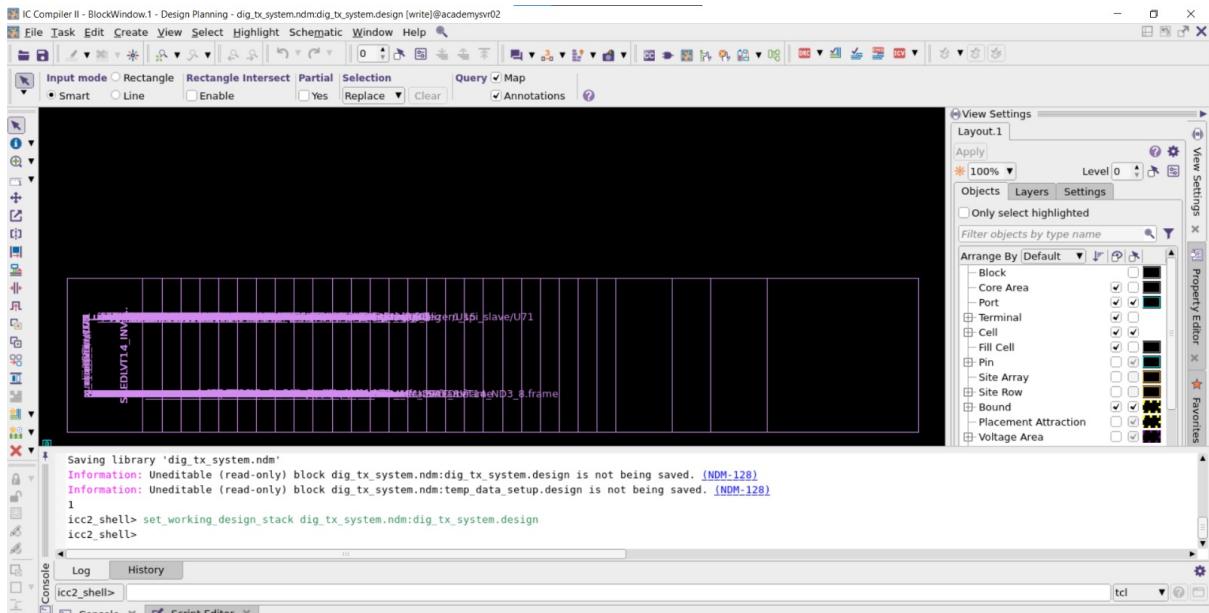


Figure 2.5: Area data setup

2.3 Floor Plan

The goal of floorplanning in the PnR process is to create an initial physical layout blueprint, optimizing the arrangement of blocks, macros, and cells within the chip. It maximizes area utilization while ensuring sufficient space for routing and avoiding overlaps. The stage supports timing closure by reducing wire lengths and aligning critical paths with constraints. It facilitates power planning by defining the power grid structure to minimize IR drop. Ultimately, it establishes a foundation for efficient placement, routing, and overall design hierarchy.

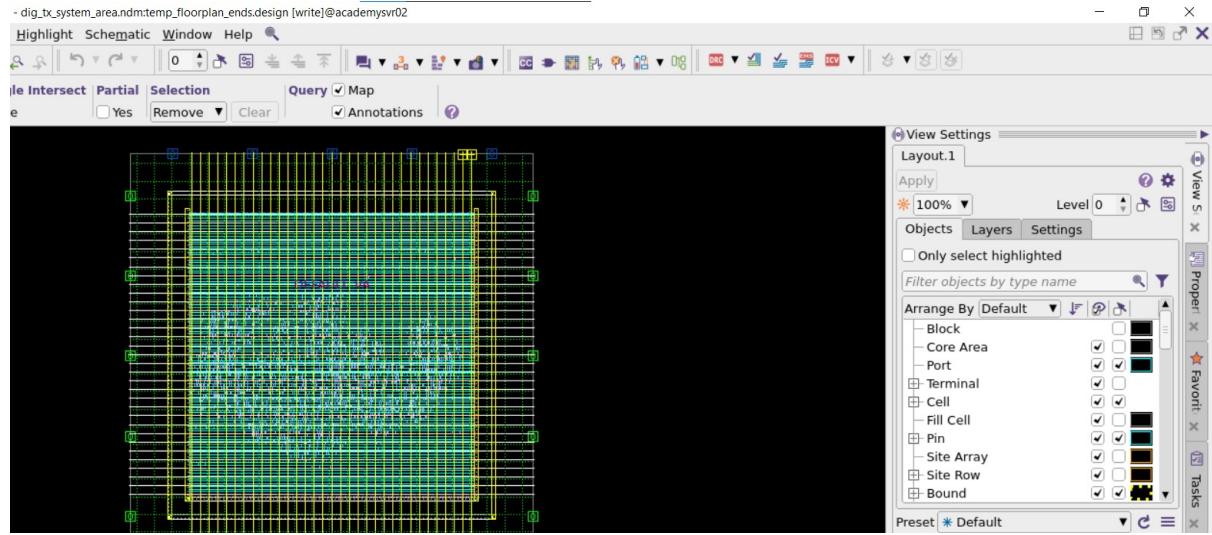


Figure 2.6: Floor planning for Area

2.4 Power Plan

The goal of power planning in the PnR process is to design an efficient power distribution network (PDN) to deliver stable voltage to all circuit components. It differs from floorplanning by focusing specifically on minimizing IR drop and noise, rather than just layout arrangement. While floorplanning sets the spatial framework, power planning optimizes power grid placement and via structures to ensure uniform power delivery. It also addresses thermal management and power integrity, unlike floorplanning's emphasis on area and routing space. Ultimately, it ensures reliable operation and supports timing and performance, complementing the broader spatial goals of floorplanning.

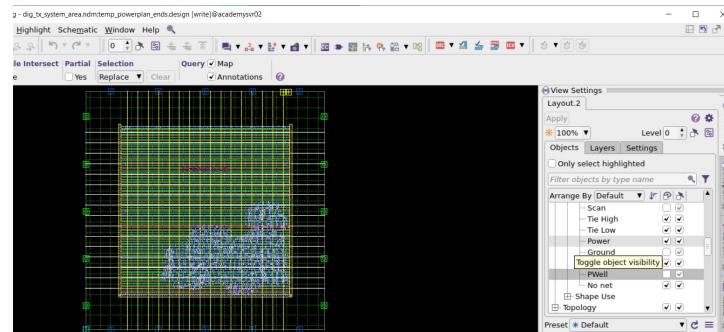


Figure 2.7: Power planning for Area

2.5 Placement

The goal of placement stage in PnR is to optimally position all cells on the chip floorplan to minimize wirelength and meet timing constraints. It ensures routability by distributing cells evenly and preventing congestion hotspots that would block routing. The placement enables timing closure by placing timing-critical cells close together to minimize interconnect delays. It achieves target utilization (0.6-0.8) while maintaining proper spacing for power distribution and DRC compliance. Ultimately, placement creates a foundation that allows clean routing completion without violations.

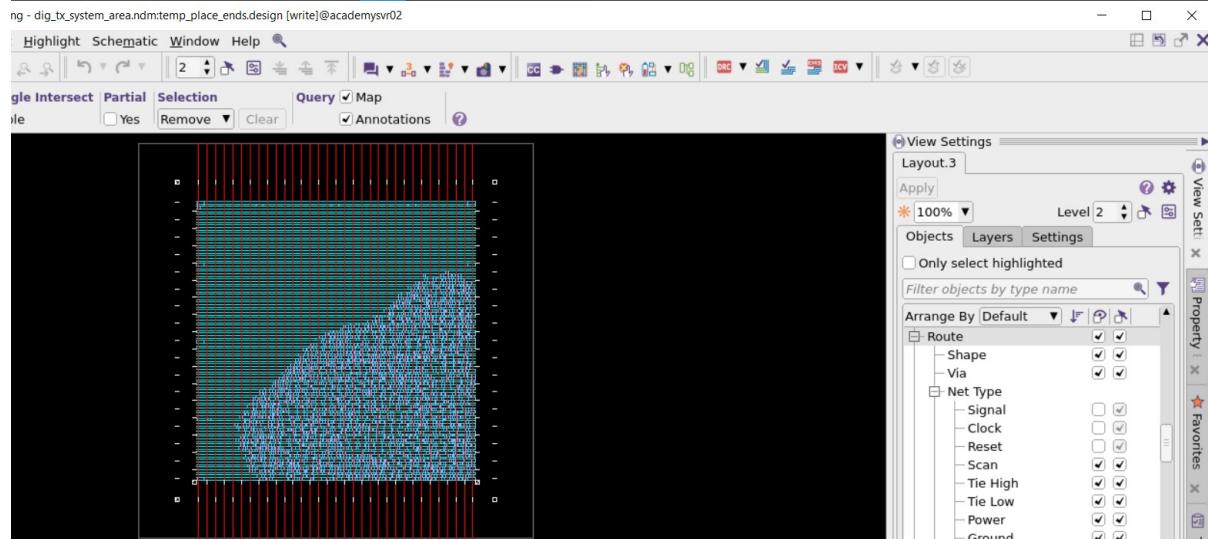


Figure 2.8: Placement stage in Area

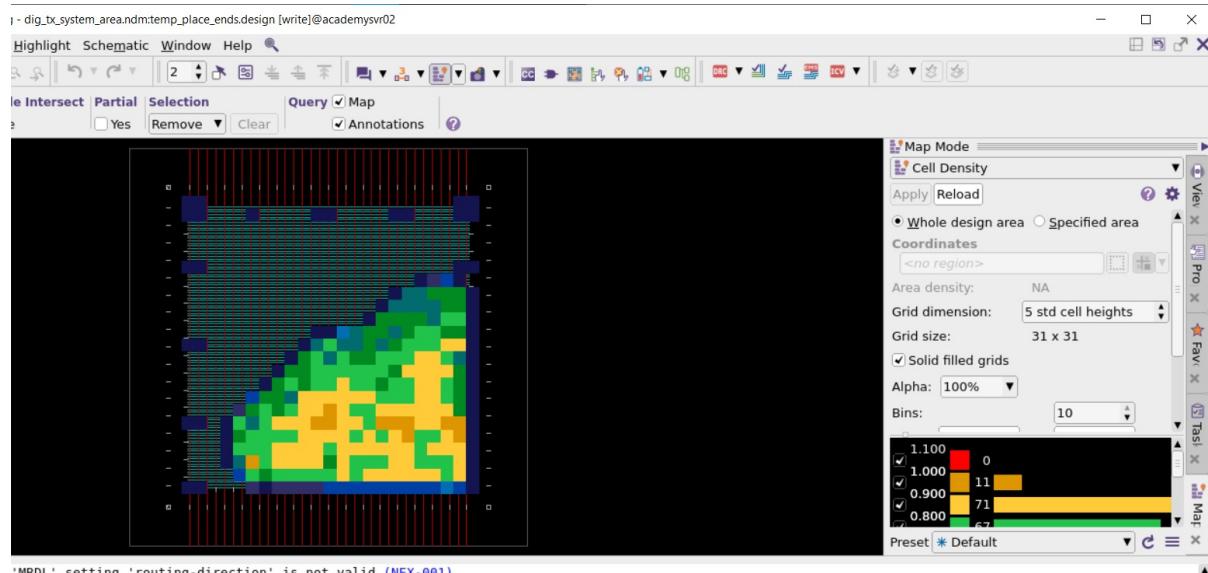


Figure 2.9: cell density for area

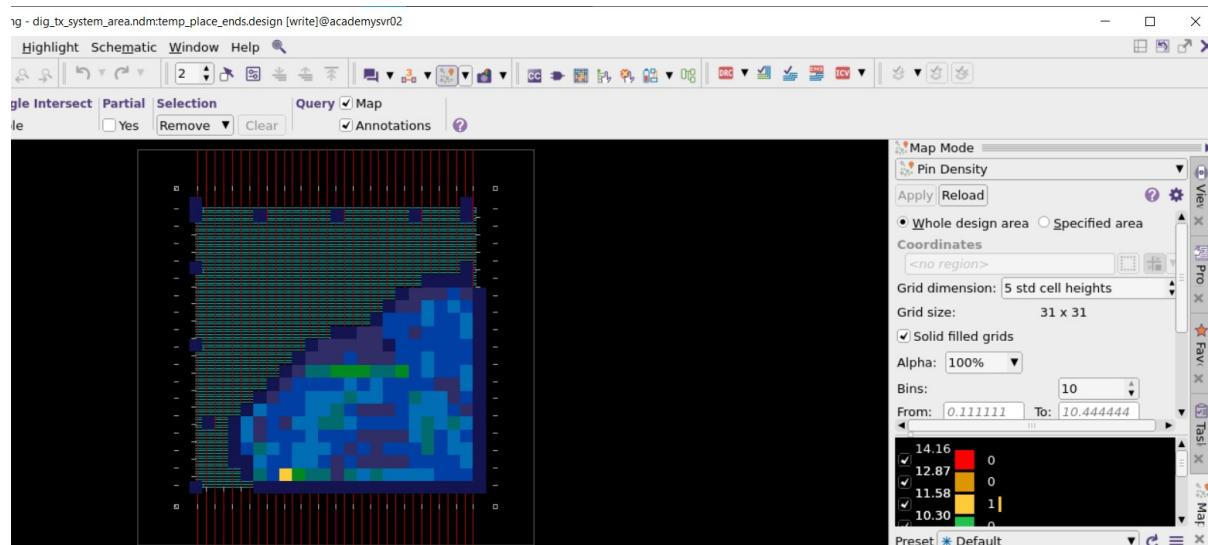


Figure 2.10: pin density for area

```
*****
Report : global timing
    -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Wed Aug 20 21:09:28 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-7.002	0.000	-0.065	-7.002	-5.970
TNS	-91.924	0.000	-0.845	-85.109	-5.970
NUM	42	0	27	14	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.164	-0.164	0.000	0.000	0.000
TNS	-38.833	-38.833	0.000	0.000	0.000
NUM	390	390	0	0	0

1

Figure 2.11: Report Global timing placement

2.6 CTS

The goal of Clock Tree Synthesis (CTS) in PnR is to create an optimized clock distribution network that delivers clock signals to all sequential elements with minimal skew and insertion delay. It ensures balanced clock tree structure by inserting buffers and inverters to equalize path delays from clock source to all flip-flops and latches. CTS minimizes clock skew across the design to prevent setup and hold time violations while managing clock latency for timing closure. It optimizes power consumption by sizing clock buffers appropriately and minimizing unnecessary switching activity in the clock network. The process creates a robust clock tree that can handle process variations and maintain signal integrity across all operating conditions.

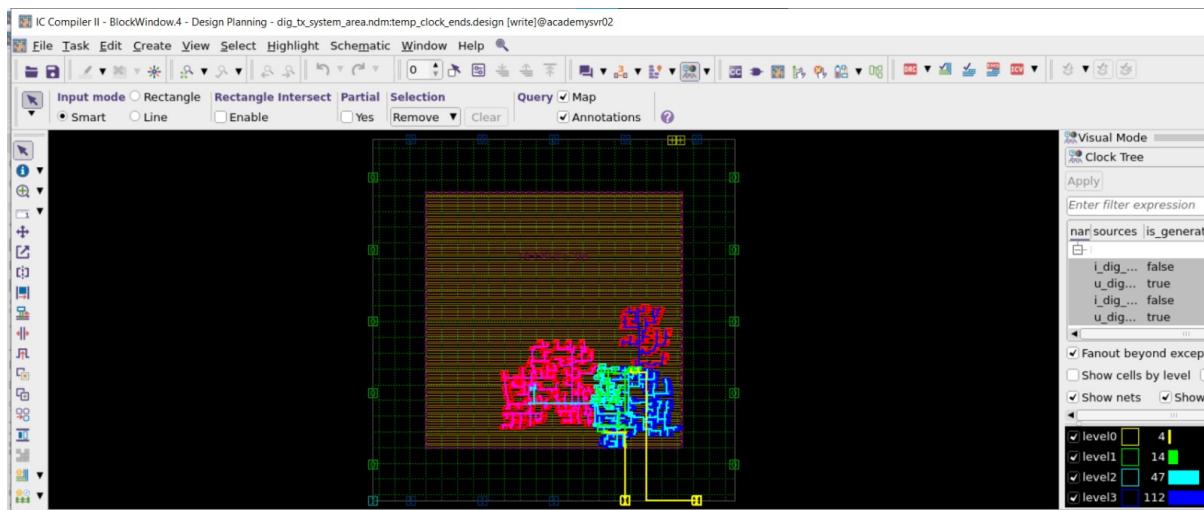


Figure 2.12: CTS for area

```
*****
Report : global timing
      -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Wed Aug 20 21:15:45 2025
*****
```

Setup violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-6.867	-0.000	-0.184	-6.867	-6.473
TNS	-96.639	-0.000	-4.665	-85.501	-6.473
NUM	43	1	27	14	1

Hold violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.139	-0.139	0.000	0.000	0.000
TNS	-0.395	-0.395	0.000	0.000	0.000
NUM	12	12	0	0	0

1

Figure 2.13: Report Global timing CTS for area

2.7 Routing

The goal of routing in PnR is to create physical wire connections between all pins according to the netlist while adhering to design rules and avoiding shorts or opens. It completes the connectivity established during placement by finding optimal paths through available metal layers and vias to minimize congestion and timing impact. Routing ensures all design rule constraints are met including minimum width, spacing, and via requirements while managing signal integrity and crosstalk effects. It optimizes wire length and layer usage to reduce power consumption and manufacturing costs while maintaining electrical performance. The process produces a fully connected, DRC-clean layout ready for signoff verification and tape-out to manufacturing.

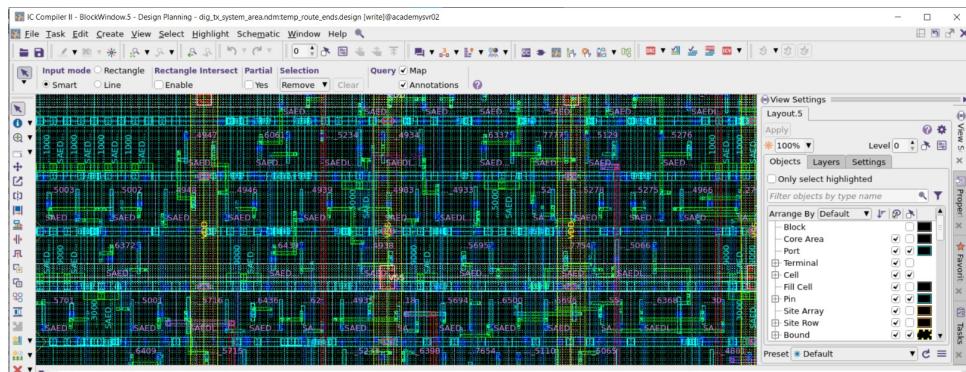


Figure 2.14: Route Area

```
*****
Report : global timing
      -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Wed Aug 20 21:20:46 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-6.753	-0.003	-0.211	-6.753	-6.455
TNS	-96.900	-0.004	-5.623	-84.818	-6.455
NUM	44	2	27	14	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.125	-0.125	0.000	0.000	0.000
TNS	-0.401	-0.401	0.000	0.000	0.000
NUM	47	47	0	0	0

Figure 2.15: Report Global timing Route for Area

2.8 Chip Finishing

The goal of chip finishing in PnR is to prepare the fully routed design for manufacturing by performing comprehensive verification and cleanup to ensure the layout meets all design rules and manufacturing requirements. It involves inserting metal fill patterns and dummy structures to satisfy foundry density rules and chemical-mechanical polishing uniformity requirements across all metal layers. Chip finishing ensures electrical correctness through final timing signoff, power integrity verification, and signal integrity analysis to guarantee the design meets all performance specifications. It completes physical verification including DRC, LVS, and antenna rule checks to eliminate any layout violations that could cause manufacturing failures or functional issues. The process generates the final GDSII database and manufacturing files that are tape-out ready for mask creation and silicon fabrication if shorts DRCs results from power planning stage which require modification in power planning script which commented ignore DRCs as shown in fig 2.17 .

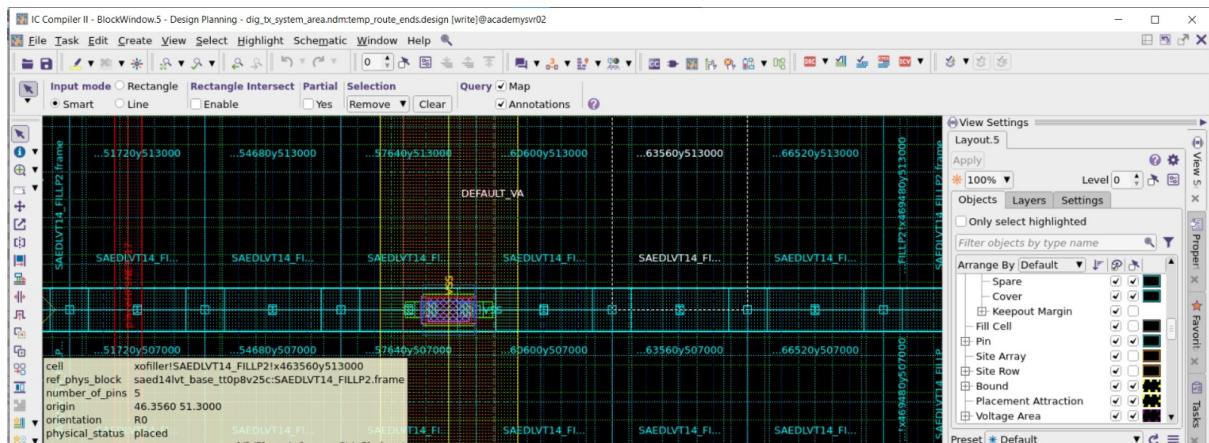


Figure 2.16: chip finishing for Area

```
compile_pg -strategies RING
#-ignore_drc
```

Figure 2.17: Modification in power plan for DRCs

```
connect_pg_net -automatic

remove_stdcell_fillers_with_violation
```

Figure 2.18: Modification in chip finishing script for DRCs fix

```
=====
Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.
=====
Total number of input nets is 3755.
Total number of short violations is 20.
Total number of open nets is 0.
Total number of floating route violations is 0.

Elapsed = 0:00:02, CPU = 0:00:02
1
```

Figure 2.19: DRCs Before fix

```
=====
Maximum number of violations is set to 1000
Abort checking when more than 1000 violations are found
All violations might not be found.
=====
Total number of input nets is 3747.
Total number of short violations is 0.
Total number of open nets is 1.
Open nets are VDD
Total number of floating route violations is 0.

Elapsed = 0:00:02, CPU = 0:00:02
1
```

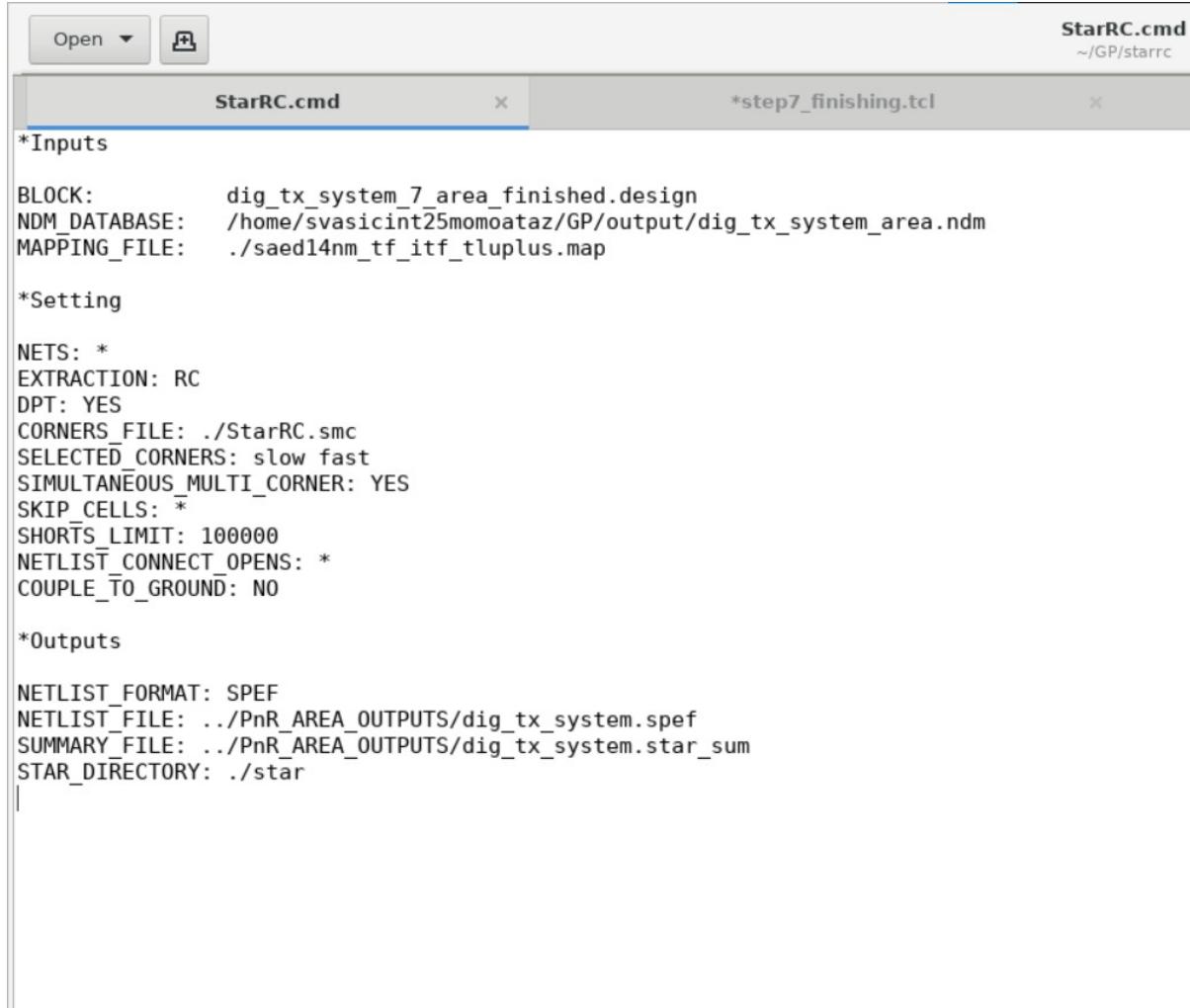
Figure 2.20: DRCs After fix

2.9 StarRC and Prime Time

The goal of StarRC is to perform accurate parasitic extraction by analyzing the physical layout and generating precise resistance, capacitance, and inductance models for all interconnects in the design. StarRC creates detailed parasitic networks that capture real silicon behavior including coupling effects, process variations, and advanced technology node characteristics for timing and signal integrity analysis. It generates SPEF files containing parasitic information that accurately represents the electrical behavior of routed wires, vias, and device parasitics for downstream tools. The tool ensures timing closure by providing highly accurate delay models that account for crosstalk, noise effects, and process corner variations throughout the design.

The goal of PrimeTime is to perform comprehensive static timing analysis using the parasitic data from extraction tools to verify that the design meets all timing constraints across all operating conditions. PrimeTime analyzes setup and hold timing requirements, clock domain crossings, and timing exceptions to ensure proper functionality at target frequencies and voltages. It performs signoff-quality timing verification that accounts for process variations, temperature

effects, and voltage drops to guarantee silicon success. The tool identifies critical paths, timing violations, and provides detailed reports for design optimization while ensuring the final design achieves timing closure for manufacturing release. We use it in my design to solve reg2reg setup and hold violations as it required the whole methods I used for fixing saved in loggg.log.



The screenshot shows the StarRC.cmd application window. The title bar indicates the current file is "StarRC.cmd" and the tab bar shows "step7_finishing.tcl". The main area displays the configuration script:

```
StarRC.cmd
~/GP/starrc

StarRC.cmd *step7_finishing.tcl

*Inputs
BLOCK: dig_tx_system_7_area_finished.design
NDM_DATABASE: /home/svasicint25momoataz/GP/output/dig_tx_system_area.ndm
MAPPING_FILE: ./saed14nm_tf_itf_tluplus.map

*Setting
NETS: *
EXTRACTION: RC
DPT: YES
CORNERS_FILE: ./StarRC.smc
SELECTED_CORNERS: slow fast
SIMULTANEOUS_MULTI_CORNER: YES
SKIP_CELLS: *
SHORTS_LIMIT: 100000
NETLIST_CONNECT_OPENS: *
COUPLE_TO_GROUND: NO

*Outputs
NETLIST_FORMAT: SPEF
NETLIST_FILE: ../PnR_AREA_OUTPUTS/dig_tx_system.spef
SUMMARY_FILE: ../PnR_AREA_OUTPUTS/dig_tx_system.star_sum
STAR_DIRECTORY: ./star
```

Figure 2.21: StarRC Area setup

The screenshot shows a terminal window titled "global_timing_before_fix_44.log". The report details the following information:

```

*****
Report : global_timing
    -format { narrow }
Design : dig_tx_system
Version: W-2024.09-SP5
Date   : Wed Aug 20 19:41:07 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-5.787	0.000	-0.090	-5.787	-5.178
TNS	-75.659	0.000	-1.824	-68.657	-5.178
NUM	42	0	27	14	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.033	-0.033	0.000	0.000	0.000
TNS	-0.381	-0.381	0.000	0.000	0.000
NUM	36	36	0	0	0

1

Figure 2.22: Area Global time before applying eco fix

```

pt_shell> insert_buffer -new_cell_names "clk_buf_captur4e14" -new_net_names "clk_net_d33elayed14" [get_pins u_dig_tx_asyn_fifo_write/fifom/fifo_reg[1][5]/0 ] [get_lib_cells */SAEDLVT14_BUF_1]
Information: Removing HyperScale Annotations from pin for buffer insertion. Annotations won't be re-added if the buffer is removed later
Warning: HyperScale annotation at pin u_dig_tx_asyn_fifo_write/fifom/fifo_reg[1][5]/D is not removed because it is not connected to driving port. (NED-079)
Information: Invalidating logical update. (PTE-139)
Information: Invalidating logical update. (PTE-139)
Information: Inserted 'clk_buf_captur4e14' at 'u_dig_tx_asyn_fifo_write/fifom/fifo_reg[1][5]/0' with 'saedl4lvt_base_tt0p8v25c/SAEDLVT14_BUF_1'. (NED-046)
{"u_dig_tx_asyn_fifo_write/fifom/clk_buf_captur4e14"}
nt _clock~_connect+timing ..delay+time_min_max pathno 5

```

Figure 2.23: Applying insert buffer to hold fixing

remove_cell

NAME
SYNTAX
ARGUMENTS
DESCRIPTION
EXAMPLES
SEE ALSO

NAME

remove_cells

Removes the specified cell instances.

SYNTAX

```
integer remove_cells
  [-design design]
  [-force]
  [cells]
  [-all]
```

Data Types

<i>design</i>	collection
<i>cells</i>	collection

Figure 2.24: remove cell to setup fixing

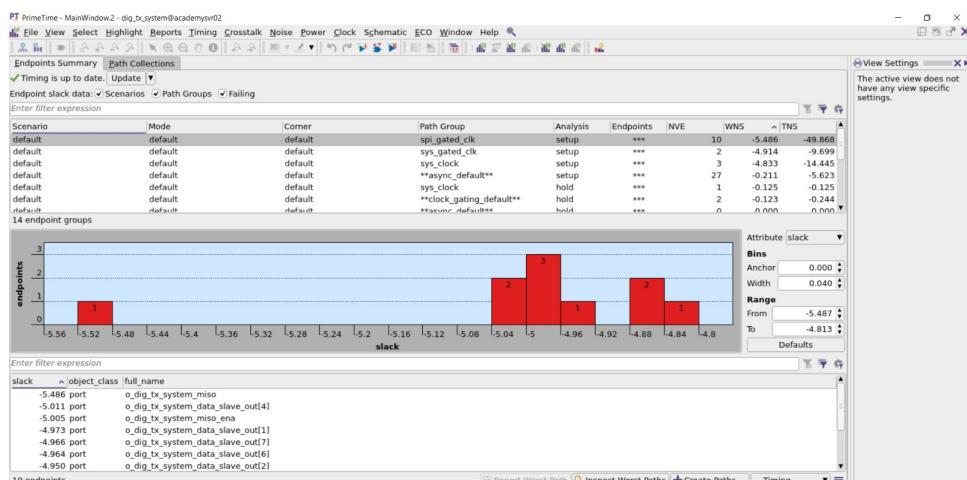


Figure 2.25: Histogram before fix

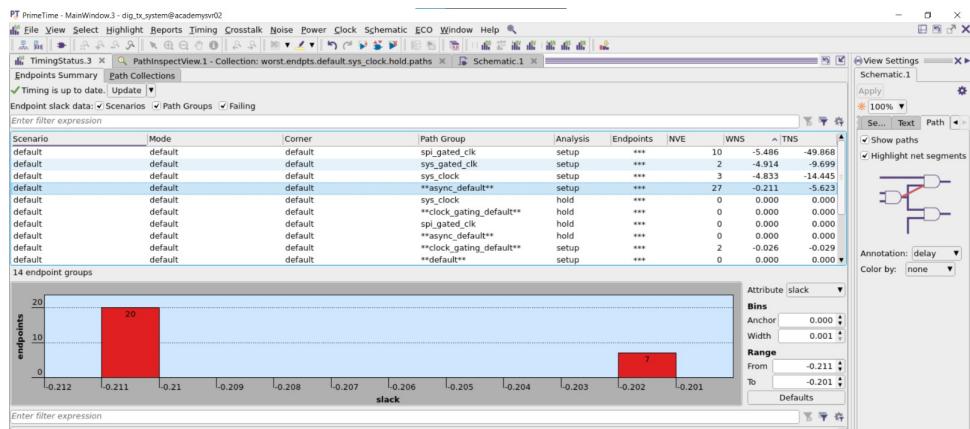


Figure 2.26: Histogram after fix

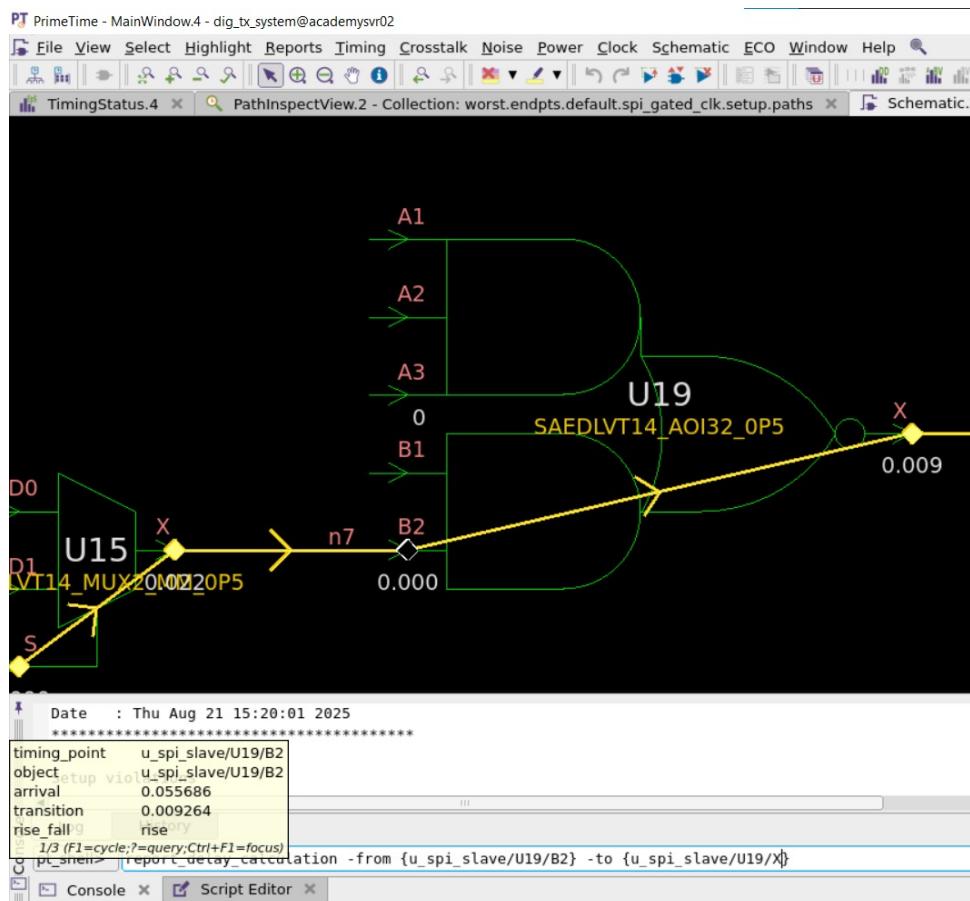


Figure 2.27: Area delay calculation

```
Open  area_delay_calculation
      ~/GP/sta
*pt.tcl  area_delay_calculation  global_timing_before_area_fix_44.log
*****
Report : delay_calculation
Design : dig_tx_system
Version: W-2024.09-SP5
Date   : Thu Aug 21 15:34:17 2025
*****  
  
From pin: u_spi_slave/U19/B2
To pin:   u_spi_slave/U19/X
Main Library Units: 1ns 1pF 1kOhm  
  
Library: 'saed14lvt_base_tt0p8v25c'
Library Units: 1ns 1pF 1kOhm
Library Cell: 'SAEDLVT14_A0I32_0P5'
arc sense:           negative_unate
arc type:            cell  
  
RC network on pin 'u_spi_slave/U19/X' :
-----  
Number of elements = 7 Capacitances + 6 Resistances
Total capacitance = 0.002593 pF
Total capacitance = 0.002593 (in library unit)
Total resistance  = 0.011039 Kohm  
  
          Rise      Fall
-----  
Input transition time = 0.009264    0.009338 (in library unit)
Effective capacitance = 0.002593    0.002593 (in pF)
Effective capacitance = 0.002593    0.002593 (in library unit)
Drive resistance       = 0.001000    0.001000 (in Kohm)
Output transition time = 0.034870    0.014299 (in library unit)
Cell delay             = 0.032203    0.009221 (in library unit)  
  
From pin: u_spi_slave/U19/B2
To pin:   u_spi_slave/U19/X
Main Library Units: 1ns 1pF 1kOhm
```

Figure 2.28: Delay calculation report .jpeg

2.10 Note

All the reports generating from compile for Area in this path and netlist in work directory

```
" /home/svasicint25momoataz/GP/PnR_AREA_OUTPUTS "
```

Figure 2.29: Area outputs

```
/home/svasicint25momoataz/GP/output/dig_tx_system_area.ndm
```

Figure 2.30: Nmd Area location

```
## reporting and output
report_timing > ../../output/${DESIGN_NAME}_timing_area_reports.log
report_qor > ../../output/${DESIGN_NAME}_qor_area_reports.log
report_area -hierarchy > ../../output/${DESIGN_NAME}_area_area_reports.log
report_power -hierarchy > ../../output/${DESIGN_NAME}_power_area_reports.log
```

Figure 2.31: Synthesis outputs for area and its location

```
[svasicint25momoataz@academysvr02 work2]$ pwd
/home/svasicint25momoataz/GP/work2
```

Figure 2.32: work directory for area

Chapter 3

PnR Flow Using Compile for Power

3.1 Compiling

The command optimizes the synthesis process with a focus on power efficiency. Medium mapping effort ensures a balanced approach to resource allocation. Disabling area effort allows the tool to ignore size constraints. High power effort may include advanced techniques like clock gating. This configuration suits designs where energy savings outweigh area concerns.

```
compile -map_effort medium -area_effort none -power_effort high
```

Figure 3.1: compile for power

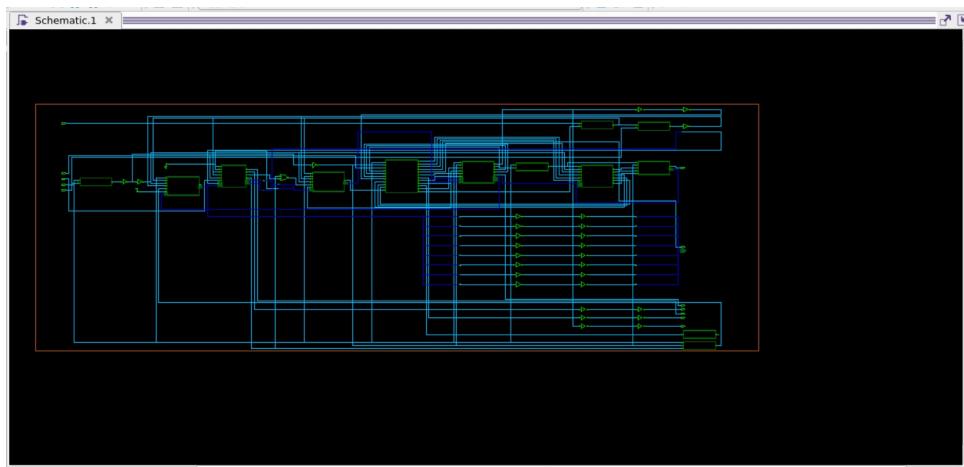


Figure 3.2: compile for power schematic

Area

```
-----  
Combinational Area: 1015.472399  
Noncombinational Area: 393.828003  
Buf/Inv Area: 343.078800  
Total Buffer Area: 163.26  
Total Inverter Area: 179.82  
Macro/Black Box Area: 0.000000  
Net Area: 1049.401049  
-----  
Cell Area: 1409.300402  
Design Area: 2458.701451
```

Design Rules

```
-----  
Total Number of Nets: 1808  
Nets With Violations: 15  
Max Trans Violations: 15  
Max Cap Violations: 15  
-----
```

| Hostname: academysvr02

Compile CPU Statistics

```
-----  
Resource Sharing: 0.83  
Logic Optimization: 7.55  
Mapping Optimization: 5.86  
-----  
Overall Compile Time: 32.62  
Overall Compile Wall Clock Time: 34.23  
-----
```

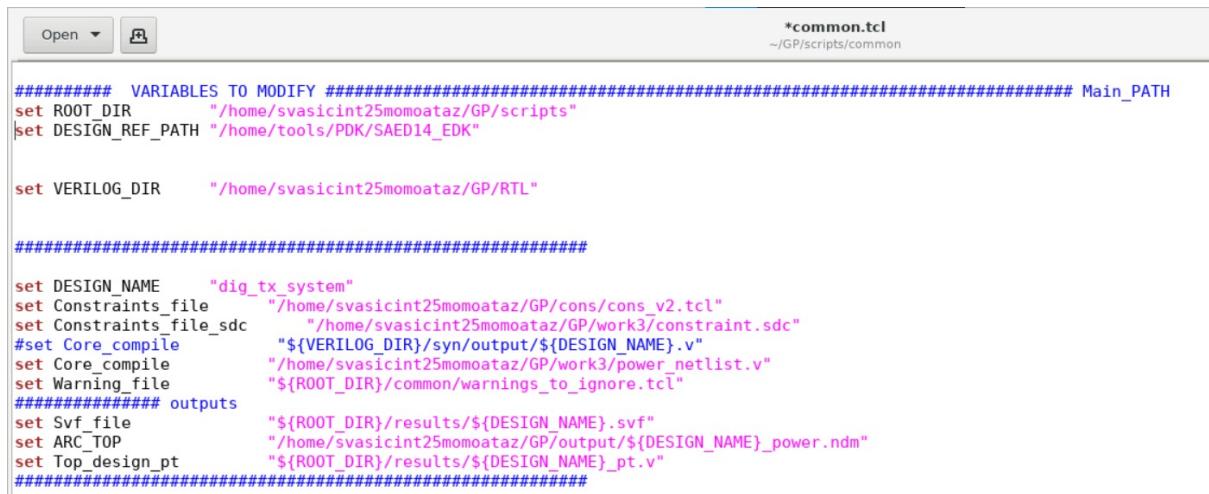
Design WNS: 6.29 TNS: 86.33 Number of Violating Paths: 44

Design (Hold) WNS: 0.13 TNS: 28.80 Number of Violating Paths: 352

Figure 3.3: compile for power QoR report

3.2 Setup Data

Data Setup goal Import the synthesized gate-level netlist from Design Compiler into the PnR tool database. Load all timing constraints, power requirements, and physical design rules from SDC constraint files. Configure the chip floorplan by defining the core area, I/O pad placement, and positioning of hard macros like memories. Set up technology libraries including LEF files for cell abstracts, DEF files for routing layers, and technology rules for the target process node. Initialize power grid specifications and clock tree requirements for the design. Verify all imported data for consistency and completeness before starting placement. Create the initial PnR database with all design information properly configured and ready for the physical implementation flow



```

Open  *common.tcl
~/GP/scripts/common

#####
# VARIABLES TO MODIFY #####
#####
set ROOT_DIR      "/home/svasicint25momoataz/GP/scripts"
set DESIGN_REF_PATH "/home/tools/PDK/SAED14_EDK"

set VERILOG_DIR    "/home/svasicint25momoataz/GP/RTL"

#####
# DESIGN NAME #####
set DESIGN_NAME      "dig_tx_system"
set Constraints_file  "/home/svasicint25momoataz/GP/cons/cons_v2.tcl"
set Constraints_file_sdc  "/home/svasicint25momoataz/GP/work3/constraint.sdc"
#set Core_compile     "${VERILOG_DIR}/syn/output/${DESIGN_NAME}.v"
set Core_compile     "/home/svasicint25momoataz/GP/work3/power_netlist.v"
set Warning_file     "${ROOT_DIR}/common/warnings_to_ignore.tcl"
#####
# OUTPUTS #####
set Svf_file        "${ROOT_DIR}/results/${DESIGN_NAME}.svf"
set ARC_TOP          "/home/svasicint25momoataz/GP/output/${DESIGN_NAME}_power.ndm"
set Top_design_pt   "${ROOT_DIR}/results/${DESIGN_NAME}_pt.v"
#####

```

Figure 3.4: Modification in common.tcl for power

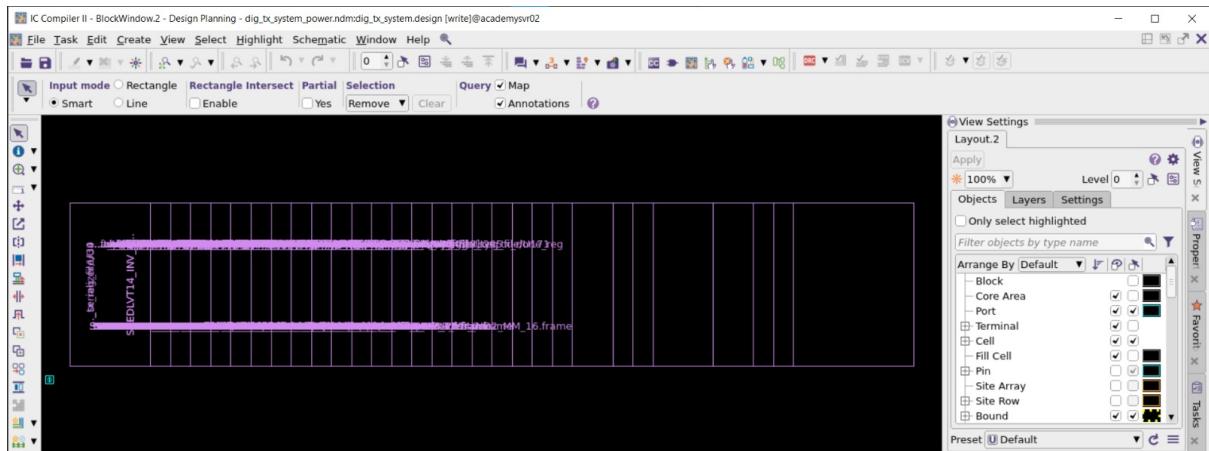


Figure 3.5: compile for power QoR report

3.3 Floor Plan

Create the chip floorplan by defining the core area dimensions and aspect ratio for optimal die size. Position hard macros like memories, analog blocks, and IP cores to minimize routing congestion and timing issues. Place I/O pads around the chip periphery based on package constraints and signal groupings. Define power domains and voltage islands with proper isolation and level shifter placement. Plan the power grid structure with power rings, stripes, and via connections for adequate current delivery. Establish placement blockages and routing channels to guide tool optimization. Set up clock domains and plan clock tree entry points for balanced distribution. Create initial pin assignments and bus routing corridors for critical nets. Verify floorplan constraints meet timing, power, and manufacturability requirements before proceeding to placement

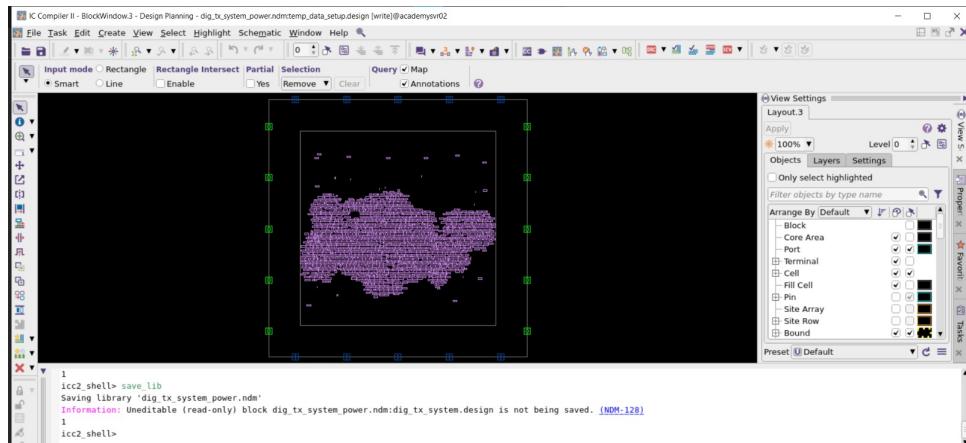


Figure 3.6: Floorplanning for power

3.4 Power Plan

Goal Plan power grid topology with power rings around the core and macro blocks for reliable current distribution. Create vertical and horizontal power stripes across the chip to minimize voltage drop and IR drop violations. Define multiple power domains and voltage islands with proper isolation cells and level shifters for power management. Position power pads strategically around the chip periphery based on current density and package constraints. Design dedicated power networks for analog blocks, PLLs, and sensitive circuits to minimize noise coupling. Plan power switches and retention registers for power gating and low-power modes. Calculate power grid resistance and ensure adequate metal width for expected current loads. Create power intent files and UPF constraints for multi-voltage domain verification. Establish power analysis checkpoints for static and dynamic power consumption validation. Verify electromigration rules and current density limits are met across all power networks. .

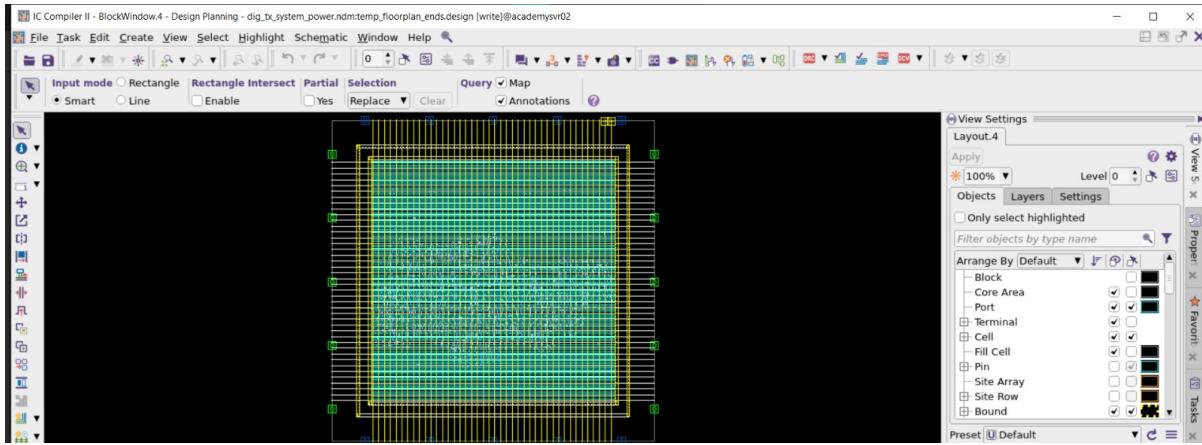


Figure 3.7: power planning for power

3.5 Placement

Place standard cells from the netlist into rows within the core area while respecting floorplan constraints and blockages. Position cells to minimize total wirelength and reduce routing congestion in critical areas. Optimize placement for timing closure by clustering timing-critical paths and reducing delays on critical nets. Balance cell density across the chip to avoid hotspots and ensure adequate routing resources. Apply placement constraints for clock cells, scan chains, and special function blocks. Perform legalization to ensure cells are properly aligned to placement sites and meet design rule requirements. Optimize power delivery by considering IR drop and placing high-current cells near power sources. Minimize crosstalk and noise by appropriate spacing of sensitive analog and digital circuits. Iterate placement refinement with timing analysis feedback to meet setup and hold time requirements. Verify placement quality through congestion analysis and timing reports before proceeding to clock tree synthesis.

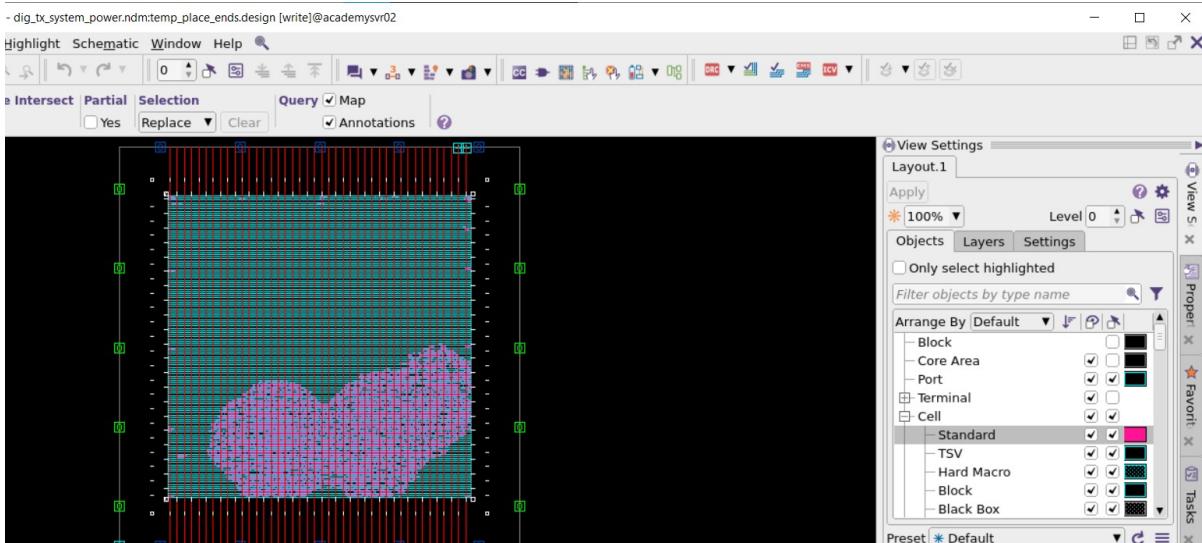


Figure 3.8: placement for power

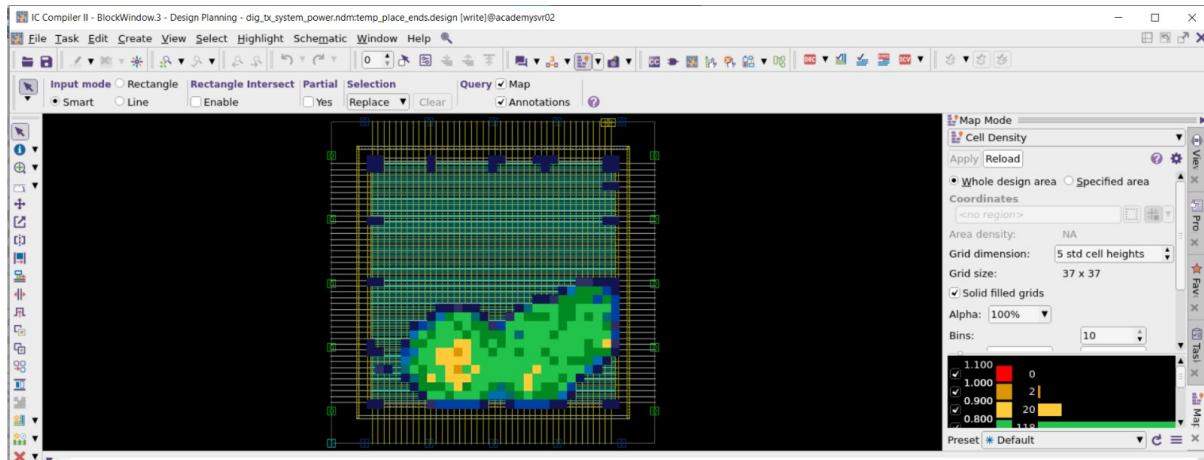


Figure 3.9: power cell denisty

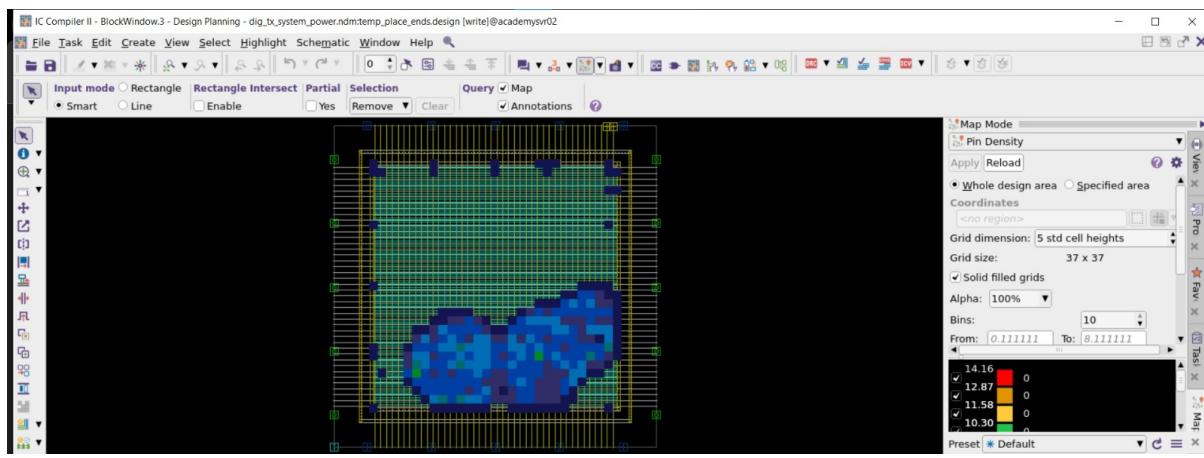


Figure 3.10: power pin denisty

```
*****
Report : global timing
    -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Mon Aug 18 17:07:47 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-6.876	0.000	-0.056	-6.876	-6.126
TNS	-92.067	0.000	-0.864	-85.077	-6.126
NUM	42	0	27	14	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.163	-0.163	0.000	0.000	0.000
TNS	-39.062	-39.062	0.000	0.000	0.000
NUM	366	366	0	0	0

1

Figure 3.11: power placement global timing

3.6 CTS

CTS goal Analyze clock domains and identify all clock sinks including flip-flops, latches, and memory elements throughout the design. Construct clock tree topology using buffers and inverters to distribute clock signals from source to all endpoints. Balance clock tree branches to minimize skew between different paths and ensure synchronous operation across the design. Size clock buffers appropriately to handle capacitive loads and maintain sharp clock edges with minimal jitter. Insert clock gates for power optimization and ensure proper enable signal timing for dynamic power management. Optimize clock tree for minimal insertion delay while meeting skew targets across process, voltage, and temperature variations. Route clock nets on dedicated low-resistance metal layers to minimize noise coupling and crosstalk effects. Perform useful skew optimization to improve timing closure by intentionally skewing clocks on non-critical paths. Validate clock tree quality through skew analysis, insertion delay reports, and power consumption verification. Generate final clock constraints and timing exceptions for subsequent routing and timing closure phases.

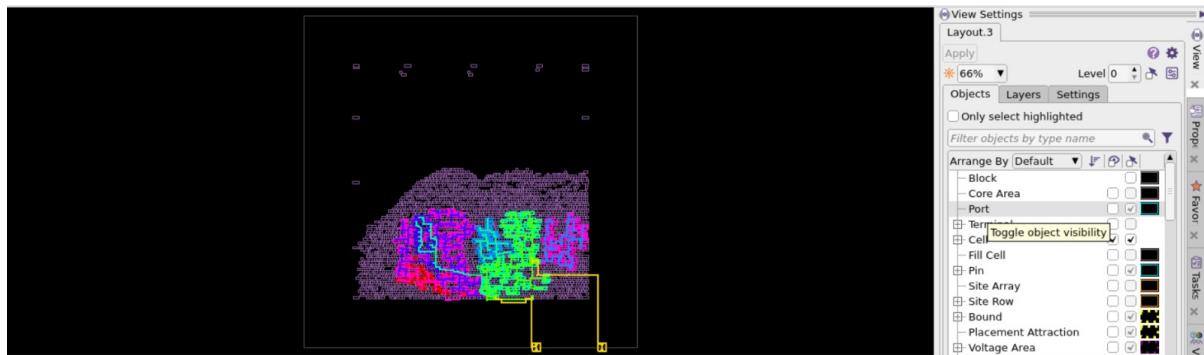


Figure 3.12: power CTS Highlight

```
*****
Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Mon Aug 18 17:18:03 2025
*****
```

Setup violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-7.481	0.000	-0.191	-7.481	-6.421
TNS	-97.192	0.000	-5.136	-85.635	-6.421
NUM	42	0	27	14	1

Hold violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.139	-0.139	0.000	0.000	0.000
TNS	-0.392	-0.392	0.000	0.000	0.000
NUM	9	9	0	0	0

1

Figure 3.13: Power CTS global timing

3.7 Routing

Goal of Route route all signal nets from placement using available metal layers while respecting technology design rules and spacing requirements. Create global routing plan to distribute nets across different metal layers and minimize congestion in critical areas. Perform detailed routing to complete all connections with proper via placement and wire sizing for signal integrity. Optimize routing for timing closure by prioritizing critical nets and minimizing delays on setup-critical paths. Route power and ground networks with adequate width to handle current density and minimize IR drop violations. Implement clock routing on dedicated layers with shielding to reduce crosstalk and maintain signal quality. Route special nets including scan chains, test structures, and analog signals with appropriate constraints and isolation. Resolve design rule violations including minimum spacing, via enclosure, and metal density requirements across all layers. Perform post-route optimization including wire sizing, buffer insertion, and rerouting to fix timing and signal integrity issues. Validate final routing through DRC checks, LVS verification, and timing sign-off analysis before tapeout preparation.

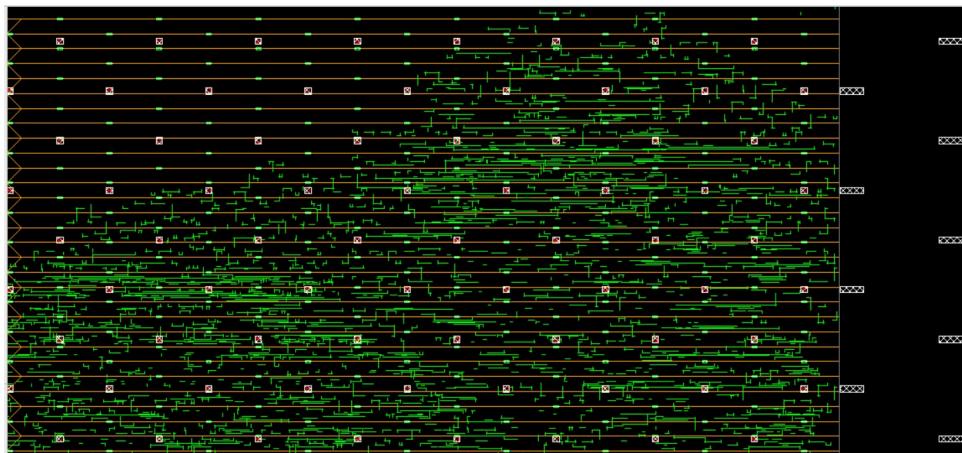


Figure 3.14: power routing

```
*****
Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Mon Aug 18 17:28:14 2025
*****
```

Setup violations				
	Total	reg->reg	in->reg	reg->out
WNS	-7.428	-0.001	-0.207	-7.428
TNS	-96.803	-0.001	-5.572	-84.888
NUM	43	1	27	14

Hold violations				
	Total	reg->reg	in->reg	reg->out
WNS	-0.123	-0.123	0.000	0.000
TNS	-0.382	-0.382	0.000	0.000
NUM	23	23	0	0

1

Figure 3.15: Power routing global timing

3.8 Chip Finishing

Chip Finishing coal Add metal fill patterns across all layers to meet foundry density requirements and improve manufacturing yield. Insert decoupling capacitors throughout the design to reduce power supply noise and improve signal integrity. Complete antenna rule fixes by adding diodes or jumpers to protect gates from plasma charging damage during fabrication. Perform comprehensive design rule checking (DRC) to ensure all geometric and spacing requirements are met for the target process. Execute layout versus schematic (LVS) verification to confirm the physical implementation matches the original netlist connectivity. Run electrical rule checking (ERC) to validate power connections, floating nets, and proper device operation. Generate final GDSII database with all layers, cells, and manufacturing data properly formatted for foundry submission. Create comprehensive timing sign-off reports including setup, hold, and transition time analysis across all operating conditions. Prepare manufacturing documentation including pin maps, power specifications, and test requirements for packaging and assembly. Perform final quality checks and obtain design team sign-off before releasing the database for mask generation and fabrication.

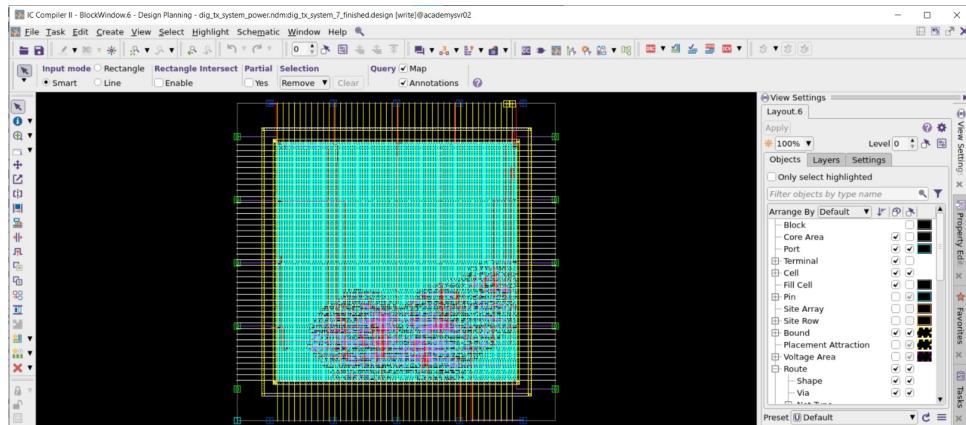


Figure 3.16: power chip finishing

```
[Check Net] All nets are submitted.
[Check Net] 100% Elapsed = 0:00:03, CPU = 0:00:03
Information: Detected open violation for Net VDD. BBox: (0.0000 0.0000)(110.9160 110.4000). (RT-585)

=====
Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.

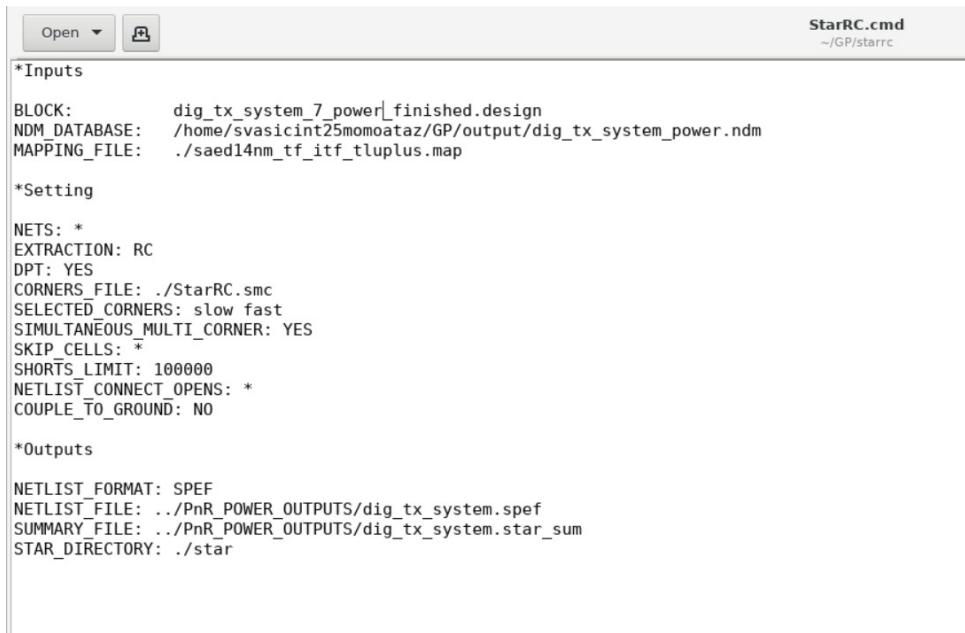
=====
Total number of input nets is 3838.
Total number of short violations is 0.
Total number of open nets is 1.
Open nets are VDD
Total number of floating route violations is 0.

Elapsed = 0:00:03, CPU = 0:00:03
1
```

Figure 3.17: power drc fix

3.9 StarRC and Prime Time

The goal of StarRC is to perform accurate parasitic extraction by analyzing the physical layout and generating precise resistance, capacitance, and inductance models for all interconnects in the design. StarRC creates detailed parasitic networks that capture real silicon behavior including coupling effects, process variations, and advanced technology node characteristics for timing and signal integrity analysis. It generates SPEF files containing parasitic information that accurately represents the electrical behavior of routed wires, vias, and device parasitics for downstream tools. The tool ensures timing closure by providing highly accurate delay models that account for crosstalk, noise effects, and process corner variations throughout the design. The goal of PrimeTime is to perform comprehensive static timing analysis using the parasitic data from extraction tools to verify that the design meets all timing constraints across all operating conditions. PrimeTime analyzes setup and hold timing requirements, clock domain crossings, and timing exceptions to ensure proper functionality at target frequencies and voltages. It performs signoff-quality timing verification that accounts for process variations, temperature effects, and voltage drops to guarantee silicon success. The tool identifies critical paths, timing violations, and provides detailed reports for design optimization while ensuring the final design achieves timing closure for manufacturing release. We use it in my design to solve reg2reg setup and hold violations as it required.



```

StarRC.cmd
~/GP/starrc

*Inputs
BLOCK: dig_tx_system_7_power_finished.design
NDM_DATABASE: /home/svasicint25momoataz/GP/output/dig_tx_system_power.ndm
MAPPING_FILE: ./saed14nm_tf_itf_tluplus.map

*Setting
NETS: *
EXTRACTION: RC
DPT: YES
CORNERS_FILE: ./StarRC.smc
SELECTED_CORNERS: slow fast
SIMULTANEOUS_MULTI_CORNER: YES
SKIP_CELLS: *
SHORTS_LIMIT: 100000
NETLIST_CONNECT_OPENS: *
COUPLE_TO_GROUND: NO

*Outputs
NETLIST_FORMAT: SPEF
NETLIST_FILE: ../PnR_POWER_OUTPUTS/dig_tx_system.spef
SUMMARY_FILE: ../PnR_POWER_OUTPUTS/dig_tx_system.star_sum
STAR_DIRECTORY: ./star

```

Figure 3.18: StarRC power setup

The file “/home/svasicint25momoata..._timing_after_fix_125.log” changed on disk.

```
*****
Report : global_timing
      -format { narrow }
Design : dig_tx_system
Version: W-2024.09-SP5
Date   : Mon Aug 18 19:01:48 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-5.709	0.000	-0.206	-5.709	-5.234
TNS	-79.844	0.000	-5.556	-69.054	-5.234
NUM	42	0	27	14	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.123	-0.123	0.000	0.000	0.000
TNS	-0.819	-0.819	0.000	0.000	0.000
NUM	53	53	0	0	0

1

Figure 3.19: Global timing before fix eco

```

pvasicnt25momoatacademymsv02~/GP/sta
File Edit View Search Terminal Help
clock network delay (ideal) 0.00 0.00
u_dig_tx_serializer/o_dig_tx_serializer_shr_crc_done_reg/CK (SAEDLVT14_FDPRBQ_V2LP_0P5)
0.00 0.00 r
u_dig_tx_serializer/o_dig_tx_serializer_shr_crc_done_reg/0 (SAEDLVT14_FDPRBQ_V2LP_0P5)
0.03 & 0.03 f
u_dig_tx_control_unit/U52/X (SAEDLVT14_INV_0P5) 0.01 & 0.04 r
u_dig_tx_control_unit/U12/X (SAEDLVT14_OAI22_0P5) 0.02 & 0.07 r
u_dig_tx_control_unit/U29/X (SAEDLVT14_OR4_1) 0.02 & 0.08 f
u_dig_tx_control_unit/clockcopt_h_inst_6576/X (SAEDLVT14_DEL_R2V2_1)
0.02 & 0.11 f
u_dig_tx_control_unit/clockcopt_h_inst_6578/X (SAEDLVT14_DEL_R2V3_1)
0.03 & 0.13 f
u_dig_tx_control_unit/clockcopt_h_inst_6577/X (SAEDLVT14_DEL_R2V3_1)
0.02 & 0.15 f
u_dig_tx_control_unit/clockropt_h_inst_7878/X (SAEDLVT14_BUF_UCDC_0P5)
0.01 & 0.16 f
u_dig_tx_control_unit/current_state_reg[0]/D (SAEDLVT14_FDPRBQ_V2_2)
0.00 & 0.16 f
data arrival time 0.16

clock sys_clock (rise edge) 0.00 0.00
clock network delay (ideal) 0.00 0.00
u_dig_tx_control_unit/current_state_reg[0]/CK (SAEDLVT14_FDPRBQ_V2_2)
0.00 r
clock reconvergence pessimism 0.00 0.00
clock uncertainty 0.15 0.15
library hold time 0.01 0.16
data required time 0.16
-----
data required time 0.16
data arrival time -0.16
-----
slack (VIOLATED: increase significant digits) -0.00

```

Figure 3.20: insert buffer fixing method

```
pt_shell> report_global_timing
*****
Report : global_timing
      -format { narrow }
Design : dig_tx_system
Version: W-2024.09-SP5
Date   : Mon Aug 18 19:20:09 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-5.71	0.00	-0.21	-5.71	-5.23
TNS	-79.84	0.00	-5.56	-69.05	-5.23
NUM	42	0	27	14	1

No hold violations found.

1

Figure 3.21: Global timing After fixing

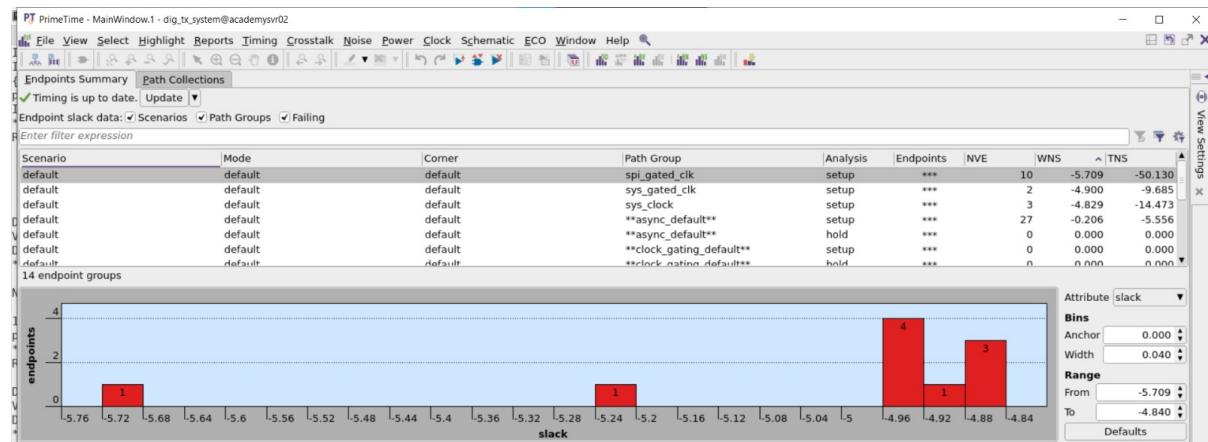


Figure 3.22: Histogram AFTER FIX

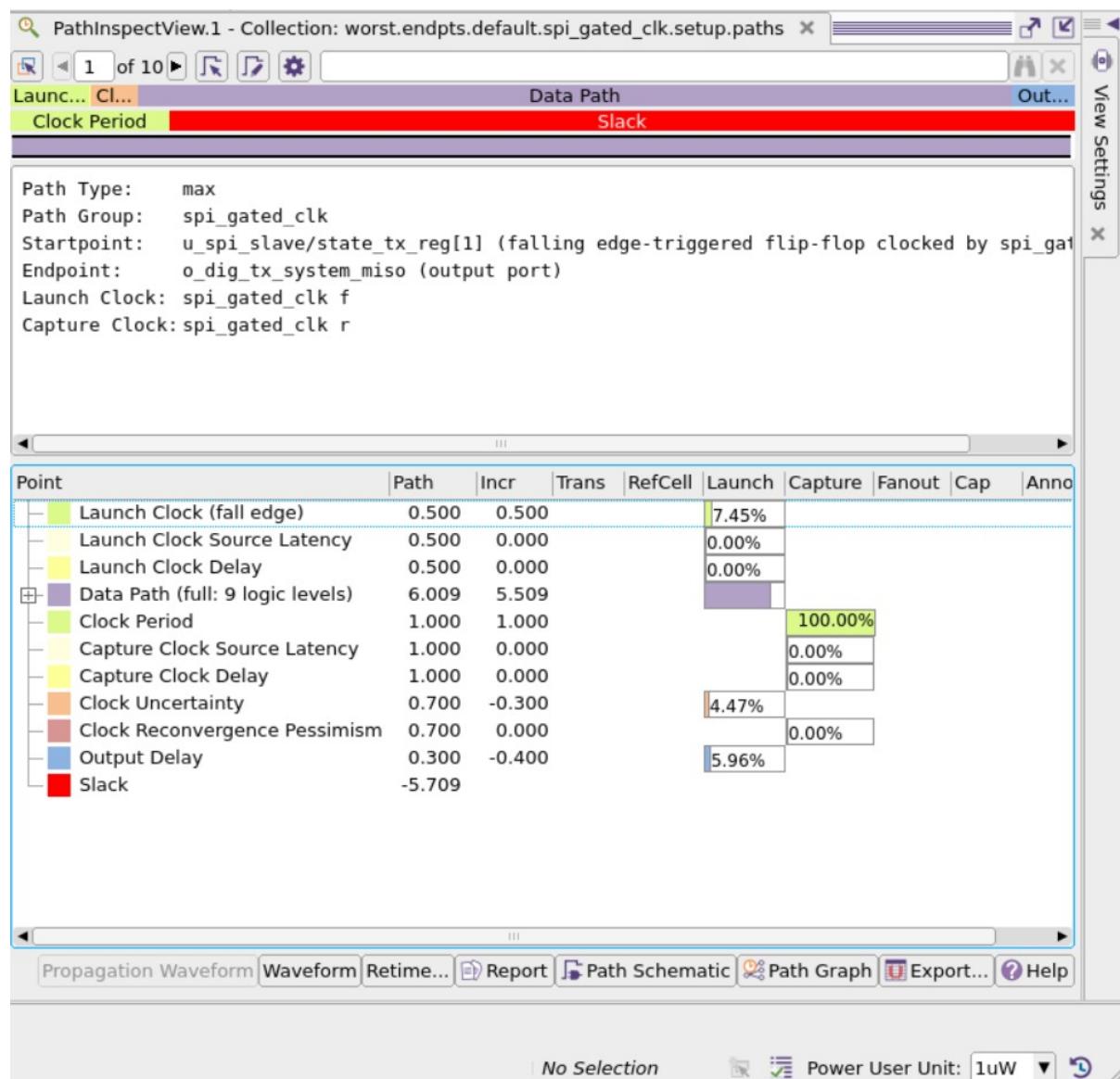


Figure 3.23: POWER inspect worst path

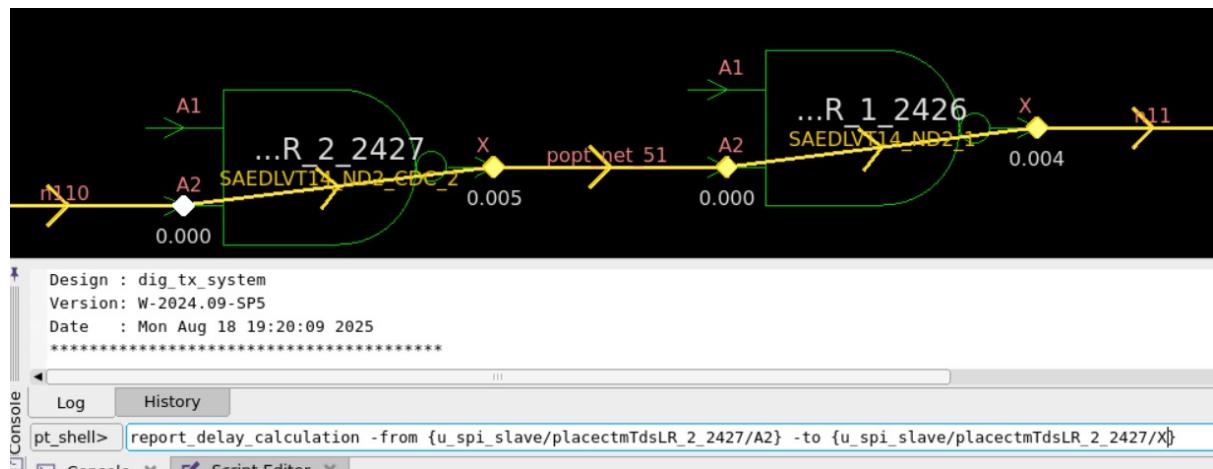


Figure 3.24: schematic delay calculation

```
pt_shell> report_delay_calculation -from {u_spi_slave/placectmTdsLR_2_2427/A2} -to {u_spi_slave/placectmTdsLR_2_2427/X}
*****
Report : delay_calculation
Design : dig_tx_system
Version: W-2024.09-SP5
Date : Mon Aug 18 19:27:14 2025
*****  
  

From pin: u_spi_slave/placectmTdsLR_2_2427/A2
To pin: u_spi_slave/placectmTdsLR_2_2427/X
Main Library Units: 1ns 1pF 1kOhm  
  

Library: 'saed14lvt_base_tt0p8v25c'
Library Units: 1ns 1pF 1kOhm
Library Cell: 'SAEDLVT14_ND2_CDC_2'
arc sense: negative_unate
arc type: cell  
  

RC network on pin 'u_spi_slave/placectmTdsLR_2_2427/X' :
-----  

Number of elements = 5 Capacitances + 4 Resistances
Total capacitance = 0.001503 pF
Total capacitance = 0.001503 (in library unit)
Total resistance = 0.011677 Kohm  
  

Rise Fall
-----  

Input transition time = 0.006206 0.005754 (in library unit)
Effective capacitance = 0.001503 0.001503 (in pF)
Effective capacitance = 0.001503 0.001503 (in library unit)
Drive resistance = 0.001000 0.001000 (in Kohm)
Output transition time = 0.003983 0.005439 (in library unit)
Cell delay = 0.004551 0.005305 (in library unit)  
  

From pin: u_spi_slave/placectmTdsLR_2_2427/A2
To pin: u_spi_slave/placectmTdsLR_2_2427/X
Main Library Units: 1ns 1pF 1kOhm  
  

Library: 'saed14lvt_base_tt0p8v25c'
Library Units: 1ns 1pF 1kOhm
Library Cell: 'SAEDLVT14_ND2_CDC_2'
arc sense: negative_unate
arc SDF condition: A1==1'b1
```

Figure 3.25: Report delay calculation

3.10 Note

All the reports generating from compile for power in this path nd netlist in work directory

```
"./home/svasicint25momoataz/GP/PnR_POWER_OUTPUTS"
```

Figure 3.26: Power outputs location

```
/home/svasicint25momoataz/GP/output/dig_tx_system_power.ndm
```

Figure 3.27: POWER NDM location

```
## reporting and output
report_timing > ./output/${DESIGN_NAME}_timing_power_reports.log
report_qor > ./output/${DESIGN_NAME}_qor_power_reports.log
report_area -hierarchy > ./output/${DESIGN_NAME}_area_power_reports.log
report_power -hierarchy > ./output/${DESIGN_NAME}_power_power_reports.log
```

Figure 3.28: synthesis outputs for power and its location

```
[svasicint25momoataz@academysvr02 work3]$ pwd
/home/svasicint25momoataz/GP/work3
```

Figure 3.29: work directory for power