Report on Parasitic Extraction using StarRC

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1 Introduction

This report details the process of performing Parasitic Extraction using StarRC and subsequent timing analysis using PrimeTime. The objective is to evaluate the design's timing performance, identify the worst path timing, and apply engineering change order (ECO) fixes to optimize the design. The report includes screenshots of scripts, timing reports, and ECO changes, along with global timing updates after each modification step.

2 Report Overview

The report should include the following steps:

1. After running Parasitic Extraction using StarRC, add screenshots of your script and Report Message Summary

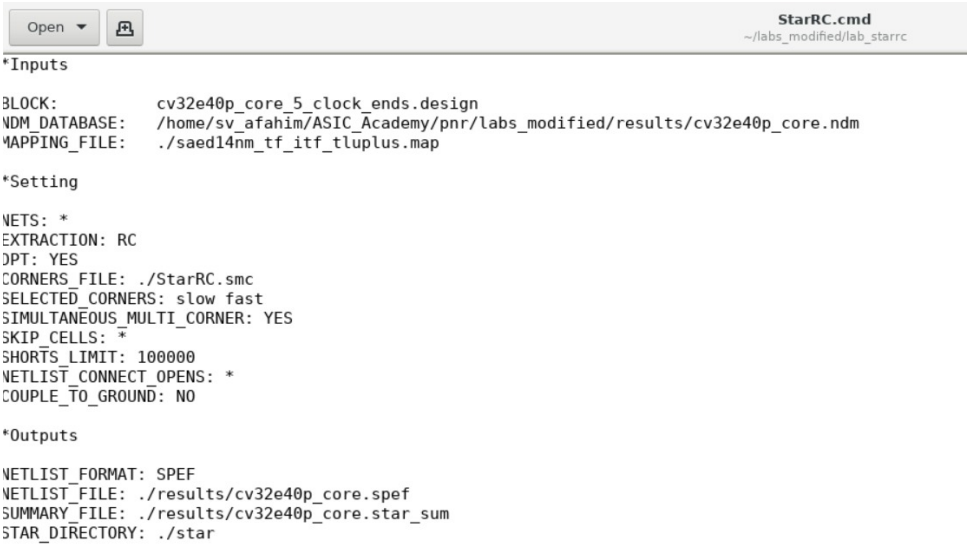

Figure 1: StarRC.cmd

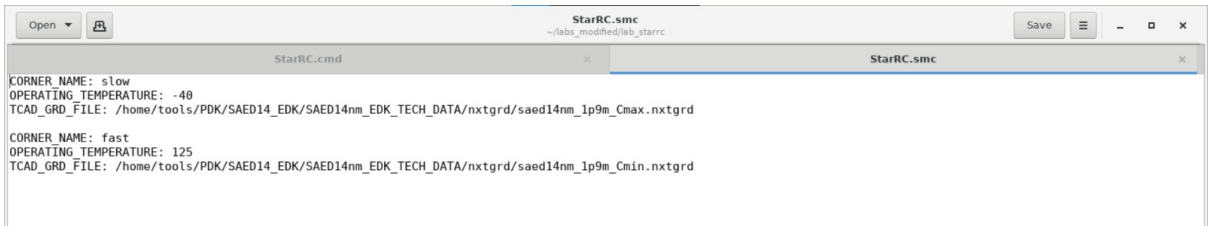

Figure 2: StarRC.smc

```
Startpoint: if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_0_
            (rising edge-triggered flip-flop clocked by clk_i)
Endpoint: if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_1_
            (rising edge-triggered flip-flop clocked by clk_i)
Last common pin: clk_i
Path Group: clk_i
Path Type: min

Point                                                    Incr       Path
-----------------------------------------------------------------------------
clock clk_i (rise edge)                                  0.00       0.00
clock network delay (propagated)                         0.05       0.05
if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_0_/CK (SAEDLVT14_FDPRBQ_V2LP_0P5)
                                                         0.00       0.05 r
if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_0_/Q (SAEDLVT14_FDPRBQ_V2LP_0P5)
                                                         0.05 &     0.10 f
if_stage_i/prefetch_buffer_i/prefetch_controller_i/U250/X (SAEDLVT14_AOI21_0P5)
                                                         0.01 &     0.11 r
if_stage_i/prefetch_buffer_i/prefetch_controller_i/U248/X (SAEDLVT14_OAI22_0P5)
                                                         0.01 &     0.12 f
if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_1_/D (SAEDLVT14_FDPRBQ_V2LP_0P5)
                                                         0.00 &     0.12 f
data arrival time                                                   0.12

clock clk_i (rise edge)                                  0.00       0.00
clock network delay (propagated)                         0.08       0.08
if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_1_/CK (SAEDLVT14_FDPRBQ_V2LP_0P5)
                                                                    0.08 r
clock reconvergence pessimism                            0.00       0.08
inter-clock uncertainty                                  0.20       0.28
library hold time                                        0.02       0.30
data required time                                                  0.30
-----------------------------------------------------------------------------
data required time                                                  0.30
data arrival time                                                  -0.12
-----------------------------------------------------------------------------
slack (VIOLATED)                                                   -0.18
```

Figure 3: worst slack

2. Screenshot of PrimeTime scripts.

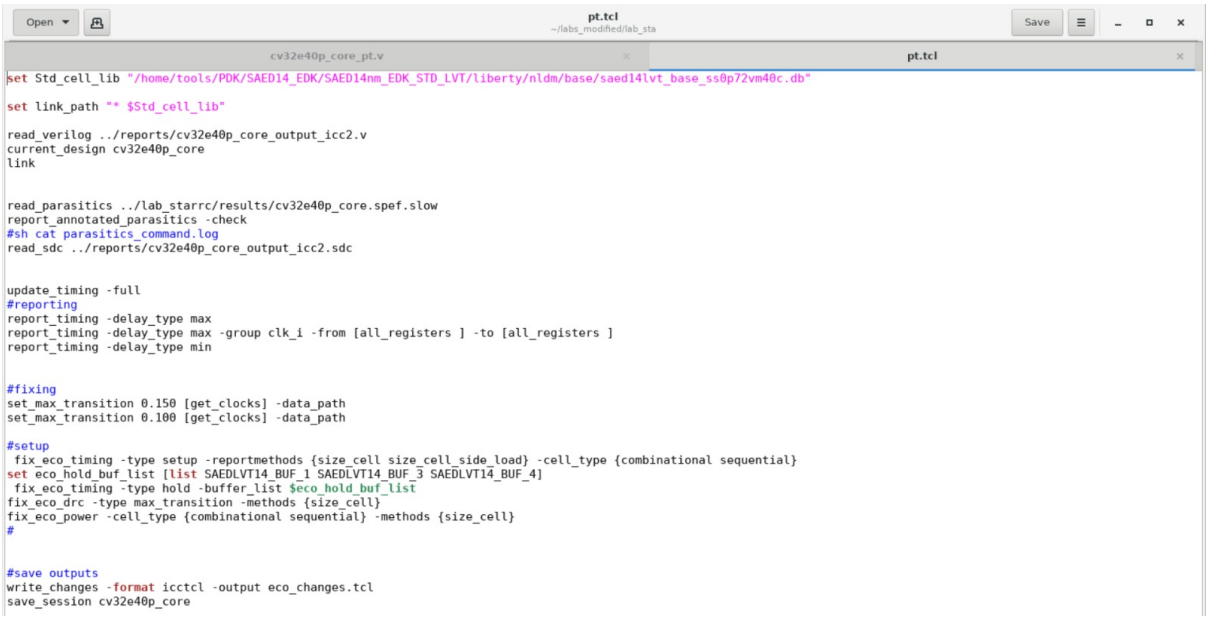

Figure 4: prime time script

3. Worst path timing report.

```
Startpoint: if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_0_
            (rising edge-triggered flip-flop clocked by clk_i)
Endpoint: if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_1_
            (rising edge-triggered flip-flop clocked by clk_i)
Last common pin: clk_i
Path Group: clk_i
Path Type: min

Point                                                    Incr       Path
-----------------------------------------------------------------------------
clock clk_i (rise edge)                                  0.00       0.00
clock network delay (propagated)                         0.05       0.05
if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_0_/CK (SAEDLVT14_FDPRBQ_V2LP_0P5)
                                                         0.00       0.05 r
if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_0_/Q (SAEDLVT14_FDPRBQ_V2LP_0P5)
                                                         0.05 &     0.10 f
if_stage_i/prefetch_buffer_i/prefetch_controller_i/U250/X (SAEDLVT14_AOI21_0P5)
                                                         0.01 &     0.11 r
if_stage_i/prefetch_buffer_i/prefetch_controller_i/U248/X (SAEDLVT14_OAI22_0P5)
                                                         0.01 &     0.12 f
if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_1_/D (SAEDLVT14_FDPRBQ_V2LP_0P5)
                                                         0.00 &     0.12 f
data arrival time                                                   0.12

clock clk_i (rise edge)                                  0.00       0.00
clock network delay (propagated)                         0.08       0.08
if_stage_i/prefetch_buffer_i/prefetch_controller_i/flush_cnt_q_reg_1_/CK (SAEDLVT14_FDPRBQ_V2LP_0P5)
                                                                    0.08 r
clock reconvergence pessimism                            0.00       0.08
inter-clock uncertainty                                  0.20       0.28
library hold time                                        0.02       0.30
data required time                                                  0.30
-----------------------------------------------------------------------------
data required time                                                  0.30
data arrival time                                                  -0.12
-----------------------------------------------------------------------------
slack (VIOLATED)                                                   -0.18
```

Figure 5: worst path

4. Report global timing for the design .

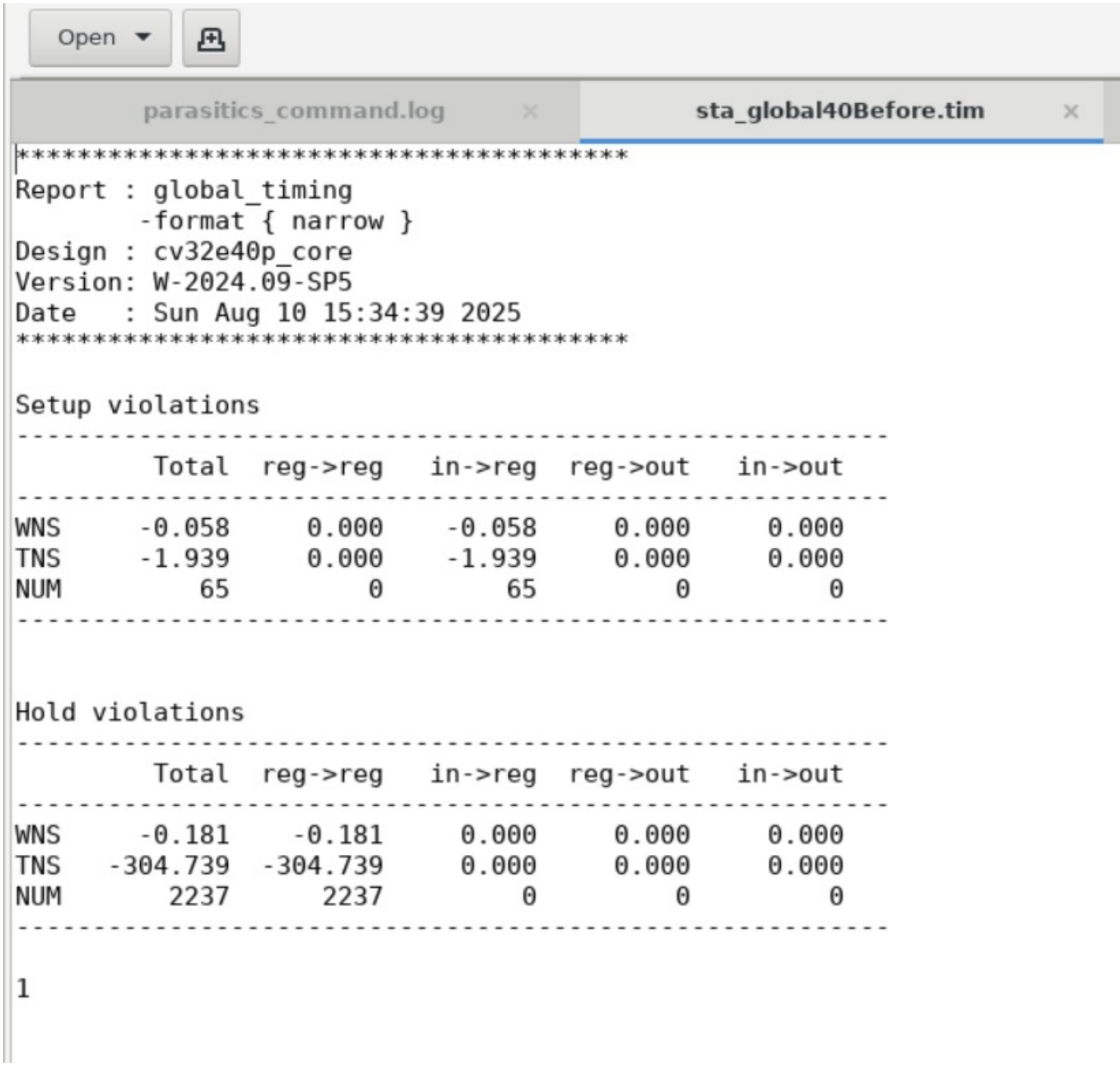

Figure 6: Global time 40 before fix

5. Screenshot of histogram for endpoint Slack for clki group and path inspector for the worst clki path for setup.

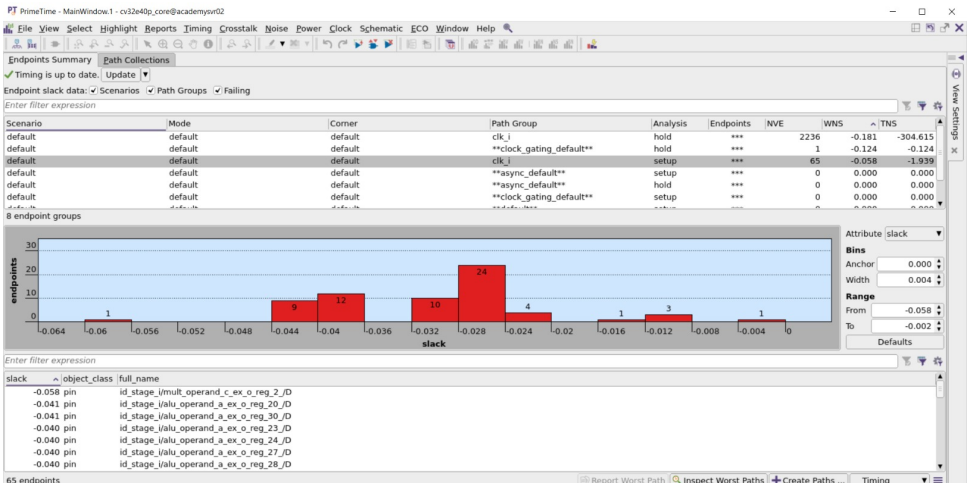

Figure 7: Histogram

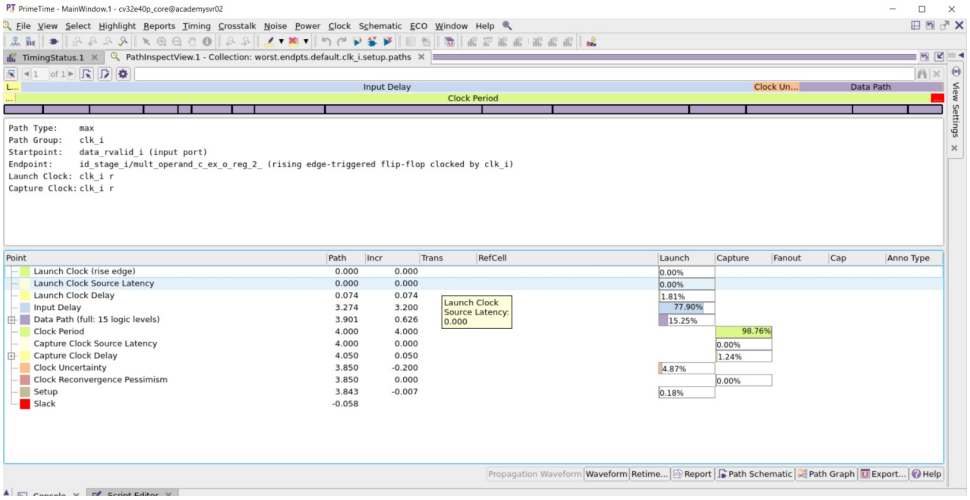

Figure 8: path view

6. report delay calculation of a selected cell from your choice, and include it in your report.

Figure 9: report delay calculation

```
report_delay_calculation -from {load_store_unit_i/placeHFSINV_4585_25/A} -to {load_store_unit_i/placeHFSINV_4585_25/X}
****************************************
Report : delay_calculation
Design : cv32e40p_core
Version: W-2024.09-SP5
Date   : Sun Aug 10 15:45:43 2025
****************************************

From pin: load_store_unit_i/placeHFSINV_4585_25/A
To pin:   load_store_unit_i/placeHFSINV_4585_25/X
Main Library Units:  1ns  1pF  1kOhm

Library: 'saed14lvt_base_ss0p72vm40c'
Library Units:  1ns  1pF  1kOhm
Library Cell: 'SAEDLVT14_INV_S_1P5'
arc sense:                      negative_unate
arc type:                       cell

   RC network on pin 'load_store_unit_i/placeHFSINV_4585_25/X' :
   -----------------------------------------------------
   Number of elements = 170 Capacitances + 203 Resistances
   Total capacitance  = 0.018353 pF
   Total capacitance  = 0.018353 (in library unit)
   Total resistance   = 0.002030 Kohm

                              Rise        Fall
   ---------------------------------------------------------------------
   Input transition time  = 0.000000    0.000000  (in library unit)
   Effective capacitance  = 0.018353    0.018353  (in pF)
   Effective capacitance  = 0.018353    0.018353  (in library unit)
   Drive resistance       = 0.001000    0.001000  (in Kohm)
   Output transition time = 0.036436    0.038257  (in library unit)
   Cell delay             = 0.027603    0.025521  (in library unit)

Information: Defining new variable 'tmp'. (CMD-041)
```

Figure 10: delay calculation report

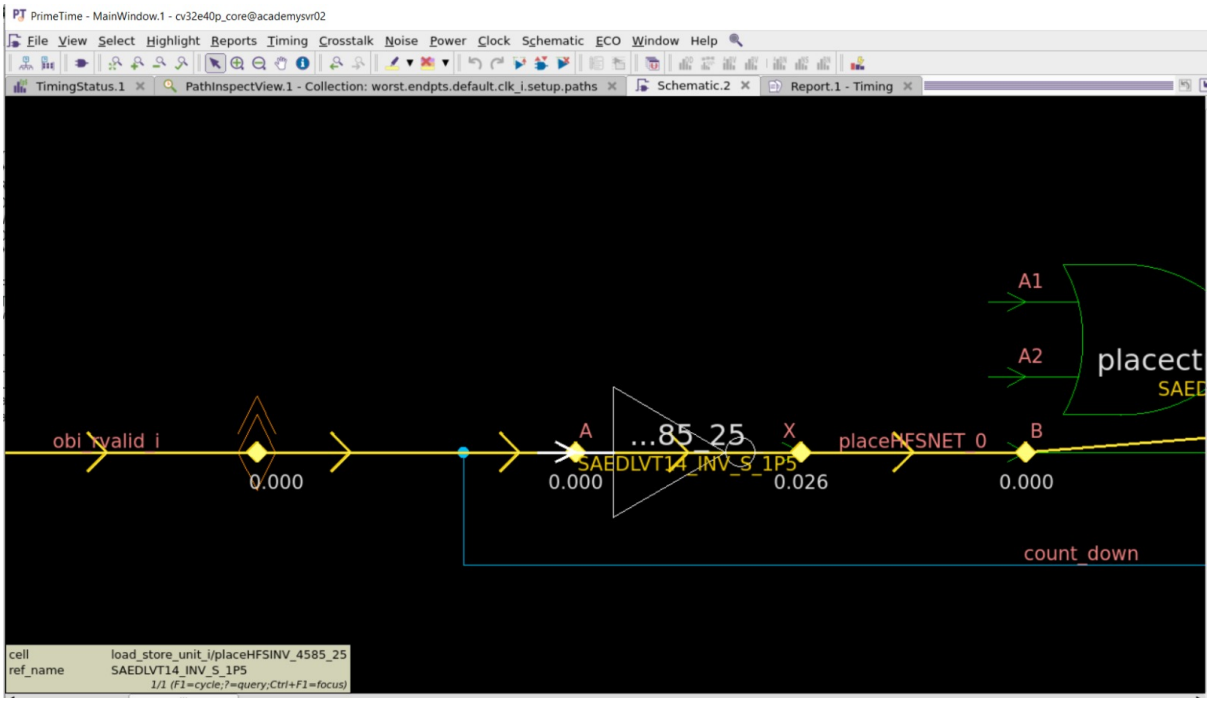

Figure 11: schematic for selected cell

7. Use the fix eco commands provided and report global timing after each step, and add it to your report.

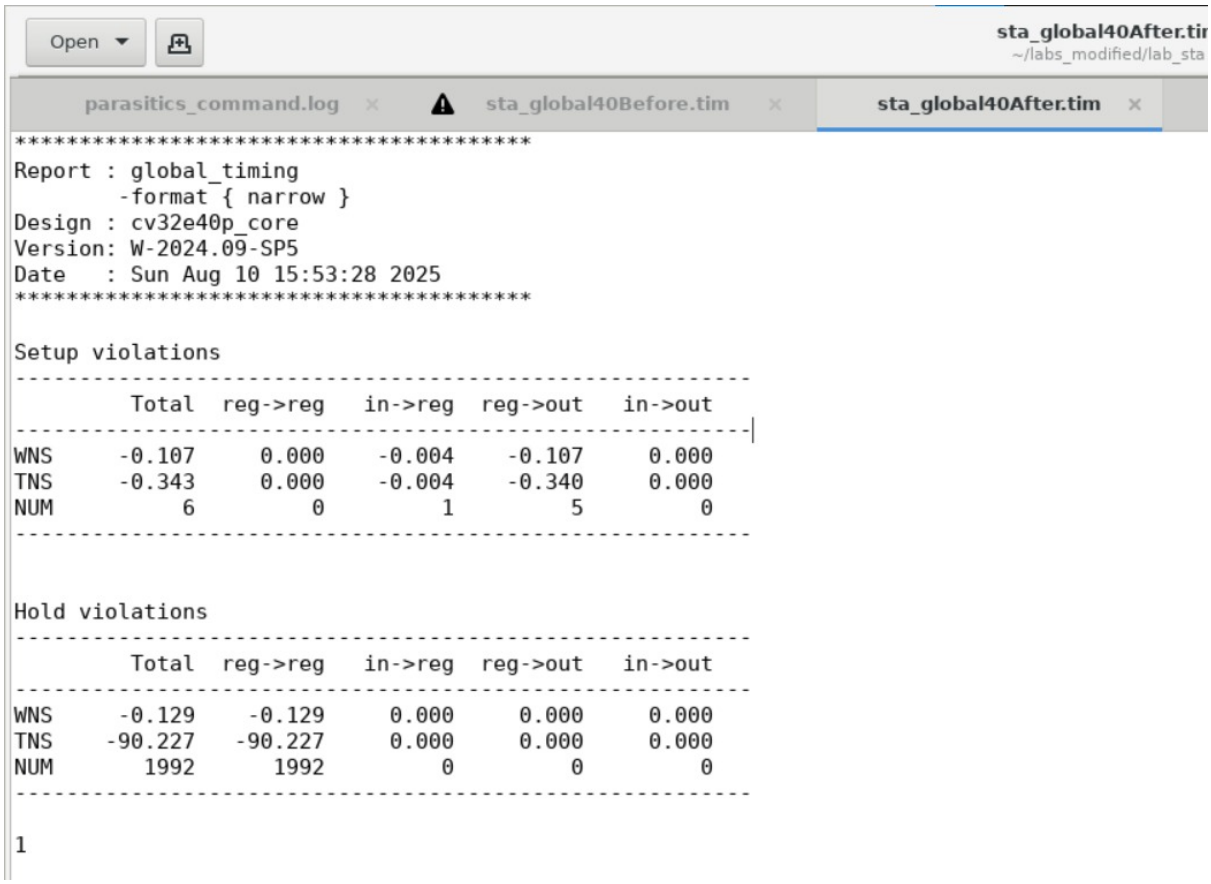

Figure 12: Global time 40 after eco fix

8. After finishing your eco fixing, write your ECO changes and add a screenshot of the file (eco changes.tcl).

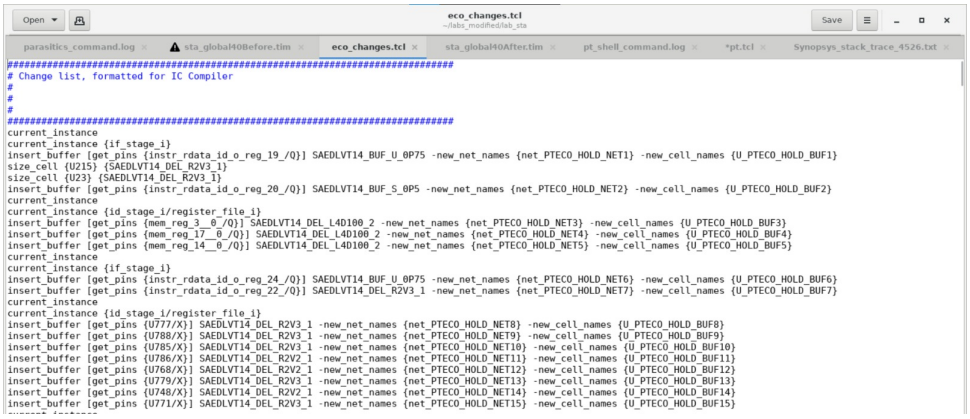

Figure 13: eco changes by insert buffer

```
insert_buffer [get_pins {instr_rdata_id_o_reg_19_/Q}]
size_cell {U215} {SAEDLVT14_DEL_R2V3_1}
size_cell {U23} {SAEDLVT14_DEL_R2V3_1}
```

Figure 14: eco changes by sizing

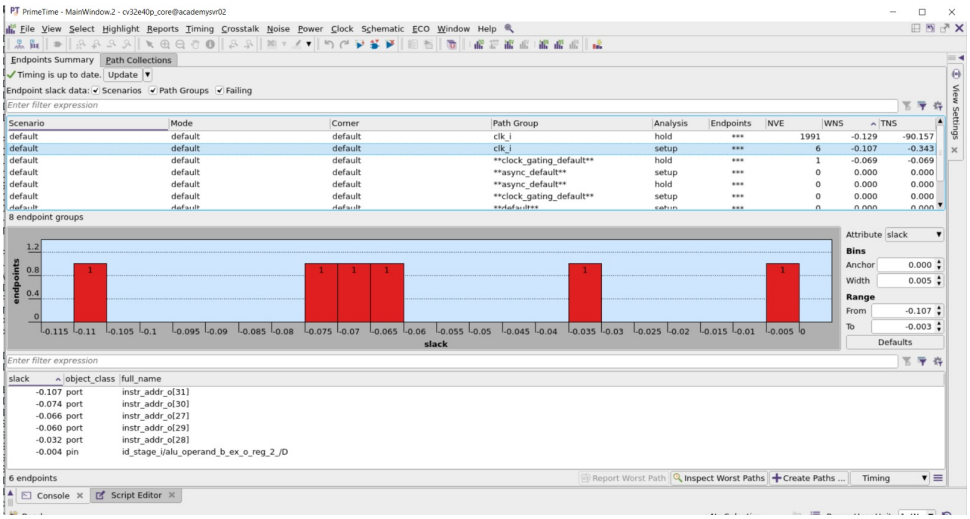

Figure 15: Histogram after fix

9. The past results are in ss0p72vm40c worst for the setup corner, relaunch your run with ff0p88v125c for the worst of hold corner, and update the timing and report the global timing for the corner used, and add it to your report with a screenshot pt script used after modifications.

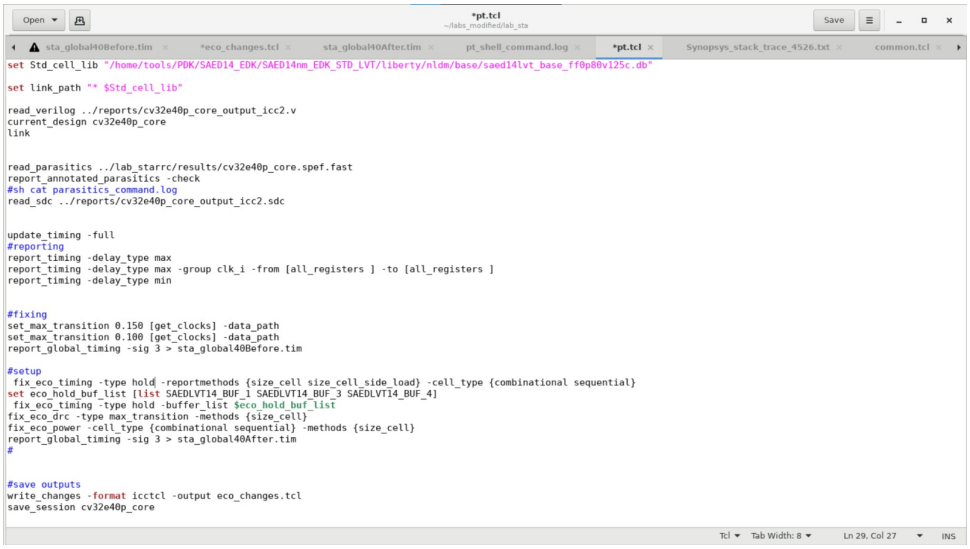

Figure 16: pt after modification

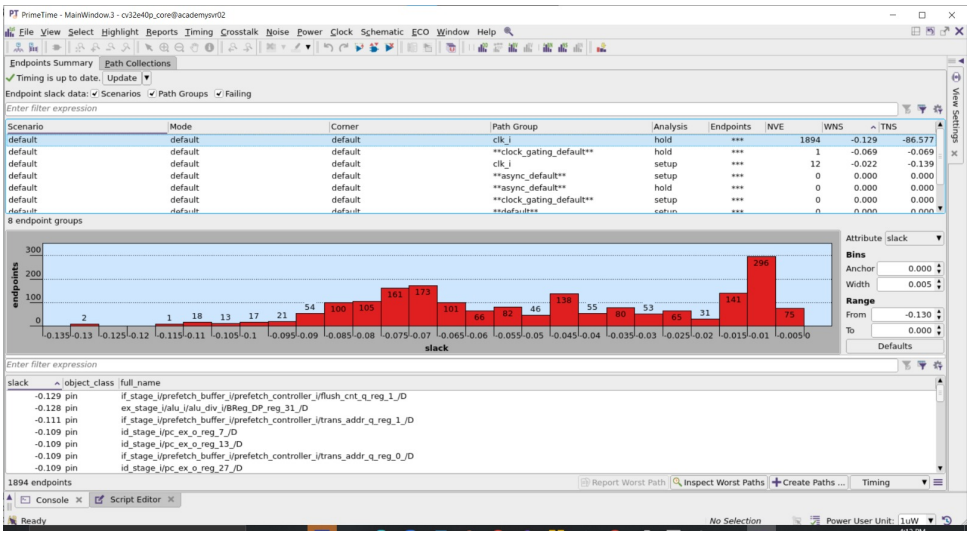

Figure 17: histogram ff

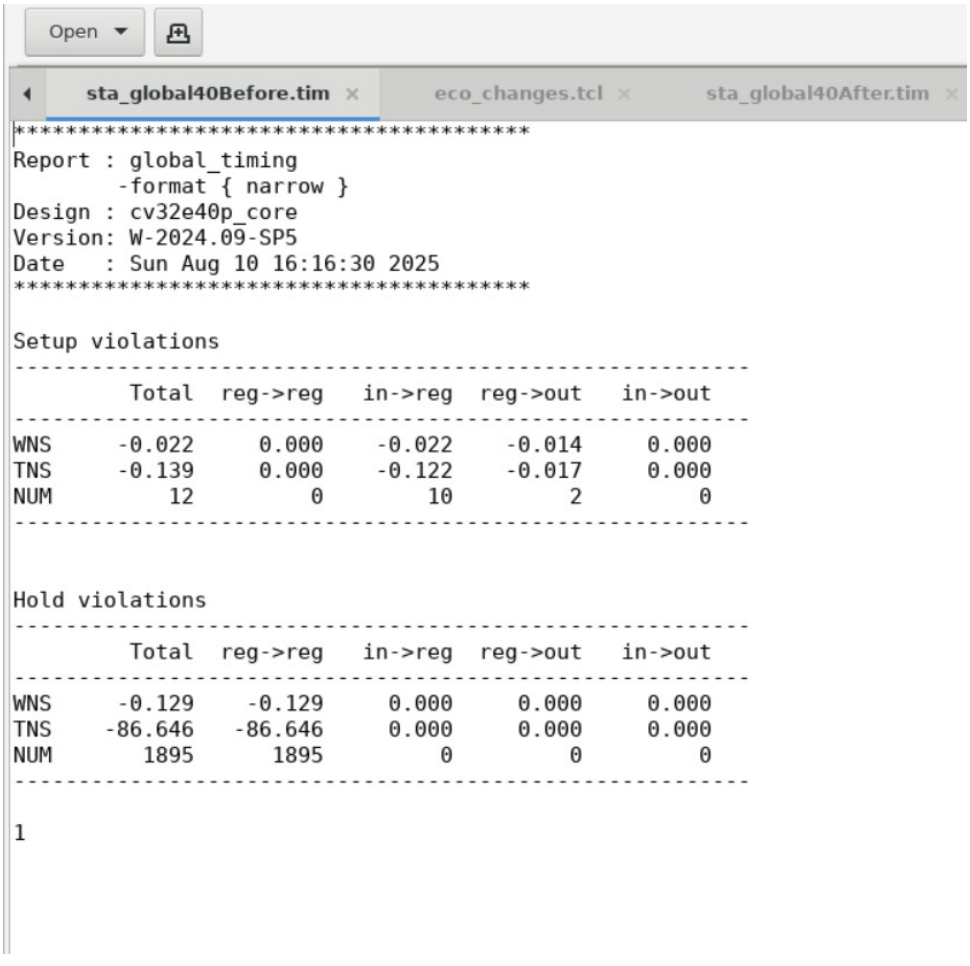

Figure 18: hold global time