COMPUTER ARCHITECTURE

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ELC 303(A)

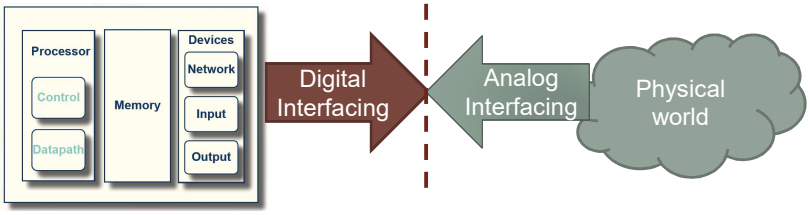
Course Goals

- Learn how to make computer systems go fast
  - Pipelining
  - Caching
  - Prediction
  - Parallelism
- Learn how do different components communicate
  - Within a computer system (interconnection)
  - With the external world (interfacing)

ANALOG/DIGITAL INTERFACING

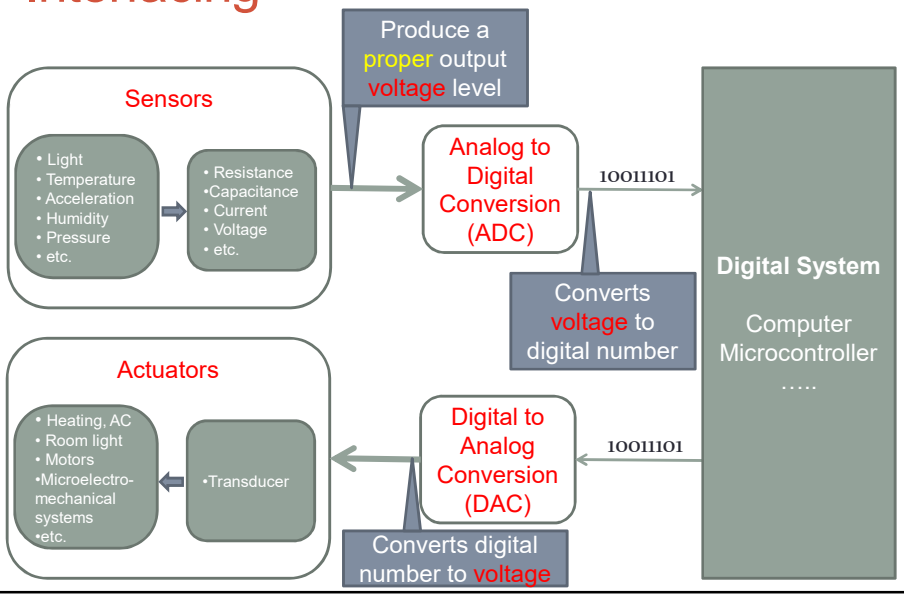
Interfacing

- Both data about the physical world and control signals sent to interact with the physical world are typically "analog" or continuously varying quantities.

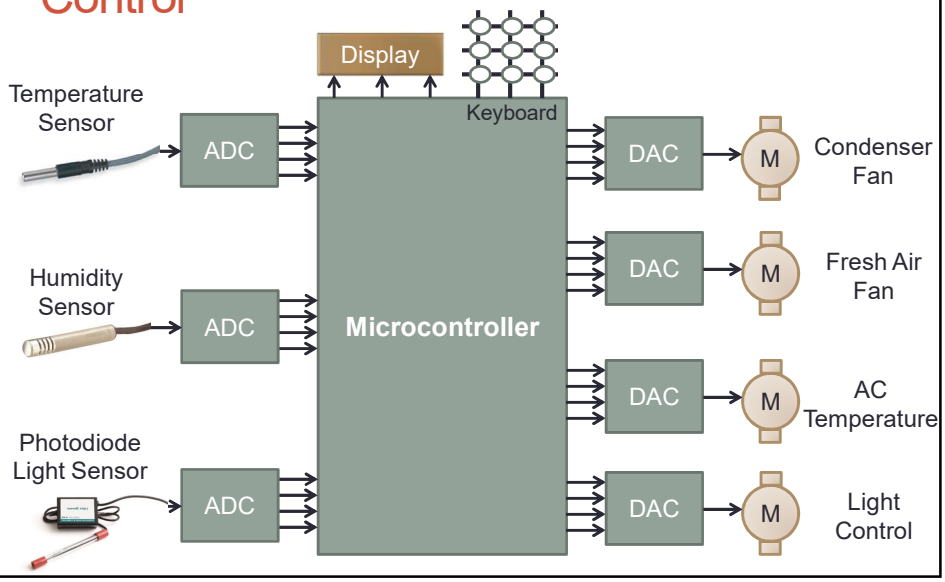


- In order to use the power of digital electronics, one must convert from analog to digital form on the measurement or input end and convert from digital to analog form on the control or output end of a laboratory system.

Interfacing



Example: Autonomous Room Ambient Control



DIGITAL-TO-ANALOG [DAC] INTERFACING

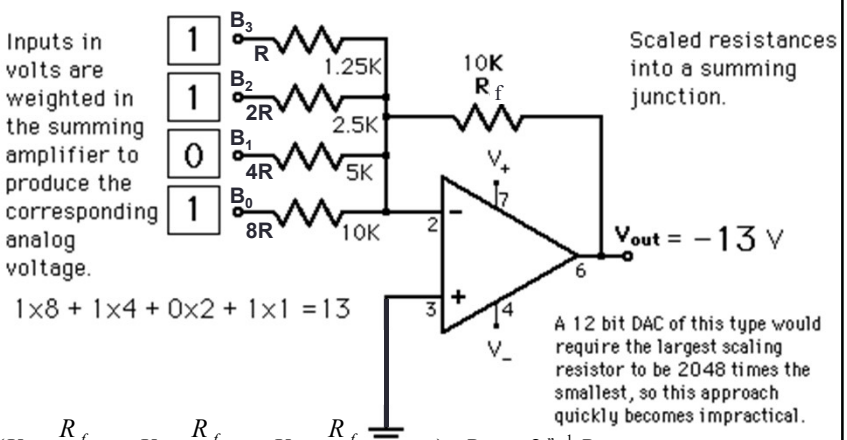
Digital-to-Analog Conversion

- DACs convert a binary number into its equivalent voltage
- DAC applications include digitally controlled gains, motors speed controls, programmable gain amplifiers, etc.

Digital-to-Analog Basic Approaches

- Weighted Summing Amplifier
  - Achieves D/A conversion using a summing amplifier
  - Not satisfactory for a large number of bits because it requires too much precision in the summing resistors
- R-2R Network Approach
  - R-2R network DAC preferable when the number of bits is large

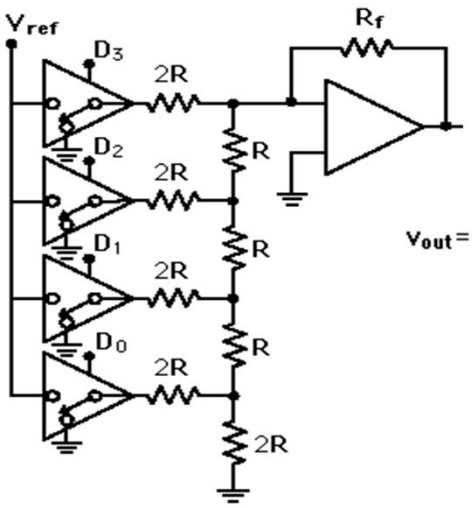
Weighted Sum DAC



$$V_{out} = -\left(V_0 \frac{R_f}{2^{n-1}R} + V_1 \frac{R_f}{2^{n-2}R} + V_2 \frac{R_f}{2^{n-3}R} + \ldots.\right),\ R_f = 2^{n-1}R$$

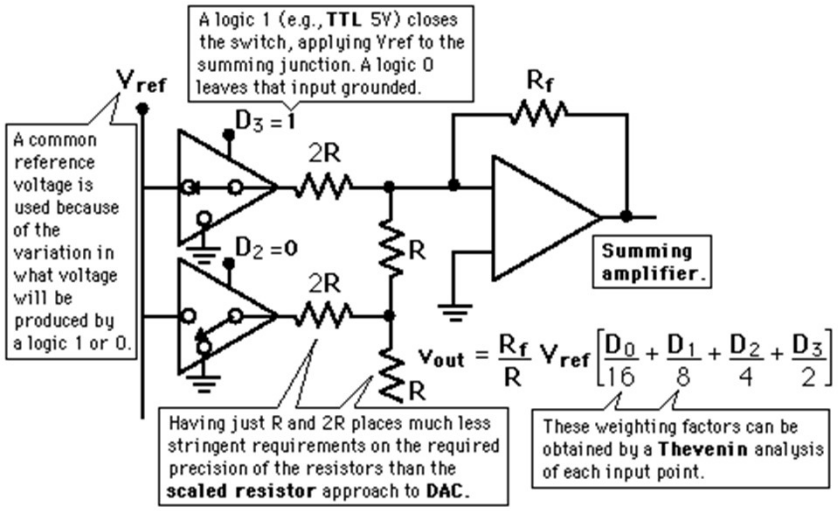
$$\frac{V_{out}}{V_{bit}} = B_0 + 2B_1 + B_2.2^2 + B_3.2^3 + \ldots + B_{n-1}.2^{n-1}$$

R-2R Ladder DAC



$$V_{out} = \frac{R_f}{R} V_{ref} \left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2} \right]$$

R-2R Ladder DAC



$$V_{out} = \frac{R_f}{R} V_{ref} \left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2} \right]$$

R-2R Ladder DAC

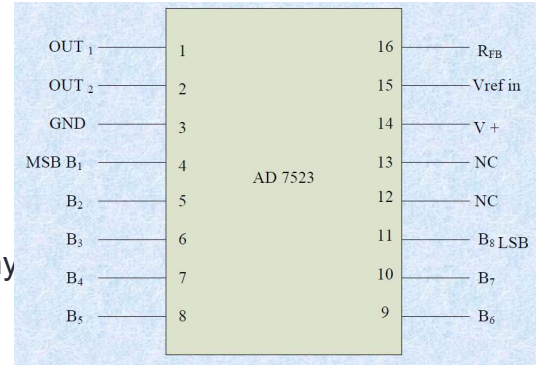
- The summing amplifier with the R-2R ladder of resistances shown produces the output where the D's take the value 0 or 1.
- The digital inputs could be TTL voltages which close the switches on a logical 1 and leave it grounded for a logical 0.
- This is illustrated for 4 bits, but can be extended to any number with just the resistance values R and 2R.

Interfacing Digital to Analog Converters

- **AD 7523 8-bit Multiplying DAC**
  - 16 pin DIP, multiplying DAC, containing R-2R ladder for D-A conversion along with single pole double thrown NMOS switches to connect the digital inputs to the ladder.

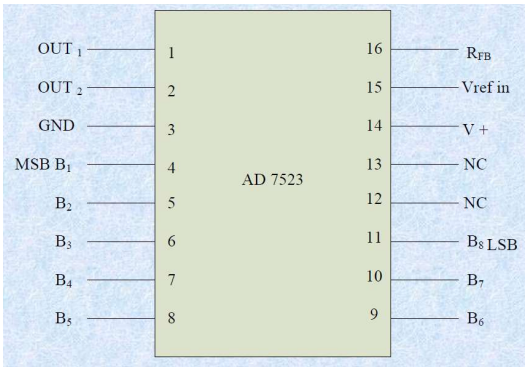
AD 7523 Pin Diagram

- Supply range is from +5V to +15V
- Vref may be any where between -10V to +10V
- The maximum analog output voltage will be any where between -10V to +10V
  - When all the digital inputs are at logic high state



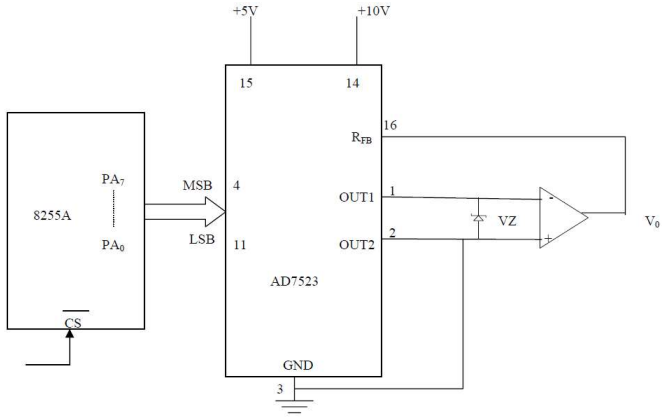
AD 7523 Pin Diagram

- Usually a zener diode is connected between OUT1 and OUT2
  - Save the DAC from negative transients
- An operational amplifier is used as a current to voltage converter at the output of AD 7523
  - convert the current output to a proportional output voltage
  - It also offers additional drive capability to the DAC output.
  - An external feedback resistor acts to control the gain. One may not connect any external feedback resistor, if no gain control is required.



Example

- Interface DAC AD7523 with an 8086 CPU running at 8MHZ and write an assembly language program to generate a sawtooth waveform of period 1ms with Vmax 5V



Sawtooth Waveform Generating Code

```
ASSUME    CS:CODE
CODE SEGMENT
START:    MOV AL,80h      ;make all ports output
          OUT CW, AL
AGAIN:    MOV AL,00h      ;start voltage for ramp
BACK:     OUT PA, AL
          INC AL
          CMP AL, 0F2h
          JB BACK
          JMP AGAIN
CODE ENDS
END       START
```

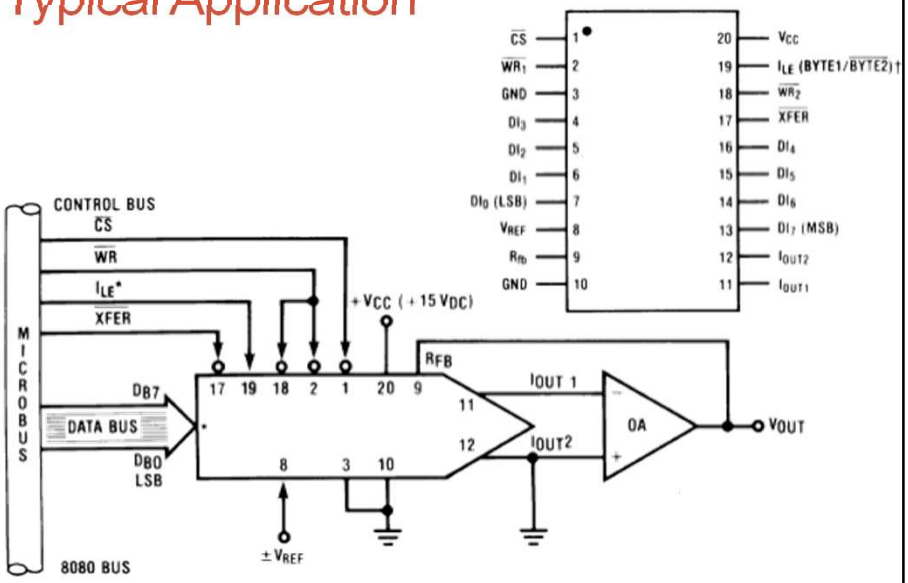
Sawtooth Waveform Generating Code

- In the above program, port A is initialized as the output port for sending the digital data as input to DAC. The ramp starts from the 0V (analog), hence AL starts with 00H. To increment the ramp, the content of AL is increased during each execution of loop till it reaches F2H
- After that the saw tooth wave again starts from 00H, i.e. 0V(analog) and the procedure is repeated. The ramp period given by this program is precisely 1.000625 ms. Here the count F2H has been calculated by dividing the required delay of 1ms by the time required for the execution of the loop once. The ramp slope can be controlled by calling a controllable delay after the OUT instruction

DAC0830/DAC0832 8-Bit Microprocessor Compatible DAC

- An advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z80®, and other popular microprocessors
- A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature)

Typical Application



ANALOG TO DIGITAL [ADC] INTERFACING

ADC Basic Principle

- The basic principle of operation is to use the comparator principle to determine whether or not to turn on a particular bit of the binary number output
- It is typical for an ADC to use a digital-to-analog converter (DAC) to determine one of the inputs to the comparator

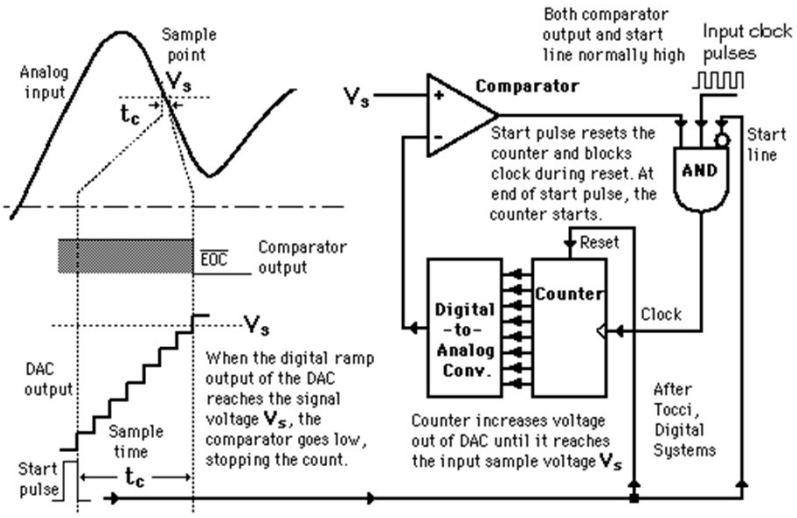
ADC Various Approaches

- 3 Basic Types
  - Digital-Ramp ADC
  - Successive Approximation ADC
  - Flash ADC

Digital-Ramp ADC

- Conversion from analog to digital form inherently involves comparator action where the value of the analog voltage at some point in time is compared with some standard
- A common way to do that is to apply the analog voltage to one terminal of a comparator and trigger a binary counter which drives a DAC

Digital-Ramp ADC



Digital-Ramp ADC

- The output of the DAC is applied to the other terminal of the comparator
- Since the output of the DAC is increasing with the counter, it will trigger the comparator at some point when its voltage exceeds the analog input
- The transition of the comparator stops the binary counter, which at that point holds the digital value corresponding to the analog voltage

Successive Approximation ADC

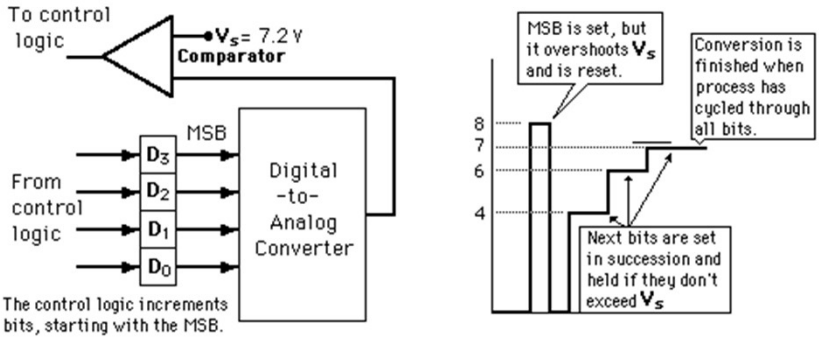
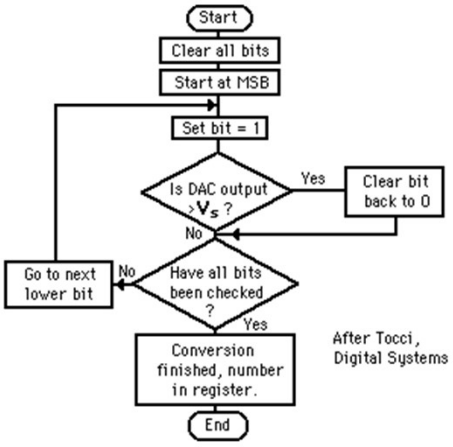


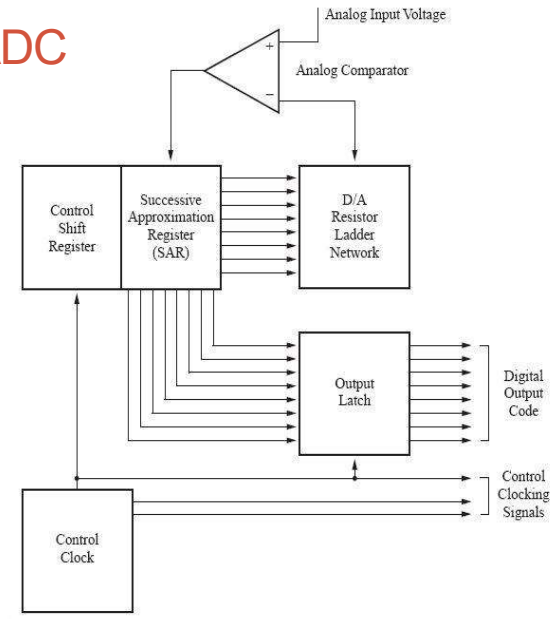
Illustration of 4-bit SAC with 1 volt step size

Successive Approximation ADC

- Much faster than the digital ramp ADC because it uses digital logic to converge on the value closest to the input voltage
- A comparator and a DAC are used in the process

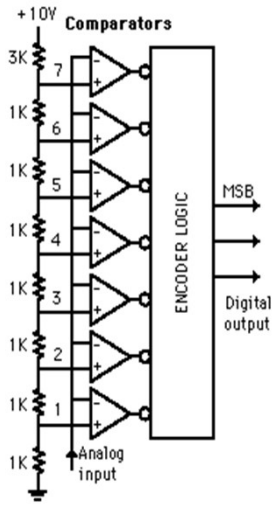


Successive Approximation ADC



Flash ADC

- It is the fastest type of ADC available, but requires a comparator for each value of output
  - (63 for 6-bit, 255 for 8-bit, etc.)
- Such ADCs are available in IC form up to 8-bit and 10-bit flash ADCs (1023 comparators) are planned
- The encoder logic executes a truth table to convert the ladder of inputs to the binary number output



Illustrated is a 3-bit flash ADC with resolution 1 volt

Flash ADC

- The resistor net and comparators provide an input to the combinational logic circuit, so the conversion time is just the propagation delay through the network
  - It is not limited by the clock rate or some convergence sequence

Interfacing Analog to Digital Converters

- ADC is treaded as an input device by the microprocessor.
- Microprocessor sends an initializing signal to the ADC to start the A-D data conversation process
  - Start of conversation (SOC) signal is a pulse of a specific duration
- The process of analog to digital conversion is a slow process
  - Microprocessor has to wait for the digital data till the conversion is over
- After the conversion is over, the ADC sends end of conversion (EOC) signal to inform the microprocessor that the conversion is over and the result is ready at the output buffer of the ADC
- The tasks of issuing an SOC pulse to ADC, reading EOC signal from the ADC and reading the digital output of the ADC are carried out either directly by the CPU or using 8255 I/O ports

Interfacing Analog to Digital Converters

- The time taken by the ADC from the active edge of SOC pulse till the active edge of EOC signal is called as the *conversion delay* of the ADC
- It may range any where from a few microseconds in case of fast ADC to even a few hundred milliseconds in case of slow ADCs
- The available ADC in the market use different conversion techniques for conversion of analog signal to digitals.
  - Successive approximation techniques and dual slope integration techniques are the most popular techniques used in the integrated ADC chip

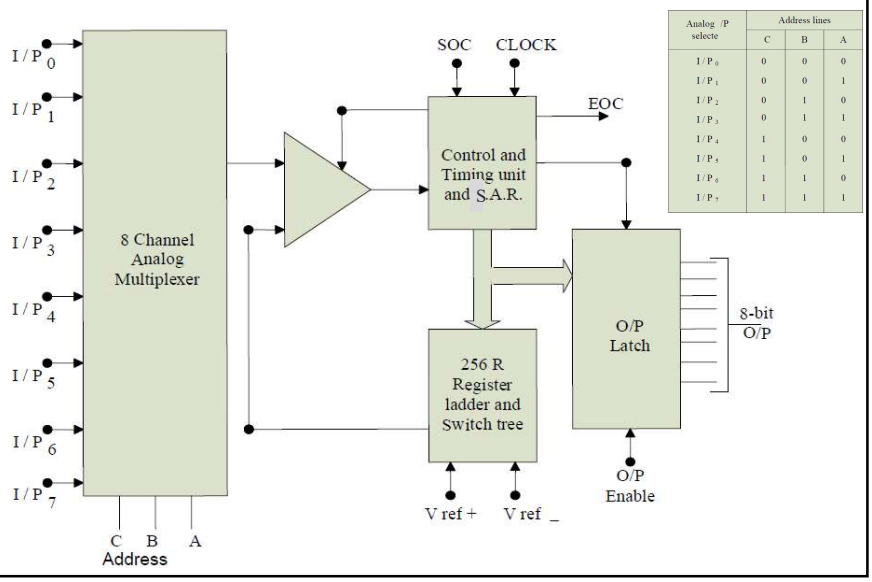
General Algorithm for ADC Interfacing

1. Ensure the stability of analog input, applied to the ADC
   - Sample and hold circuit
     - Samples the analog signal and holds it constant for a specific time duration
     - Microprocessor may issue a hold signal to the sample and hold circuit
2. Issue start of conversion pulse to ADC
3. Read end of conversion signal to mark the end of conversion processes
4. Read digital data output of the ADC as equivalent digital output
   - If the applied input changes before the complete conversion process is over, the digital equivalent of the analog input calculated by the ADC may not be correct

ADC 0808/0809

- 8-bit CMOS, successive approximation converters
  - One of the fast techniques for analog to digital conversion
    - Conversion delay is 100μs at a clock frequency of 640 KHz, which is quite low as compared to other converters
- There are unipolar analog to digital converters, i.e. they are able to convert only positive analog input voltage to their digital equivalent
- These chips do not contain any internal sample and hold circuit
- These converters do not need any external zero or full scale adjustments as they are already taken care of by internal circuits
- These converters internally have a 3:8 analog multiplexer so that at a time 8 different analog conversion by using address lines - ADD A, ADD B, ADD C
  - Using these address inputs, multichannel data acquisition system can be designed using a single ADC
    - The CPU may drive these lines using output port lines
  - In case of single input applications, these may be hardwired to select the proper input

Block Diagram of ADC 0808 / 0809



Analog I/P selecte	Address lines		
	C	B	A
I / P 0	0	0	0
I / P 1	0	0	1
I / P 2	0	1	0
I / P 3	0	1	1
I / P 4	1	0	0
I / P 5	1	0	1
I / P 6	1	1	0
I / P 7	1	1	1

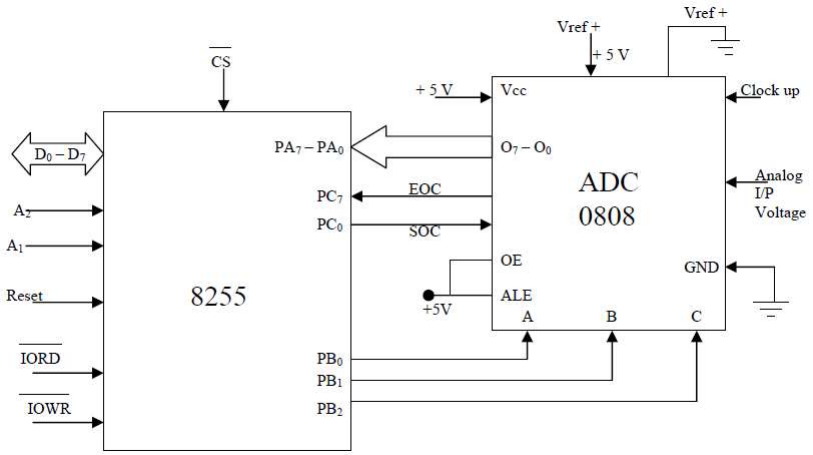
ADC 0808 / 0809 Pin Description

- Vcc Supply pins +5V
- GND GND
- Vref+ Reference voltage positive +5 Volts maximum.
- Vref- Reference voltage negative 0Volts minimum.
- I/P0 –I/P7 Analog inputs
- ADD A,B,C Address lines for selecting analog inputs.
- O7 – O0 Digital 8-bit output with O7 MSB and O0 LSB
- SOC Start of conversion signal pin
- EOC End of conversion signal pin
- OE Output latch enable pin, if high enables output
- CLK Clock input for ADC

Example: Interfacing 0808 with 8086

- Interfacing ADC 0808 with 8086 using 8255 ports. Use port A of 8255 for transferring digital data output of ADC to the CPU and port C for control signals. Assume that an analog input is present at I/P2 of the ADC and a clock input of suitable frequency is available for ADC.
- **Solution**: The analog input I/P2 is used and therefore address pins A,B,C should be 0,1,0 respectively to select I/P2. The OE and ALE pins are already kept at +5V to select the ADC and enable the outputs.
  - 8255 Port C upper acts as the input port to receive the EOC signal while port C lower acts as the output port to send SOC to the ADC
  - 8255 Port A acts as a 8-bit input data port to receive the digital data output from the ADC

Interfacing 0808 with 8086



ADC Assembly Control Code

```
        MOV   AL, 98h        ;initialise 8255 as
        OUT   CWR, AL        ;discussed above.
        MOV   AL, 02h        ;Select I/P2 as analog
        OUT   Port B, AL     ;input.
        MOV   AL, 00h        ;Give start of conversion
        OUT   Port C, AL     ; pulse to the ADC
        MOV   AL, 01h
        OUT   Port C, AL
        MOV   AL, 00h
        OUT   Port C, AL
WAIT:   IN    AL, Port C     ;Check for EOC by
        RCR                  ; reading port C upper and
        JNC   WAIT           ;rotating through carry.
        IN    AL, Port A     ;If EOC, read digital equivalent in AL
        HLT                  ;Stop.
```


ADC080x, 8-Bit Microprocessor Compatible A/D Converters interfacing