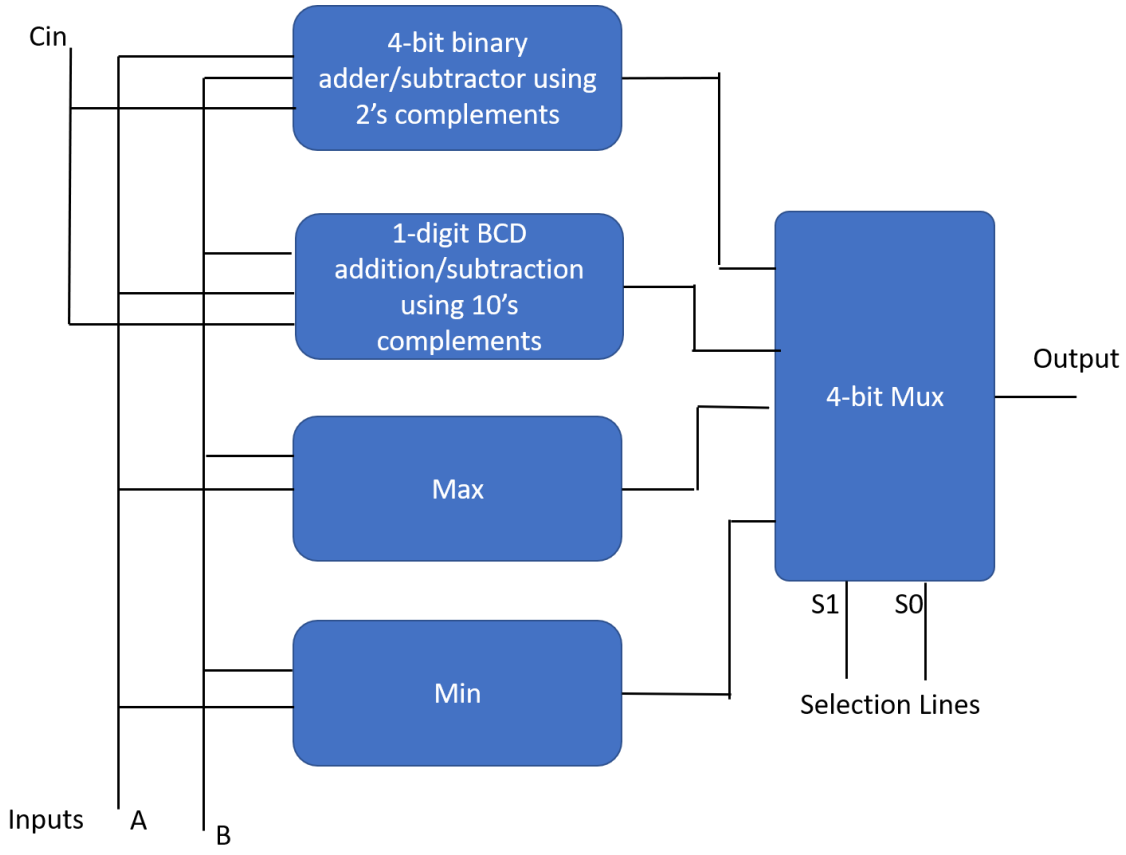
BIRZEIT UNIVERSITY

Faculty of Engineering & Technology
Electrical & Computer Engineering Department
Digital Systems ENCS234

Verilog Project

Implement and test the following combinational circuit using Verilog HDL:



Notes:

- The inputs (A, B) are 4-bits
- The output also is 4-bits
- The circuit will operate (the output of the circuit is) as following:

Cin	S1	S0	Output
0	0	0	4-bit addition
1	0	0	4-bit subtraction
0	0	1	BCD addition
1	0	1	BCD subtraction
x	1	0	Max(A, B)
x	1	1	Min(A, B)

Procedure:

- Implement the 1-bit binary adder/subtractor using structural Verilog HDL code.
- Use the created module of 1-bit binary adder/subtractor to build 4-bit adder/subtractor structurally, then using Quartus to create a symbol for it.
- Write the module of 1-digit BCD adder/subtractor, then using Quartus to create a symbol for it.
- Write the code of MAX module, then using Quartus to create a symbol for it.
- Write the code of the MIN module, then using Quartus to create a symbol for it.
- Write a Verilog HDL code to describe the module 4-bit 4×1 multiplexer, then using Quartus to create a symbol for it.
- Test each module.
- Use Quartus schematic to describe the whole system from its subsystems.
- Test the whole system.

Project Report

The report document must contain sections highlighting the following:

1 – Design and Implementation

- Specify clearly the design and implementation details of each components.
- Provide drawings of the component circuits and the overall system.
- Carry out the design and implementation with the following aspects in mind:
  - Correctness of the individual components
  - Correctness of the overall design when wiring the components together
  - Completeness: all operation were implemented properly.

2 – Simulation and Testing

- Carry out the simulation of each component.
- Carry out the simulation of the whole system.
- Also provide snapshots of the Simulator window with your test cases and showing the simulation output results.

3 – Teamwork

- Two students can form a group.
- Group members are required to coordinate the work equally among themselves so that everyone is involved in all the following activities:
  - Design and Implementation
  - Simulation and Testing
- Clearly show the work done by each group member.

Submission Guidelines

Attach one zip file containing all the design circuits, the programs source code (Screenshot is not allowed in writing the code (copy the code from Quartus software)) as well as the report document to Ritaj as a reply to this message.

Grading policy

The grade will be divided according to the following components:

1. Correctness: whether your implementation is working
2. Completeness and testing: whether all components and cases have been implemented, handled, and tested properly
3. Participation and contribution to the project
4. Report document

Deadline

4/7/2020