Digital Logic Design (CE221) Project Proposal

Digital Logic-Based Elevator Control with Real-Time Feedback

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Abstract

This project aims to design and implement a fully operational elevator control system using digital logic circuits. Elevators are essential systems in modern buildings, and their efficient operation relies on advanced control mechanisms. Our project replicates such a system to simulate essential functionalities like floor selection, direction indication, and real-time feedback, using fundamental digital components such as logic gates, flip-flops, counters, and decoders.

The objective of the project is to provide a deeper understanding of digital logic design principles by constructing a functional prototype that handles multiple floor requests, displays the current floor using a 7-segment display, and provides user-friendly interaction through LEDs and auditory feedback. Key features include sequential logic for state memory, combinational logic for decision-making, and a buzzer for auditory cues.

The project utilizes hardware like breadboards and integrated circuits for implementation and simulation tools like Logisim and Multisim for design validation. A shift register ensures controlled delays, while comparators handle floor requests and current floor comparisons.
The system's operation includes LEDs indicating elevator direction and stop status, alongside push buttons for floor selection.

The outcome demonstrates a reliable and efficient prototype that integrates various digital logic principles into a cohesive system, simulating real-world elevator operations. The project also highlights the potential of digital systems in addressing practical challenges. It serves not only as an educational tool but also as a foundation for understanding complex automated systems, paving the way for applications in elevator systems, automated gates, and other control systems.

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Introduction

Background

Elevators are indispensable in modern infrastructure, offering efficient vertical transportation in residential and commercial buildings. As the demand for automation grows, elevator systems serve as a prime example of digital logic principles in action, combining hardware components with intelligent control mechanisms. Their ability to manage user requests, track floor positions, and provide real-time feedback highlights the practical application of digital circuits. This project leverages the principles of combinational and sequential logic to emulate such a system, bridging theoretical concepts with practical implementation. Beyond academics, the project showcases how digital systems address real-world challenges like optimizing transportation efficiency and safety in automated environments.

Objective

The primary goal of this project is to design and implement a fully operational elevator control system using fundamental digital logic components. The system is intended to prioritize and process user floor requests, display the current floor using a 7-segment display, and provide directional and status indicators through LEDs. By integrating various digital logic components such as flip-flops, counters, and comparators, the project aims to create a functional prototype that demonstrates efficient request handling, precise feedback mechanisms, and user-friendly interaction.

Scope

The project focuses on the design and construction of an elevator control system suitable for a multi-story building. It incorporates essential features such as floor selection, direction indication, and emergency stop functionality. The design is limited to using basic digital components like logic gates, counters, flip-flops, encoders, 7447 BCD to Seven Segment Converter. While the prototype does not control a physical elevator, it simulates real-world operations effectively, serving as a model for practical elevator systems. Additionally, it highlights the educational value of digital logic principles in solving real-life automation challenges.

Overview

This report details the development process of the elevator control system. The **Methodology** section outlines the problem statement, design requirements, approach, and tools used. The **Implementation** section provides a step-by-step explanation of simulations and hardware assembly. Results are discussed in the **Results and Discussion** section, covering findings, challenges, and comparisons. The report concludes with insights into the potential applications and limitations of the project.

Methodology

Problem Statement:

- Physical effort reduction:
  To eliminate the need for individuals to climb stairs, particularly for those with mobility limitations or carrying heavy loads.
- Significantly reduces travel time between floors, especially in multi-story buildings
- Ensures accessibility for people with disabilities
- Provides a controlled environment, reducing the risk of accidents associated with stairs, such as falls or slips.

Design Requirements

Components List with Specification:

1. Seven Segment Display

- To show the floor number

2. Push Buttons

- Represent floor call buttons
- **Voltage Rating**: Typically 5V-12V

3. LEDs

- For indicating status(direction (up or down) and stop)
- Type: Standard LED.
- Forward Voltage: ~2V (red) or ~3V (green).
- Current: ~20mA.

4. Comparator (4063)

- To compare the current floor (from the counter) with the requested floor (from the encoder).
- 4-bit magnitude comparator
- **Inputs**: Two 4-bit binary numbers

Note: We used 4-bit magnitude comparator because 3-bit magnitude comparator is not commercially available in GIKI's locality.

5. **555 Timer**
   - ❖ Function: Generates precise time delays (Clock pulses)
   - ❖ Specifications: Operating voltage 4.5V-16V, adjustable timing.

6. **8-to-3 Encoder (10165)**
   - ❖ Encodes the requested floor number into a 3-bit binary number

7. **Counter (74LS190)**
   - ❖ Tracks the current floor and counts up/down to the requested floor
   - ❖ Specifications: Synchronous counter, Voltage: 5V, Max Frequency = 25MHz

8. **BCD to 7-segment converter (7447)**
   - ❖ Converts the BCD (Binary) floor number to 7-segments inputs for display

9. **Basic Logic Gates (AND, OR, NOT, XOR etc.) and Push Buttons**
   - ❖ For manipulating the clock input and Up/Down counting control
   - ❖ Push Buttons are used for Floor Request and Emergency Stop

Design Approach

Logic Design and Flow:

When a button is pressed, it sends a signal to the 8-to-3 Encoder (10165) to encode the requested floor.

Encoder receives the signals from the push buttons and sends 3-bit encoded data to the **Comparator** (4063) and the **Counter** (74LS193). Comparator compares the current floor (from the counter) with the requested floor (from the encoder).

UP Led lights up when the requested floor is higher than the current floor. Down Led lights up when the requested floor is lower than the current floor. Stop Led lights up when the requested floor equals the current floor.

555 Timer drives the **Counter** (74LS193) to increment or decrement the floor number. Counter then sends the current floor value (binary) to the **Comparator** and the **7-Segment Display.** Seven segment display receives the input in binary and displays the current floor number in decimal.

Truth Tables

1. Comparator (For comparing 2 bits)

Inputs		Outputs		
B	A	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Note: 3-bit comparator Truth Table is an extension of the table above. It was not practical to include it here.

Karnaugh Maps for Each Output:

1. $A > B$

$A \backslash B$	0	1
0	0	0
1	1	0

Simplified Expression:

$$A > B = A \cdot \overline{B}$$

2. $A = B$

$A \backslash B$	0	1
0	1	0
1	0	1

Simplified Expression:

$$A = B = \overline{A} \cdot \overline{B} + A \cdot B$$

3. $A < B$

$A \backslash B$	0	1
0	0	1
1	0	0

Simplified Expression:

$A < B = \overline{A} \cdot B$

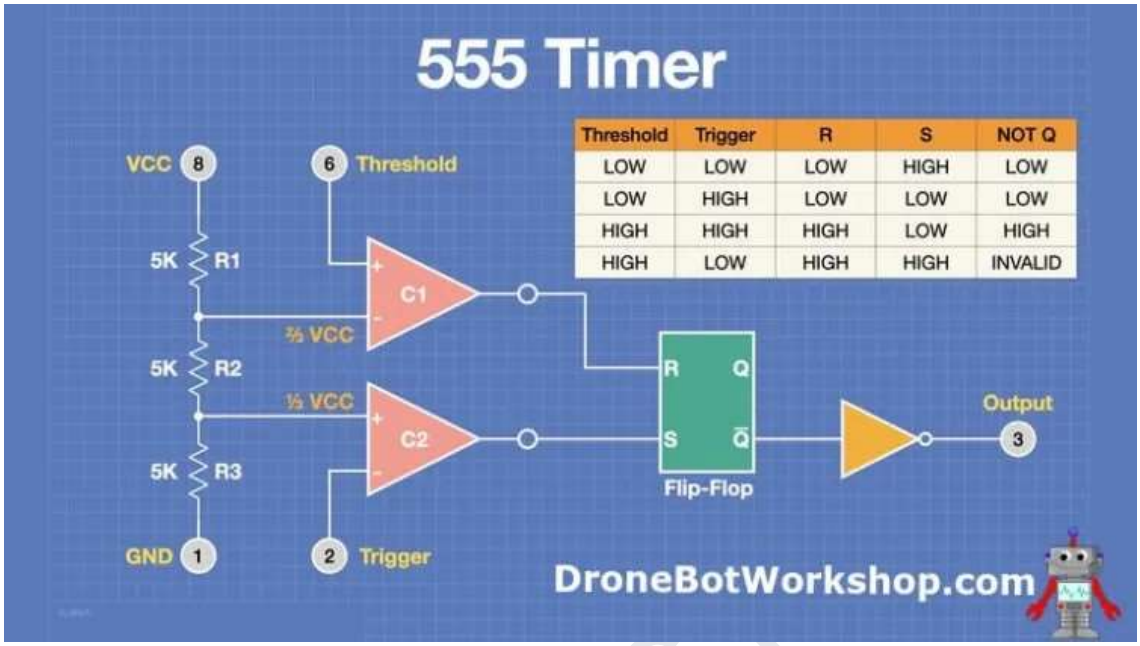
2. Encoder

Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

X = Don't Care

Note: K-Maps for Encoder are not needed as it can be constructed simply and taking OR operation of the decimal inputs.

3. 555 Timer



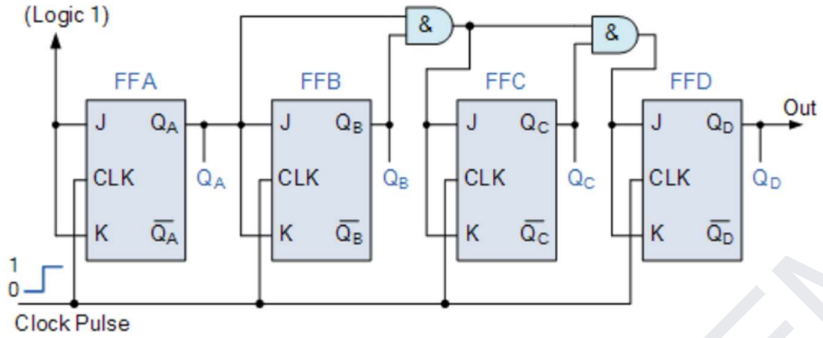
4. 4-bit Synchronous Up/Down Counter

Excitation table:

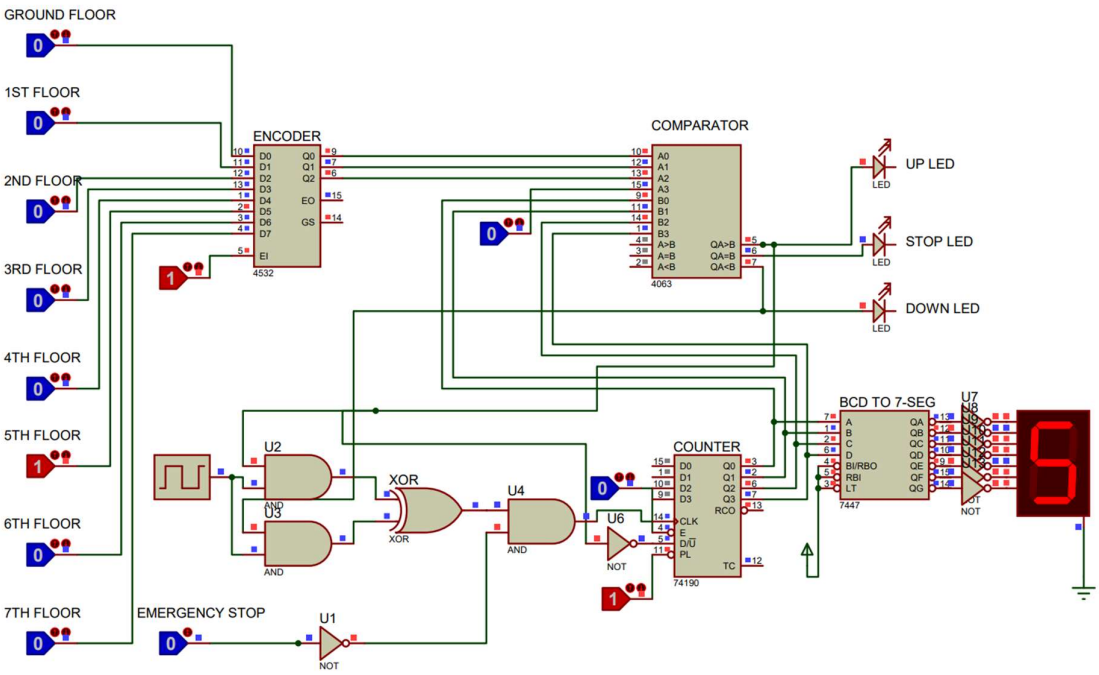
Counter States								JK FLIPFLOP INPUTS							
PRESENT STATE				NEXT STATE											
Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0	J0	K0	J1	K1	J2	K2	J3	K3
0	0	0	0	0	0	0	1	1	X	0	X	0	X	0	X
0	0	0	1	0	0	1	0	X	1	1	X	0	X	0	X
0	0	1	0	0	0	1	1	1	X	X	0	0	X	0	X
0	0	1	1	0	1	0	0	X	1	X	1	1	X	0	X
0	1	0	0	0	1	0	1	1	X	0	X	X	0	0	X
0	1	0	1	0	1	1	0	X	1	1	X	X	0	0	X
0	1	1	0	0	1	1	1	1	X	X	0	X	0	0	X
0	1	1	1	1	0	0	0	X	1	X	1	X	1	1	X
1	0	0	0	1	0	0	1	1	X	0	X	0	X	X	0
1	0	0	1	1	0	1	0	X	1	1	X	0	X	X	0
1	0	1	0	1	0	1	1	1	X	X	0	0	X	X	0
1	0	1	1	1	1	0	0	X	1	X	1	1	X	X	0
1	1	0	0	1	1	0	1	1	X	0	X	X	0	X	0
1	1	0	1	1	1	1	0	X	1	1	X	X	0	X	0
1	1	1	0	1	1	1	1	1	X	X	0	X	0	X	0
1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1

Note: 5 input Kmaps (including U/D) are not part of the CE221 course. A schematic circuit diagram is provided below for 4-bit Up/Down Counter

Binary 4-bit Synchronous Up Counter



Schematic Circuit Diagram for Elevator Control System



Results

Our elevator system successfully operates as intended, efficiently handling floor selection and movement. The system uses a combination of binary counters, BCD-to-7-segment decoders, and other components to display the current floor and respond to user inputs. The logic design ensures smooth functionality within the constraints of the hardware.

Conclusions

- The project demonstrated how fundamental digital logic principles can be applied to real-world scenarios.
- Effective teamwork and debugging were critical in achieving a functional system.
- The design is scalable and could be enhanced for more complex elevators.

Challenges and Solutions

1. **Component Compatibility**:
   - **Challenge**: Finding compatible components (e.g., 7-segment display drivers).
   - **Solution**: Extensive research and testing ensured we selected suitable parts.
2. **Invalid Input Handling**:
   - **Challenge**: Managing invalid BCD inputs that caused undefined states.
   - **Solution**: Implemented constraints in the circuit and corrected wiring issues.
3. **Wiring Complexity**:
   - **Challenge**: Managing the large number of connections in Proteus.
   - **Solution**: Systematic testing and modular design simplified the debugging process.

Future Prospects

- **Expansion**: The system can be extended to support more floors or multi-car elevators.
- **Integration**: Adding microcontrollers for advanced features like smart scheduling and weight sensors.
- **Efficiency**: Optimizing the design for reduced power consumption and faster response times.
- **Safety**: Incorporating emergency stop mechanisms and fault detection.

This project lays a strong foundation for transitioning from basic digital systems to more sophisticated, real-world engineering solutions.