UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Spring 1398-99
Computer Assignment 1
Basic Switch and Gate Structures in Verilog
Week 4

Name:
Date:

1. Generate switch level description for a Majority gate (MAJ) using a complex gate structure. The output of MAJ is w_m = ~(a&b | a&c | b&c). Write this description in Verilog using NMOS and PMOS transistors used in CMOS structures. Use #(3, 4, 5) delay for the NMOS transistors and #(5, 6, 7) for the PMOS transistors. Use inverters where needed, and describe them at the switch level using the same transistors. Show a symbol for MAJ that represents its implementation as a complex gate structure. I.e., a structure with only one pull-up and one pull-down.
2. Write switch level 2- and 3-input NAND structures using transistors of Part 1. Simulate these gates and extract worst-case *to1* and *to0* gate delay values.
3. Write Verilog description for MAJ using Verilog NAND primitives. Use worst-case delay values for the NAND gates obtained in Part 2.
4. In a testbench instantiate MAJ of Part 1 (MAJ1) and MAJ of Part 3 (MAJ3). Run simulations and compare the two outputs. Explain the differences.
5. Write a new MAJ module (MAJ5) using SystemVerilog **assign** statement. This structure has two places for delay parameters, *to1* and *to0*. Use parameters for this module in place of the two delay values; call them *d0to1* and *d1to0*. Simulate MAJ5 along with MAJ1 to estimate the delay parameters for MAJ5. Back-annotate these delay parameters into *d0to1* and *d1to0*. Take the extracted parameters and using #(..) in the instantiation of MAJ5 run the simulations and compare the results.

6. Write a 3-input ODD gate whose output is w_o = (a ^ b ^ c). Use parameters for the delay values as you did in Part 5. Based on the transistor structure of this gate and the delay values as given in Part 1, estimate the delay values of this gate. Refer to this module as ODD6.

7. In a testbench use parameterized MAJ5 and ODD6 in a circuit with a, b, c inputs and r, and s outputs. Run simulations and report the results.