report of CA#1

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part 1) output MAJ is $w_m = (a\&b|a\&c|b\&c)$

in This structure we use 24 transsistor.

in a cmos stractale That called MAJ

we use six wires for simulate

The Design and a,b,c main input

and 1 output called w_m.

pullup And pulldown desig correctly

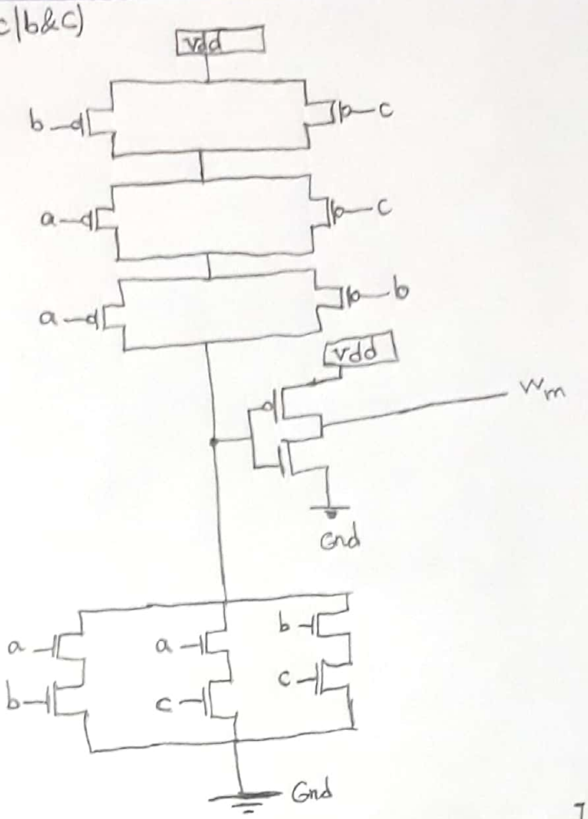
As you see.

but in code ⇒ All of details

of design transfer into code

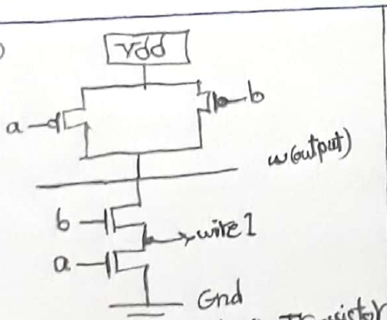
in switch level forexample

⇒ nmos #(3,4,5) T1 (drain, source, control)
pmos #(5,6,7) T2 (drain, source, control)



⇒ AFter simulate the design I have a test bench That gets Three inputs and 1 output the delay Assign arbitary and in last step we will see the wave form and analyze the wave.

part 2-1 2-input NAND



in This part we have a cmos 2-nand structure

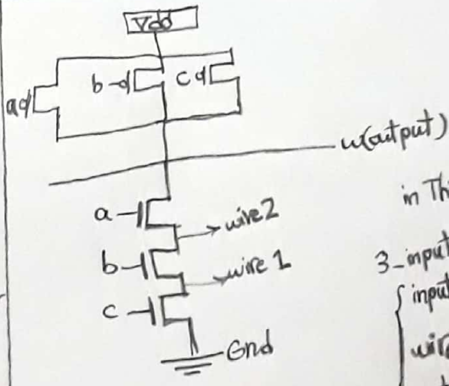
- input ⇒ a, b
- wire ⇒ wire 1
- output ⇒ w

I design That in a NAND module. AND with 4 Transsistor 2nmos and 2pmos with given delay I omplete The circuit. AFter That we assign values to every input and output in TB and in last part we analyze the wave.

calculate delay for 2-input NAND ⇒

nmos(3,4,5)
pmos(3,6,7) ⇒ delay
To ∅ ⇒ #8ns
To 1 ⇒ #10ns

3-input NAND (part 2-2



in This part we have a cmos 3_input structure

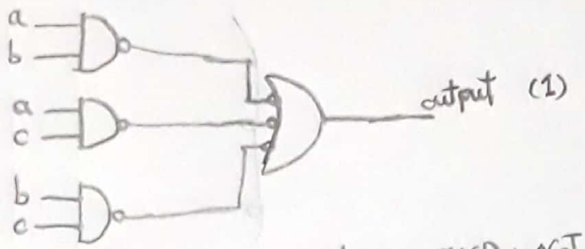
- input ⇒ a, b, c
- wire ⇒ wire 1, wire 2
- output ⇒ output

in This part I repeat all of work which done in previous section.

calculate delay for 3_input NAND ⇒

nmos(3,4,5)
pmos(5,6,7) ⇒
To ∅ ⇒ #12ns
To 1 ⇒ #15ns

part 3) After make a cmos gate we have a circuit with only NAND gates.



3 2-input nand
+
1 3-input nand

in This part we replace AND with ~~a~~ NAND+NOT it conclused a circuit like Figure above.
modalesim has NAND primitives with below syntax.
NAND #(To1,To0) name(out1, in1, in2,....). in last step I use the value delay for nand obtained in part 2 as you see in my code. After that the action of assign value in testbench will done and the analyze wave is the last step for us :)

part 4) we have a test bench that contain both MAJ (1 & 3) with same inputs. After simulate And ran we have 2 wave-form. diffrence of two waves are related to delay and accuracy
The Time between to 1 in both waves is Almost 10ns.
and the accuracy of MAJ 1(switch level) is better than MAJ3 (gate level)

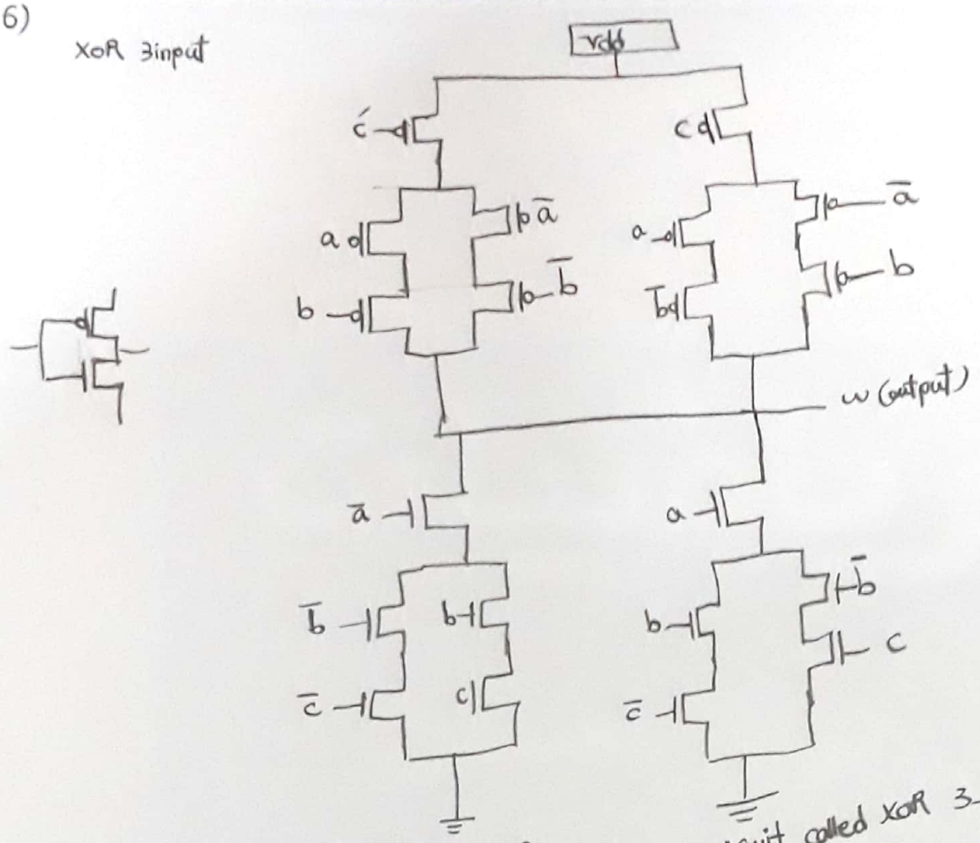
part 5) in This part we learn how to use Assign to make a optimum output of MAJ (MAJ5)
in this part we extract the delay from wave of MAJ(1) [switch level] then use these delay inplace of two delay value of assign structure.

These delay → To1 = 26ns
To0 = 22ns
→ extract from wave

but in code → After use Assign to make structure MAJ we have problem with testbench.
in testbench we declare MAJ1(part I) and MAJ5 and the last step is assign value for inputs and outputs
with Analyze the wave MAJ1 we extract the delay and use them as parameters of assign

part 6)

XoR 3input



in This part we should calculate the delay for above circuit called XoR 3_input

delay not gate $\begin{cases} \text{To } 0 & 7ns \\ \text{To } 1 & 5ns \end{cases}$

the worst case delay $\begin{cases} \text{To1} \Rightarrow \text{worst path} \Rightarrow 3*5 + \text{worst not}(7ns) = \boxed{22ns} \\ \text{to } 0 \rightarrow \text{worst path} \rightarrow 3*7 + \text{worst not}(5ns) = \boxed{26ns} \end{cases}$

in my code ⇒ like part 5, I use assign to make ODD structure with delay value which calculate above and After that we have a module ODD_TB That used to assign value to inputs and output just like always we analyze the wave. and

part 7) in This part I use a testbench and declare both ODD and MAJ5 structure with same input a, b, c and output r for MAJ5 & output s for ODD and analyze both wave form in simulation of modulesim.

The results shows that MAJ and ODD are complementary this mean when output of MAJ is zero the output of ODD is one. (Except in 000 & 111)

This result shown in figures.

a	b	c	MAJ(r)	ODD(s)
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
1	0	0	0	1
0	1	1	1	0
1	1	0	1	0
1	0	1	1	0
1	1	1	1	1