UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, Spring 1398-99
Computer Assignment 2
Basic Switch and Gate Structures in Verilog
Week 7

Name:
Date:

1. Write a 3-input parameterized MAJ gate, using delay values as the parameters. Similarly, generate a 3-input XOR gate (the ODD circuit from Assignment 1).
2. Generate a full adder using MAJ and XOR circuits of Part 1. Write this description in SystemVerilog. Use delay parameters based on the circuits you developed in Assignment 1.
3. Using SystemVerilog **generate** statement, generate a 16-bit adder using 16 instances of the full adder of Part 2.
4. Simulate the adder of Part 3 in a SystemVerilog testbench. Manually estimate the worst-case delay of this circuit. Use the test vector obtained manually in your testbench to validate the worst-case delay and the test vector that causes it.
5. Use a 5-variable Karnaugh map to build a 2-bit adder with a_1, a_0, b_1, b_0, and *ci* (carry-in) inputs, and s_1, s_0, and *co* (carry-out) outputs. Using a single **assign** statement write SystemVerilog description of this circuit. If this circuit is built using NAND gates of Assignment 1, estimate the delay values for the outputs of this circuit. Use the worst-case of all the delay values (*to1*, *to0*) for the **assign** statement describing the 2-bit adder.
6. Using SystemVerilog **generate** statement, generate a 16-bit adder using 8 instances of the 2-bit adder of Part 5.
7. Simulate the adder of Part 6 in a SystemVerilog testbench. Manually estimate the worst-case delay of this circuit. Use the test vector obtained manually in your testbench to validate the worst-case delay and the test vector that causes it.
8. Write a testbench and instantiate both adders of Part 3 and Part 6. Use the same test data for both adders. Compare the outputs and explain the differences.