A) the first step for designing the tanh module is generating Rom ; in this part we need a .mif file to store data as shown below.

addres	000	001	010	011	100	101
.mif → memory	0000000000000	0110011001100	0110011110011	1000101001011	0000010000011	0011000000011

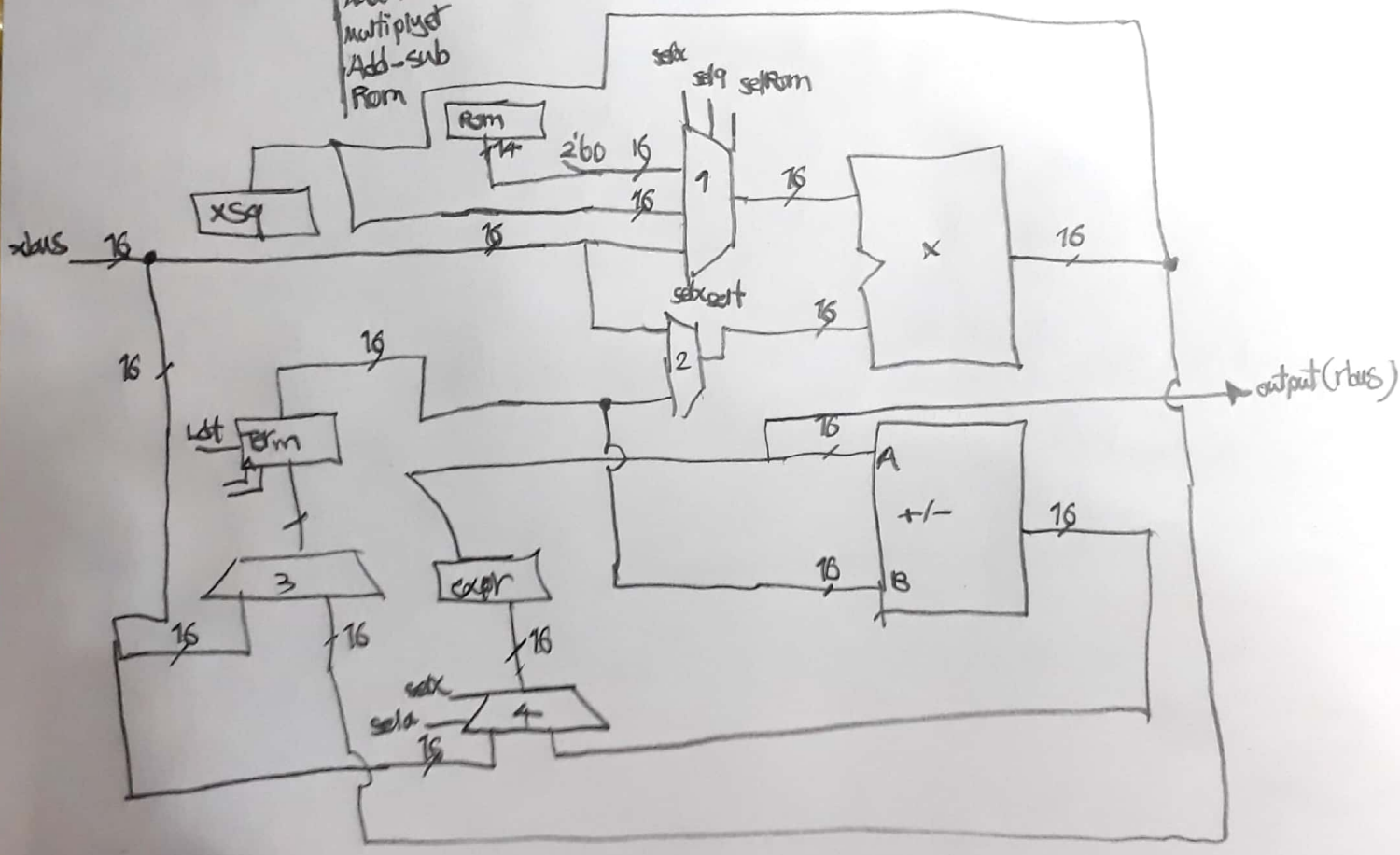
110	111
0000000110100	0001011010101

After that I use th 1-port Rom perinities of qurtus to load my .mif file and generate Rom

B) in this part according to the discribtion of CA I made all of block I need to design the datapath

as we now ⇒ counter, tanh_reg, expr_reg, xsq_reg, mux1, mux2, mux3, mux4, multiplyer, Add-sub, Rom

in This part I select the option of writing the components in verilog and then creat the schem_block

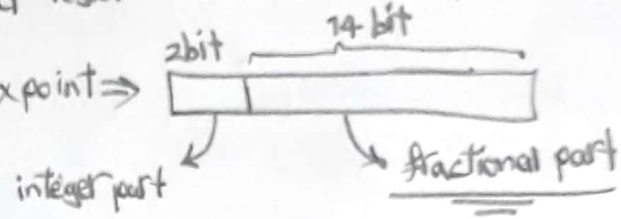


the datapath of tanh module

C) the verilog ode has been attached in my file. [both dp & controll_unit)

D) in quartus I complete my schematic circuit and connected that to others unit such as cc_unit to make whole tanh module. and Then I write a testbench to test my module

* noTiced ⇒ The value domin that supported in my module included $0 < xbus < 1$ and in this region we have correct result. and also the fix_point 16 bit input and output mentioned as below ⇒ fix point ⇒



E) after compliting my schematic now I synthesize that in quartus and after that we created the .VO file that included all of detail of tanh_module and as we know in this part we created a post_synthesis output and then I added the .VO file and the TB I develop in part D to pre_simulate my tanh module. *noticed all of my result as screenshot and file has been attached *

F) the last part of CA we use TB of part D to simulate pre and post synthesis in This part we added .VO and .V and instatiate both of them is a testbench and we see 2 wave and the only thing that we should do is comparing both signals.

* the result has been attached *

compare ⇒ the delay of module that obtain from schematic is more than simulating with the ode