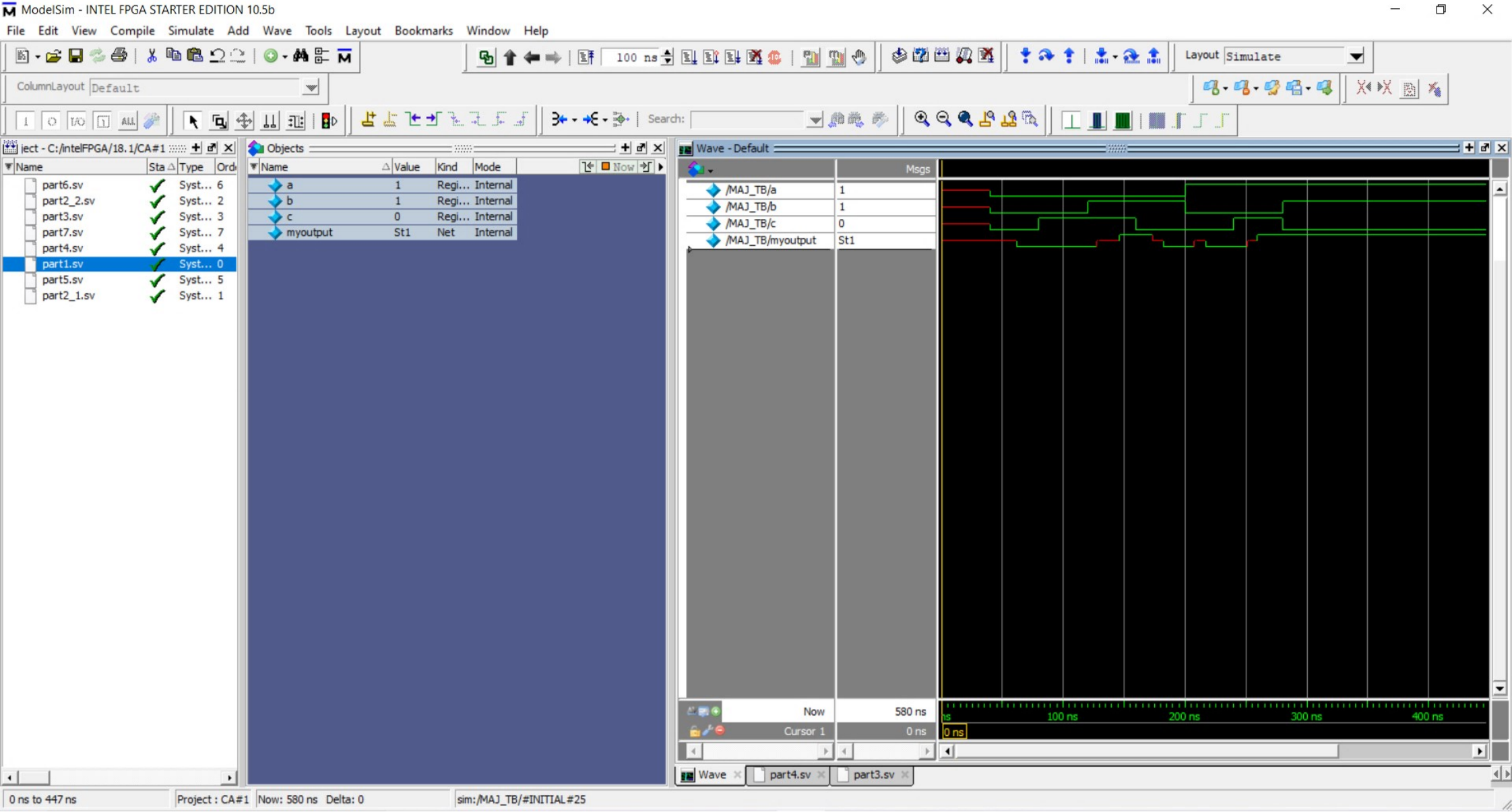
C:/intelFPGA/18.1/part1.sv (/MAJ_TB) - Default

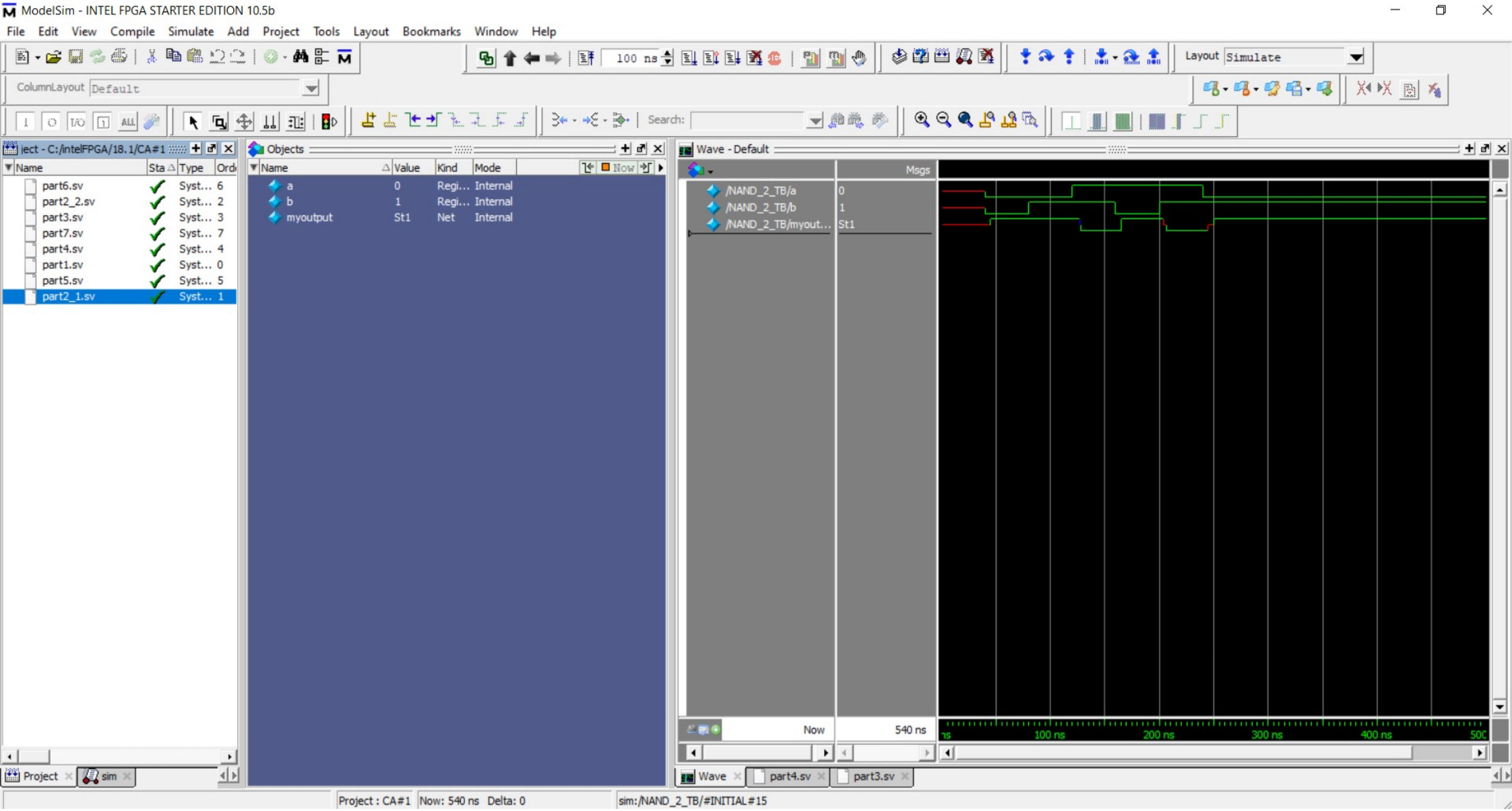
```
1  `timescale 1ns/1ns
2  module MAJ(input a,b,c,output w);
3  supply1 vdd;
4  supply0 Gnd;
5  wire j1,j2,j3,j4,j5,j6;
6  nmos#(3,4,5)T1(j1,Gnd,b);
7  nmos#(3,4,5)T2(j2,Gnd,c);
8  nmos#(3,4,5)T3(j3,Gnd,c);
9  nmos#(3,4,5)T4(j6,j1,a);
10 nmos#(3,4,5)T5(j6,j2,a);
11 nmos#(3,4,5)T6(j6,j3,b);
12 nmos#(3,4,5)T7(w,Gnd,j6);
13 pmos#(5,6,7)T8(j4,vdd,c);
14 pmos#(5,6,7)T9(j4,vdd,b);
15 pmos#(5,6,7)T10(j5,j4,a);
16 pmos#(5,6,7)T11(j5,j4,c);
17 pmos#(5,6,7)T12(j6,j5,a);
18 pmos#(5,6,7)T13(j6,j5,b);
19 pmos#(5,6,7)T14(w,vdd,j6);
20 endmodule
21 module MAJ_TB();
22 logic a,b,c;
23 wire myoutput;
24 MAJ tabe(a,b,c,myoutput);
25 initial begin
26 #40  a=0;b=0;c=0;
27 #40  c=1;
28 #40  b=1;
29 #40  c=0;
30 #40  a=1;b=0;c=0;
31 #40  c=1;
32 #40  c=0;b=1;
33 #300 $stop;
34 end
35 endmodule
36
```


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Objects
Name Value Kind Mode
a 1 Regi... Internal
b 1 Regi... Internal
c 0 Regi... Internal
myoutput St1 Net Internal
Wave - Default
Msgs
/MAJ_TB/a 1
/MAJ_TB/b 1
/MAJ_TB/c 0
/MAJ_TB/myoutput St1
Now 580 ns
Cursor 1 0 ns
100 ns
200 ns
300 ns
400 ns
part6.sv
part2_2.sv
part3.sv
part7.sv
part4.sv
part1.sv
part5.sv
part2_1.sv
Wave
part4.sv
part3.sv
0 ns to 447 ns
Project : CA#1
Now: 580 ns Delta: 0
sim:/MAJ_TB/#INITIAL#25

C:/intelFPGA/18.1/part2_1.sv - Default

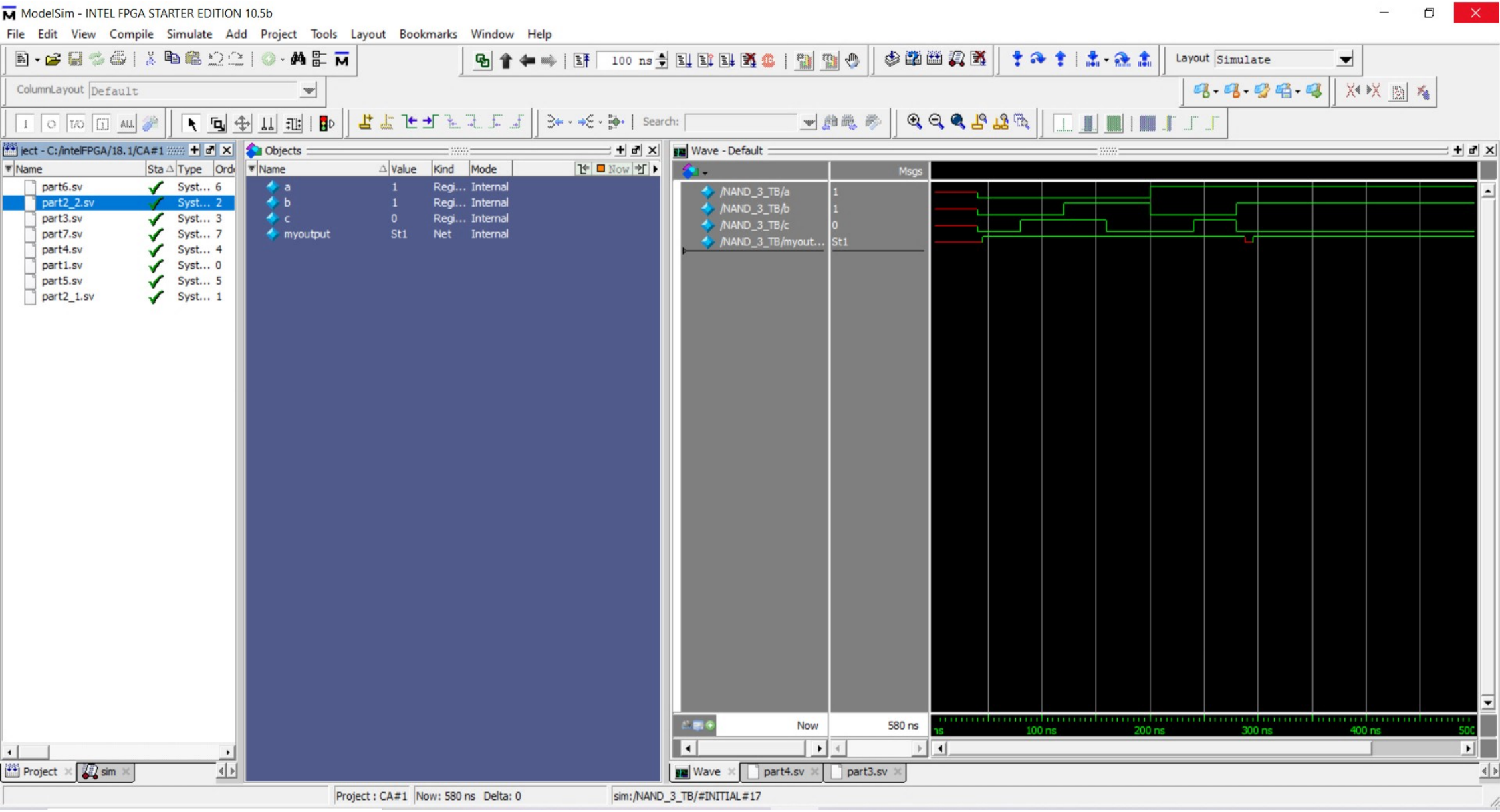
Ln#

```
1  `timescale 1ns/1ns
2  module NAND_2(input a,b,output w);
3  supply1 vdd;
4  supply0 Gnd;
5  wire j1;
6  nmos#(3,4,5)T1(j1,Gnd,a);
7  nmos#(3,4,5)T2(w,j1,b);
8  pmos#(5,6,7)T3(w,vdd,a);
9  pmos#(5,6,7)T4(w,vdd,b);
10 endmodule
11 module NAND_2_TB();
12 logic a,b;
13 wire myoutput;
14 NAND_2 tabe(a,b,myoutput);
15 initial begin
16 #40  a=0;b=0;
17 #40  b=1;
18 #40  a=1;
19 #40  a=1;b=0;
20 #40  b=1;
21 #40  a=0;b=1;
22 #300 $stop;
23 end
24 endmodule
25
```


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Objects
Name Value Kind Mode
a 0 Regi... Internal
b 1 Regi... Internal
myoutput St1 Net Internal
Wave - Default
Msgs
/NAND_2_TB/a 0
/NAND_2_TB/b 1
/NAND_2_TB/myout... St1
Now 540 ns
100 ns 200 ns 300 ns 400 ns
Project : CA#1 Now: 540 ns Delta: 0
sim:/NAND_2_TB/#INITIAL#15

C:/intelFPGA/18.1/part2_2.sv - Default

```
Ln#
 1  `timescale 1ns/1ns
 2  module NAND_3(input a,b,c,output w);
 3  supply1 vdd;
 4  supply0 Gnd;
 5  wire j1,j2;
 6  nmos#(3,4,5)T1(j1,Gnd,c);
 7  nmos#(3,4,5)T2(j2,j1,b);
 8  nmos#(3,4,5)T3(w,j2,a);
 9  pmos#(5,6,7)T4(w,vdd,a);
10  pmos#(5,6,7)T5(w,vdd,b);
11  pmos#(5,6,7)T6(w,vdd,c);
12  endmodule
13  module NAND_3_TB();
14  logic a,b,c;
15  wire myoutput;
16  NAND_3 tabe(a,b,c,myoutput);
17  initial begin
18  #40  a=0;b=0;c=0;
19  #40  c=1;
20  #40  b=1;
21  #40  c=0;
22  #40  a=1;b=0;c=0;
23  #40  c=1;
24  #40  c=0;b=1;
25  #300 $stop;
26  end
27  endmodule
28
```

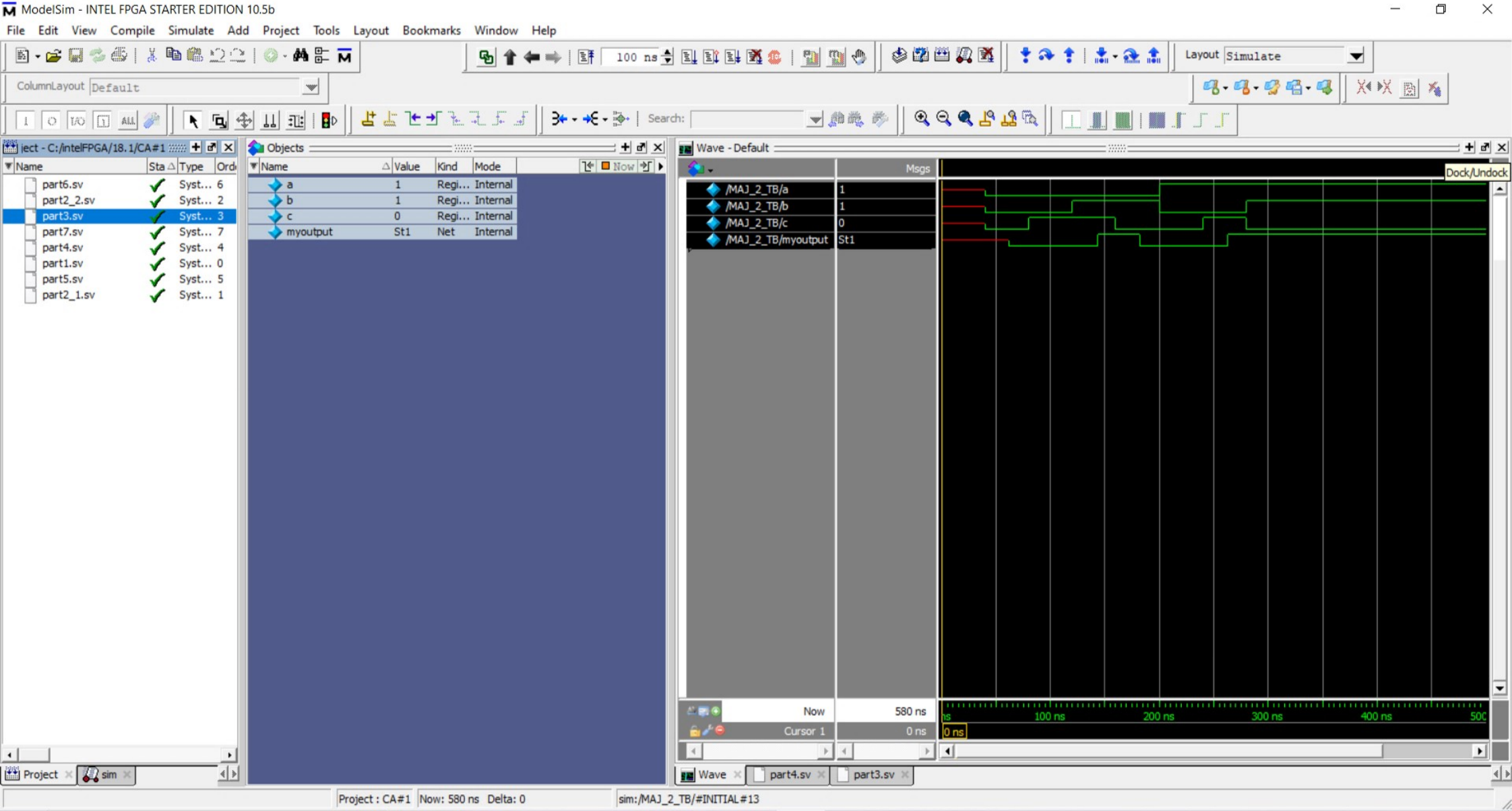

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
ject - C:/intelFPGA/18.1/CA#1
Name Sta Type Ord
part6.sv Syst... 6
part2_2.sv Syst... 2
part3.sv Syst... 3
part7.sv Syst... 7
part4.sv Syst... 4
part1.sv Syst... 0
part5.sv Syst... 5
part2_1.sv Syst... 1
Project sim
Objects
Name Value Kind Mode
a 1 Regi... Internal
b 1 Regi... Internal
c 0 Regi... Internal
myoutput St1 Net Internal
Wave - Default
Msgs
/NAND_3_TB/a 1
/NAND_3_TB/b 1
/NAND_3_TB/c 0
/NAND_3_TB/myout... St1
Now 580 ns
100 ns 200 ns 300 ns 400 ns
Wave part4.sv part3.sv
Project : CA#1 Now: 580 ns Delta: 0 sim:/NAND_3_TB/#INITIAL#17

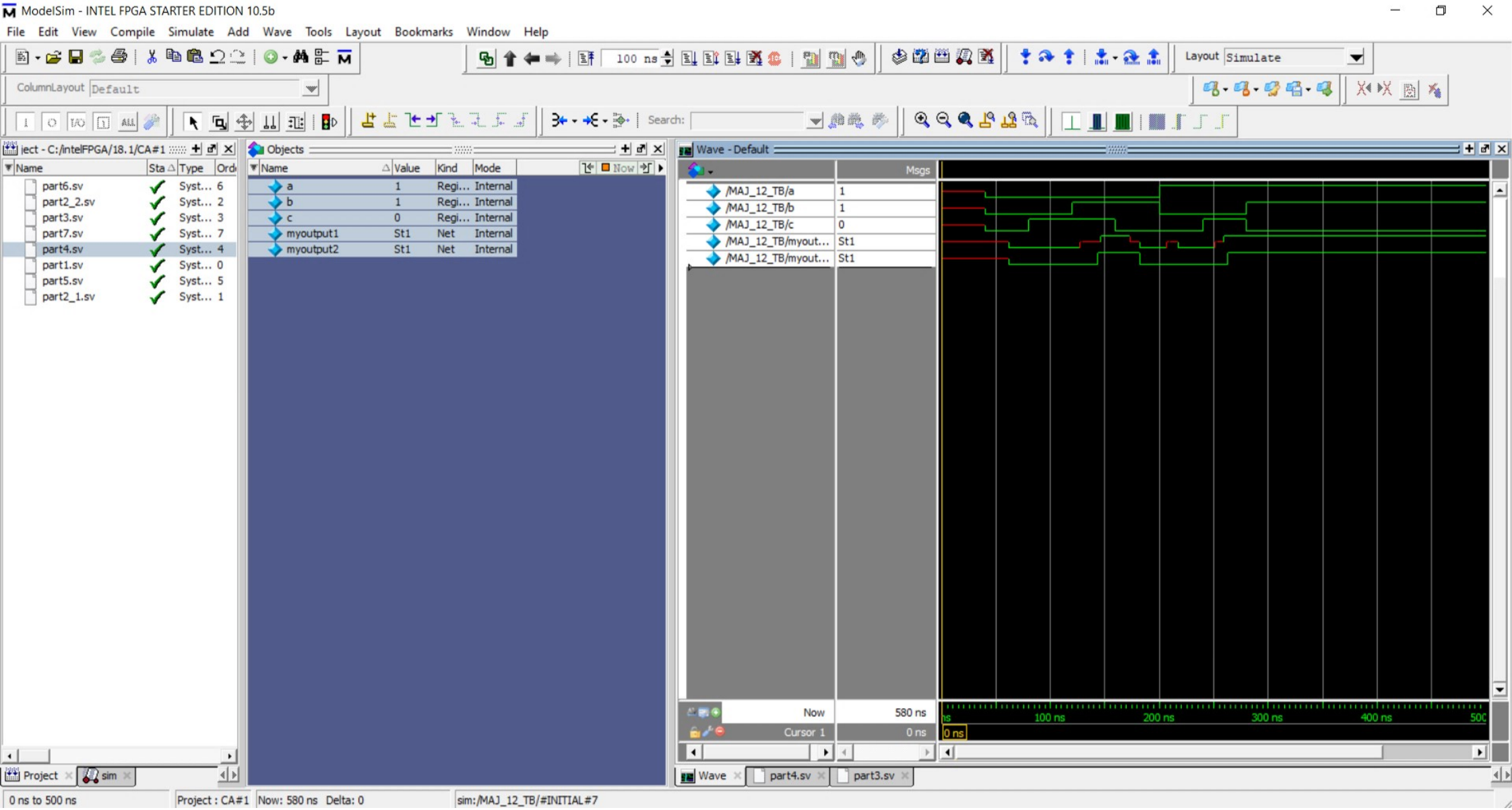
C:/intelFPGA/18.1/part3.sv - Default

Ln#

Dock/Undock

```
1  `timescale 1ns/1ns
2  module MAJ_NAND2(input a,b,c,output w);
3  wire j1,j2,j3,j4;
4  nand #(10,8)m1(j1,a,b);
5  nand #(10,8)m2(j2,a,c);
6  nand #(10,8)m3(j3,b,c);
7  nand #(15,12)m4(w,j1,j2,j3);
8  endmodule
9  module MAJ_2_TB();
10 logic a,b,c;
11 wire myoutput;
12 MAJ_NAND2 tabe2(a,b,c,myoutput);
13 initial begin
14 #40  a=0;b=0;c=0;
15 #40  c=1;
16 #40  b=1;
17 #40  c=0;
18 #40  a=1;b=0;c=0;
19 #40  c=1;
20 #40  c=0;b=1;
21 #300 $stop;
22 end
23 endmodule
24
25
```


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Objects
Name Value Kind Mode
a 1 Regi... Internal
b 1 Regi... Internal
c 0 Regi... Internal
myoutput St1 Net Internal
Wave - Default
Msgs
/MAJ_2_TB/a 1
/MAJ_2_TB/b 1
/MAJ_2_TB/c 0
/MAJ_2_TB/myoutput St1
Now 580 ns
Cursor 1 0 ns
100 ns
200 ns
300 ns
400 ns
Dock/Undock
Project
sim
Wave
part4.sv
part3.sv
Project : CA#1
Now: 580 ns Delta: 0
sim:/MAJ_2_TB/#INITIAL#13

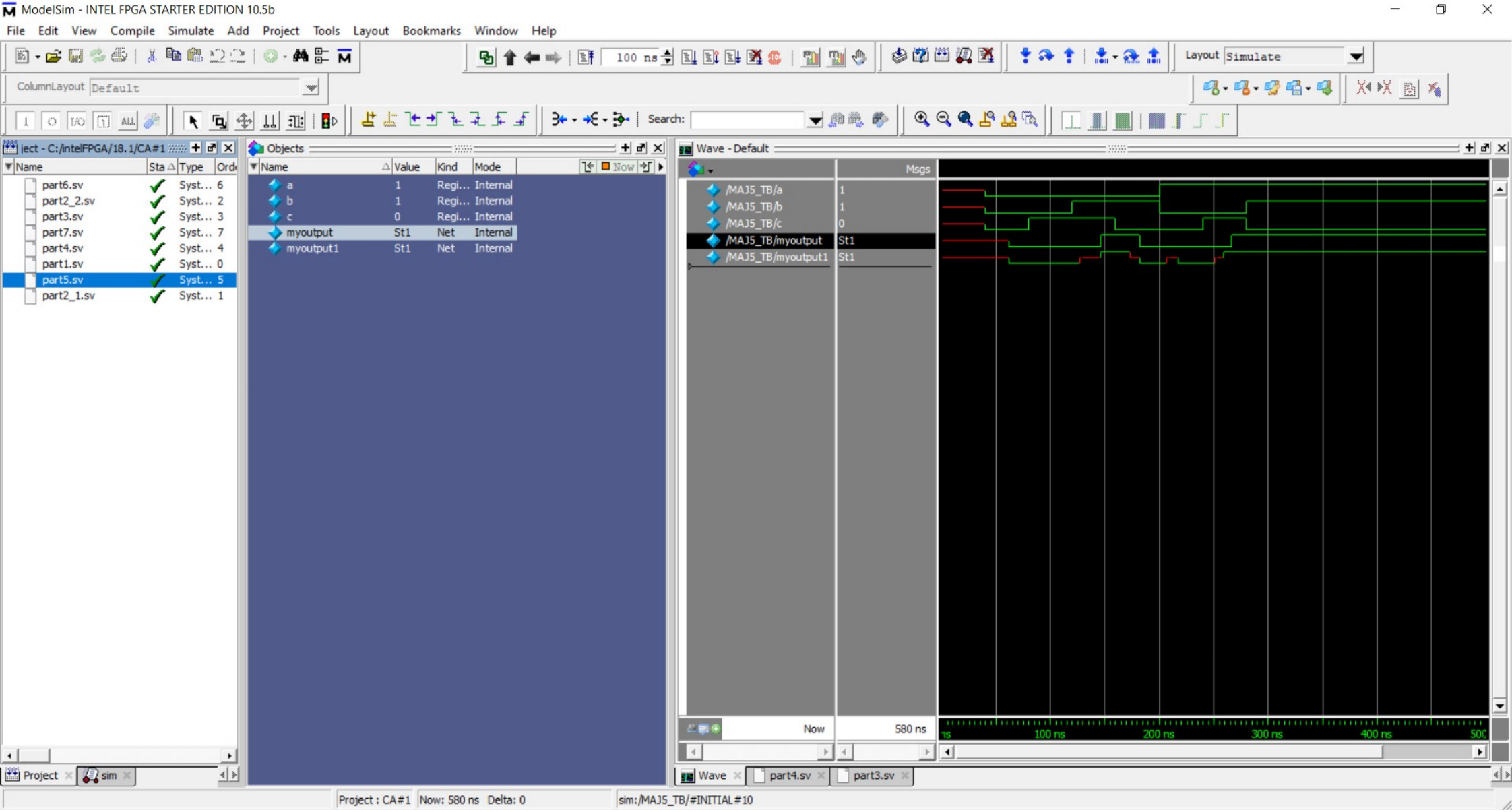

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
ject - C:/intelFPGA/18.1/CA#1
Name Sta Type Ord
part6.sv Syst... 6
part2_2.sv Syst... 2
part3.sv Syst... 3
part7.sv Syst... 7
part4.sv Syst... 4
part1.sv Syst... 0
part5.sv Syst... 5
part2_1.sv Syst... 1
Objects
Name Value Kind Mode
a 1 Regi... Internal
b 1 Regi... Internal
c 0 Regi... Internal
myoutput1 St1 Net Internal
myoutput2 St1 Net Internal
Wave - Default
Msgs
/MAJ_12_TB/a 1
/MAJ_12_TB/b 1
/MAJ_12_TB/c 0
/MAJ_12_TB/myout... St1
/MAJ_12_TB/myout... St1
Now 580 ns
Cursor 1 0 ns
100 ns 200 ns 300 ns 400 ns
0 ns
Project sim
Wave part4.sv part3.sv
0 ns to 500 ns
Project : CA#1
Now: 580 ns Delta: 0
sim:/MAJ_12_TB/#INITIAL#7

C:/intelFPGA/18.1/part4.sv - Default

```
1  `timescale 1ns/1ns
2  module MAJ_12_TB();
3  logic a,b,c;
4  wire myoutput1,myoutput2;
5  MAJ_NAND2 tabe2(a,b,c,myoutput2);
6  MAJ tabe1(a,b,c,myoutput1);
7  initial begin
8  #40  a=0;b=0;c=0;
9  #40  c=1;
10 #40  b=1;
11 #40  c=0;
12 #40  a=1;b=0;c=0;
13 #40  c=1;
14 #40  c=0;b=1;
15 #300 $stop;
16 end
17 endmodule
18
```

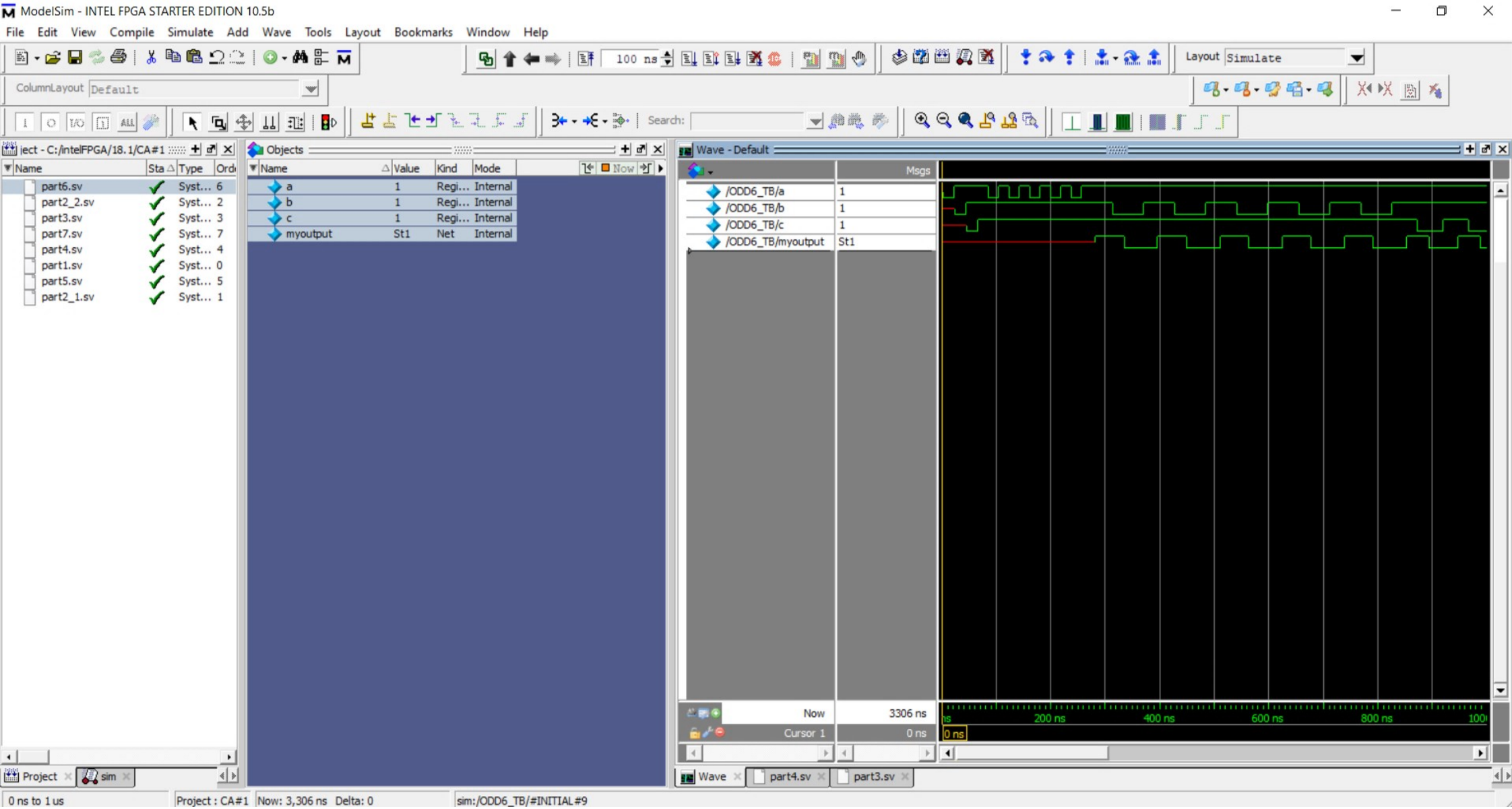
C:/intelFPGA/18.1/part5.sv - Default

```
Ln#
 1  `timescale 1ns/1ns
 2  module MAJ5 #(parameter d0to1,d1to0)(input a,b,c , output w);
 3  assign #(d0to1,d1to0) w=(a&b|b&c|a&c);
 4  endmodule
 5  module MAJ5_TB();
 6  logic a,b,c;
 7  wire myoutput,myoutput1;
 8  MAJ5 #(26,22) tabe(a,b,c,myoutput);
 9  MAJ tabe1(a,b,c,myoutput1);
10  initial begin
11  #40  a=0;b=0;c=0;
12  #40  c=1;
13  #40  b=1;
14  #40  c=0;
15  #40  a=1;b=0;c=0;
16  #40  c=1;
17  #40  c=0;b=1;
18  #300 $stop;
19  end
20  endmodule
```


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
Objects
Name Value Kind Mode
a 1 Regi... Internal
b 1 Regi... Internal
c 0 Regi... Internal
myoutput St1 Net Internal
myoutput1 St1 Net Internal
Wave - Default
Msgs
/MAJ5_TB/a 1
/MAJ5_TB/b 1
/MAJ5_TB/c 0
/MAJ5_TB/myoutput St1
/MAJ5_TB/myoutput1 St1
Now 580 ns
100 ns 200 ns 300 ns 400 ns
part6.sv Syst... 6
part2_2.sv Syst... 2
part3.sv Syst... 3
part7.sv Syst... 7
part4.sv Syst... 4
part1.sv Syst... 0
part5.sv Syst... 5
part2_1.sv Syst... 1
Project sim
Wave part4.sv part3.sv
Project : CA#1 Now: 580 ns Delta: 0
sim:/MAJ5_TB/#INITIAL#10

C:/intelFPGA/18.1/part6.sv - Default

```
Ln#
 1  `timescale 1ns/1ns
 2  module ODD6 #(parameter d0to1,d1to0)(input a,b,c,output w);
 3  assign #(d0to1,d1to0) w=(a^b^c);
 4  endmodule
 5  module ODD6_TB();
 6  logic a,b,c;
 7  wire myoutput;
 8  ODD6 #(26,22) tabe2(a,b,c,myoutput);
 9  initial begin
10  #2  a=0;
11  #20 a=1;
12  #2  b=0;
13  #20 b=1;
14  #2  c=0;
15  #20 c=1;
16  repeat(10)#19 a=~a;
17  repeat(10)#57 b=~b;
18  repeat(10)#47 c=~c;
19  #2010 $stop;
20  end
21  endmodule
22
23
```

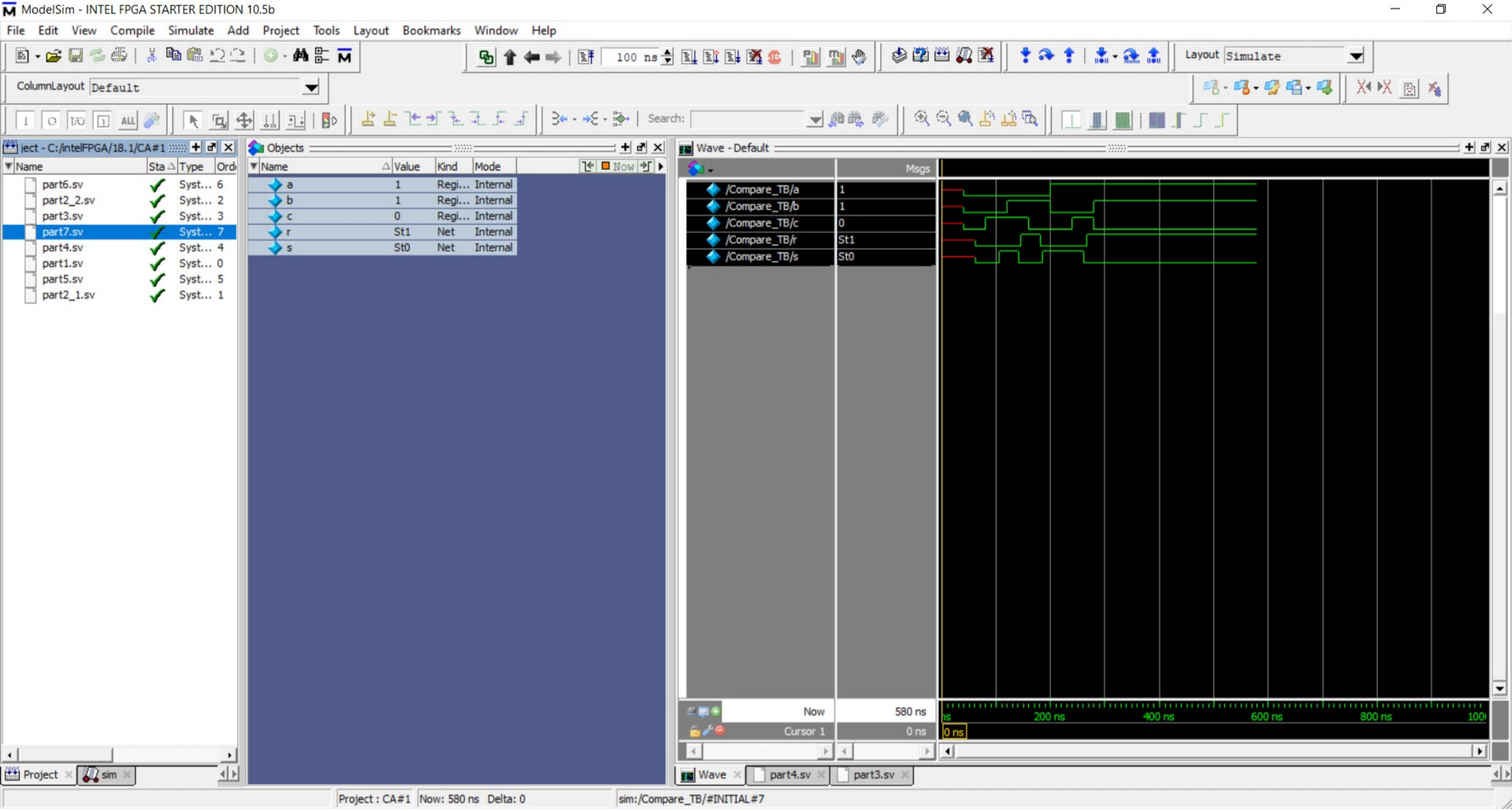

ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout Default
Search:
ject - C:/intelFPGA/18.1/CA#1
Name Sta Type Ord
part6.sv Syst... 6
part2_2.sv Syst... 2
part3.sv Syst... 3
part7.sv Syst... 7
part4.sv Syst... 4
part1.sv Syst... 0
part5.sv Syst... 5
part2_1.sv Syst... 1
Objects
Name Value Kind Mode
a 1 Regi... Internal
b 1 Regi... Internal
c 1 Regi... Internal
myoutput St1 Net Internal
Wave - Default
Msgs
/ODD6_TB/a 1
/ODD6_TB/b 1
/ODD6_TB/c 1
/ODD6_TB/myoutput St1
Now 3306 ns
Cursor 1 0 ns
200 ns
400 ns
600 ns
800 ns
0 ns
Project
sim
Wave
part4.sv
part3.sv
0 ns to 1 us
Project : CA#1
Now: 3,306 ns Delta: 0
sim:/ODD6_TB/#INITIAL#9

C:/intelFPGA/18.1/part7.sv (/Compare_TB) - Default

Ln#

```
1  `timescale 1ns/1ns
2  module Compare_TB();
3  logic a,b,c;
4  wire r,s;
5  MAJ5 #(26,22) tabel(a,b,c,r);
6  ODD6 #(26,22) tabe2(a,b,c,s);
7  initial begin
8  #40  a=0;b=0;c=0;
9  #40  c=1;
10 #40  b=1;
11 #40  c=0;
12 #40  a=1;b=0;c=0;
13 #40  c=1;
14 #40  c=0;b=1;
15 #300 $stop;
16 end
17 endmodule
18
```

Ln: 1 Col: 0


ModelSim - INTEL FPGA STARTER EDITION 10.5b
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
100 ns
Layout Simulate
ColumnLayout Default
Search:
ject - C:/intelFPGA/18.1/CA#1
Name Sta Type Ord
part6.sv Syst... 6
part2_2.sv Syst... 2
part3.sv Syst... 3
part7.sv Syst... 7
part4.sv Syst... 4
part1.sv Syst... 0
part5.sv Syst... 5
part2_1.sv Syst... 1
Project
sim
Objects
Name Value Kind Mode
a 1 Regi... Internal
b 1 Regi... Internal
c 0 Regi... Internal
r St1 Net Internal
s St0 Net Internal
Now
Wave - Default
Msgs
/Compare_TB/a 1
/Compare_TB/b 1
/Compare_TB/c 0
/Compare_TB/r St1
/Compare_TB/s St0
Now 580 ns
Cursor 1 0 ns
200 ns
400 ns
600 ns
800 ns
0 ns
Wave
part4.sv
part3.sv
Project : CA#1
Now: 580 ns Delta: 0
sim:/Compare_TB/#INITIAL#7