UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367, Spring 1398-99

Computer Assignment 3

Week 12

Latches and Flip-flops

Name:	**Date:**
Username:	

1. Generate a clocked SR-latch with four NAND gates. Use Verilog for describing this circuit. Use approximate gate delays that are based on switch level delays of 4 NS for the NMOS and 6 NS for the PMOS transistors. Apply simultaneous active high inputs (S and R) and see the loss of memory.
2. Use an inverter to convert the SR latch of Part 1 to a clocked D-latch.
3. Simulate your circuits of Part 2 to verify its operation.
4. Show the design of an 8-bit binary down-counter (paper design) with an active high enable input.
5. Use the latch of Part 2 to build the counter of Part 4. Write SystemVerilog description using a **generate** statement.
6. Simulate the circuit of Part 5 and see how it operates.
7. Use two D-latches of Part 2 build a master-slave D-type flip-flop.
8. Create a synchronous reset for the flip-flop of Part 7 such that when this input becomes 1, the output becomes 0 with the clock. Write a SystemVerilog module. Simulate this circuit to verify its operation and its resetting.
9. Use the flip-flop of Part 8 for the implementation of the counter of Part 4. Write SystemVerilog description using a **generate** statement.
10. Simulate the circuit of Part 9 and see how it operates. In a testbench show how the operation of circuits of Parts 9 and 5 differ.