UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design, ECE 367, Spring 1398-99

Computer Assignment 4

Week 12

Latches and Flip-flops

Name:	**Date:**
Username:	

1. Show the design of a Residue-7 circuit using basic gates. For the gates of this circuit use approximate gate delays that are based on switch level delays of 4 NS for the NMOS and 6 NS for the PMOS transistors. Now write a behavioral description of the Residure-7 circuit and apply your worst-case delay values to this description. Simulate and verify the operation of this circuit.

2. Write SystemVerilog description of a 3-bit D register with load enable, rising-edge clock, and an asynchronous reset. Estimate clock-to-output delay based on delays given in the above problem. Use an always statement for describing this circuit. Simulate and verify the operation of this circuit.

3. Write SystemVerilog description of a modulo-8 binary up-counter with count enable, rising-edge clock, an asynchronous reset, and a carry-out. Estimate clock-to-output delay based on delays given in Problem 1. Use an always statement for describing this circuit. Simulate and verify the operation of this circuit.

4. A 48-bit Residue-7 circuit is to be designed. The 48-bits of data for this circuit come in 6-bit chunks, where each chunk is received synchronous with a clock edge. When the eight chucks are starting, aa start signal becomes 1 and remains 1 for the 8-clock cycle duration. The Residue-7 of the 48 data bits becomes ready after start becomes 0. Note that the circuit must be reset before a new calculation begins. A ready signal indicates that the result of the 48 bits of data is ready. Build this circuit using components of Parts 1, 2 and 3. Write SystemVerilog description of this circuit by instantiating the corresponding components.

5. Write a testbench for Part 4 and test the complete operation of this circuit.