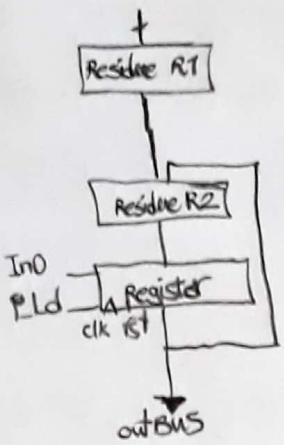
Date: 99/1/17 | CA-Report 5 | Mohammad Heydari 810197494

Dr. Navabi

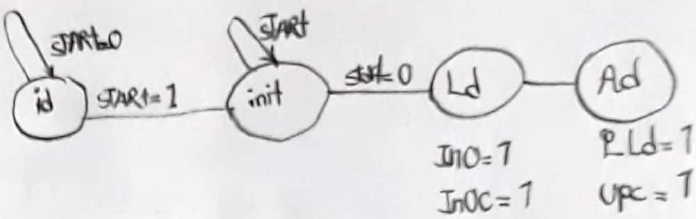
Q1) inBus ⇒ 6bit

A)

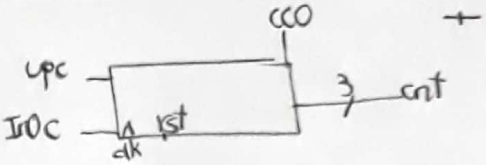


* Datapath of the SSR7 *

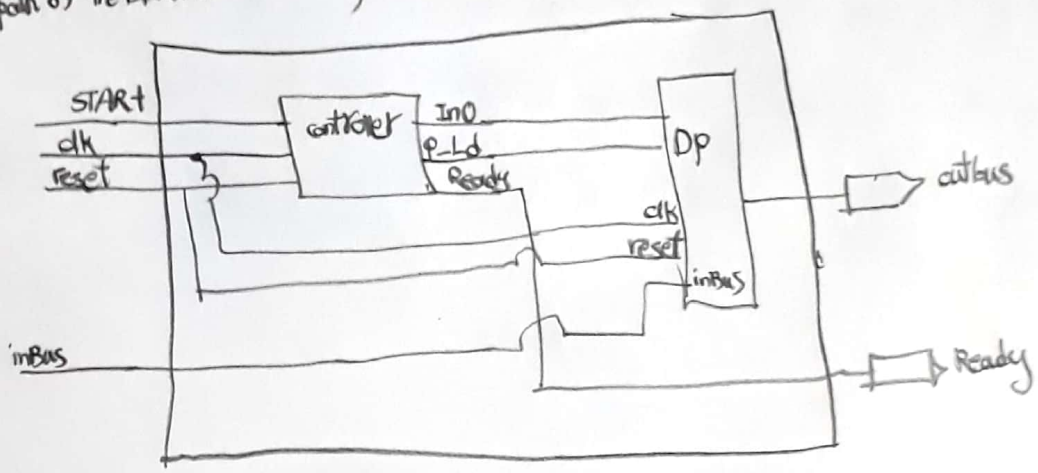
B)



* controller of the SSR7 *



c)



* The schematic of whole SSR7 *

Q2) as you see based on the Top-level design I generated the systemverilog code of the SSR7 as you see in Top design I have a datapath includes 2 residue + 1 register in this part I have just made a relation between the various module of residue and register. for initial state I have a InO to drive output to zero and make sure that I never faced up with the 'z' or 'x' value and also I have a P_Ld signal to load R2 into output. I use behavioral mode of code and only use from always statements. in addition I generated a controller with signals such as Ready and start and also InO, InOc, upc that all of that make a module called controller it maked just like the statemachine as you saw in part 1 and with case statement and always statement I handle the various states. in the last part I instantiated 2 module in one module called SS that covers both of Dp and controller.

* all of my code attached in my zip files

(23) in this part every 8 chunks bring synchronous with 8 clock and given to the input manually according to the question after instantiate of my module and define the input and output I declared my SS module with inputs and outputs. in This part I use for statement to handle the driving chunks and also use repeat to generate clockpulse and also use $random to gain random variable in my code upper steps repeated 4 Times to show that my code defenitly work correctly

(24) in This part I synthesize my code into a system verilog HDL file and after that I creat the derise of S,SR7 and study all of the reports and all of that will be attached. in second part of Qustion 4 I investigate the various type of "views" such as RTL and Technology and etc in This part I will attached all of my results in zip files