d.norabi
date → 1399/2/26

CA3-report

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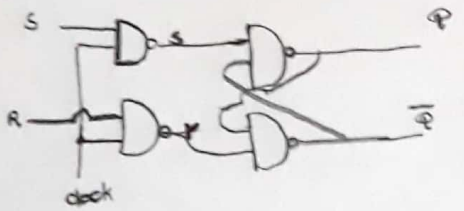
Q1)



* design of a SR-latch *

as we know we have 4 nands with 2 inputs Then we calculate the delay of nand from the cmos structure of Transsister.

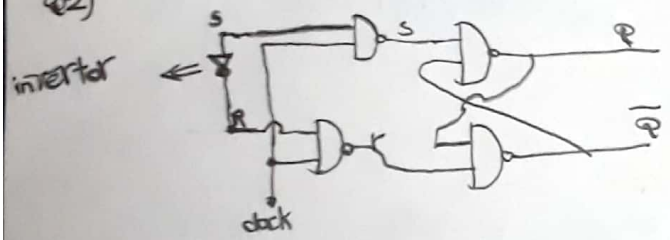
⇒ 2-nand → To 0 ⇒ 8ns
→ To 1 ⇒ 8ns

in my code I define two wires s&r and Then I drive the inputs of 4 nands. also we have two input → S, R and two outputs named Q & QB . in my code I define an input named clock

accordings to the question in my testbench after 1 cycle of S And R ; we give 1,1 to the inputs of S & R

to see memory loss

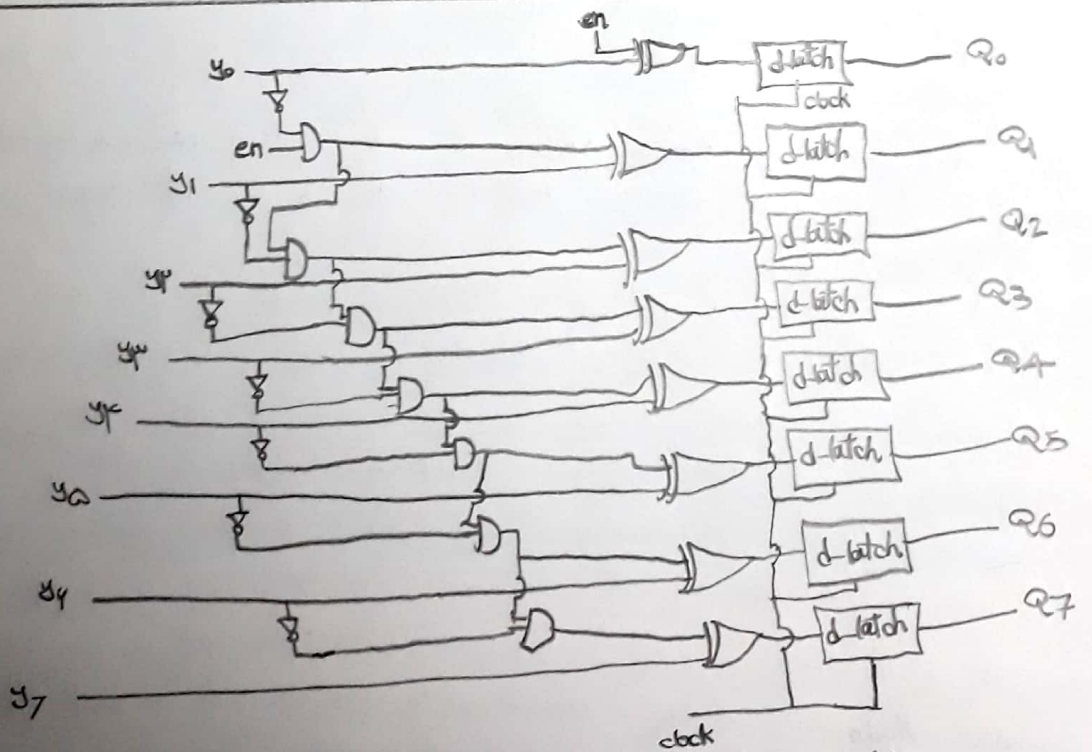
Q2)



⇒ a clocked d-latch

Q3) in This part I use a SR-loch of part 1 and with instatiate that and using not gate make a d-latch after that i make a test bench to Testing the operation of circuit. The operation with wave accepted and screenshot attached.

Q4)



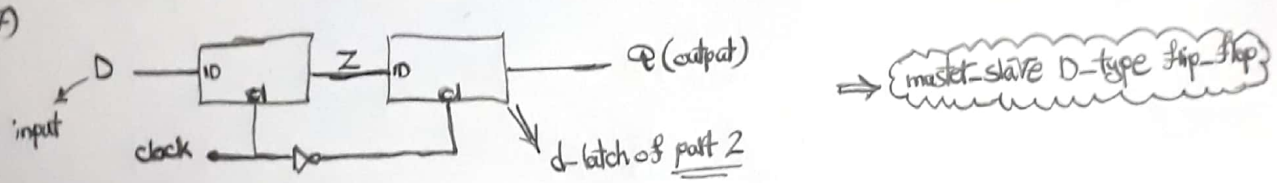
*design of down counter * with active high enable

Q5) in This part with the generate statement and also using the design of part 4 I make a code that gets input Y and clock and reset and deincrements Y and put it in output Q.

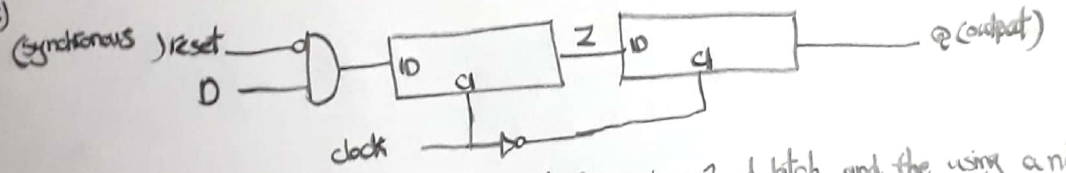
the code attached in finaly file.

Q6) in this part I defin the input & output such as ⇒ clock-reset_en, D , output ⇒ Q in my testbench after that I give the initial value at the first time ⇒ clock=1, reset=1, en=1 , D=8'b11111111 after that for handling the repeation I use initial repeat in my testbench and repeat the downcounter 256 Times in The initial repeat I change the clock every 30ns and every 200ns I put the output Q in the input D for the repeation. also in the initial begin I change the value of reset from 1 to 0 after 170ns notice ⇒ the downcounter work for suitable length of the clock as we done and handle in my code after that in The wave we see that after each clock the input deincrements and pass to the output for the repeation. and also we knows that This down-counter dont work correctly in all of time cause of using d-latch in the design and This structure has Transparency for eliminate that I use flip flop instead of d-latch.

Q7)



Q8)



in This part, first I with system verilog of a flip flop using 2-d-latch and the using a not and a and gate design a synchronous reset for circuit as the question mention it. Then when { reset=0 ⟶ Q=Q ; reset=1 ⟶ Q=0 }

The whole code attached in my files.

Q9) in This part just like part 5 I with system verilog decribtion of a down counter with flip flop of part 8 and using generate I handle downcounter also I use many logic gates. all of that attached in my files

Q10) in This part just like part 6 I define same input such as ⇒ clock-reset_en, D and two output Q, Q1 with initial values that expected. D=8'b11111111 , D1=8'b11111111 , in a testbench I define down counter part 6 & 7 with same input and different outputs. in This case I use initial repeat to handle the repetition and cycling for having enough Time to catch steady state I determine 30ns for clock to change its value. also I put the output Q to input D after the delay that catches from my circuit cause of using complex gate and also I have a initial begin to handle the reset value. and as we see on the wave with the same input for down-counter part 9 (flip flop) we need 2 cycle of clock to drive the output and deincrementing but for down-counter part 6 (d-latch) we need 1 cycle of clock to drive the output and deincrementing because of transparency it doesn't seem usable and we prefer to have a flip-flop down-counter

all of the results attached in my files