Experiment #1 - Clock and Periodic Signal Generation

Mohammad.heydari
810197494

INTRODUCTION

In this experiment we investigate some of important basic about the clock generation ,Schmitt oscillator , duty cycle and many other things such as frequency devider , Ring oscillator and a review of T flip_flop & Jk flip_flop then we use Quartus to make a simple FPGA design , after preparing design we try to get a .vo output from FPGA and then we transfer the .vo to the modlesim where we analyse the wave.

1 CLOCK GENERATION USING ICS AND ANALOG COMPONENTS

In this part we use Ltpspise software to design Ring oscillator , Schmitt triger and also Lm555 timer then using simple analyses we obtain the requirements of the question.

1.1 Ring Oscillator

As we know The delay of logic gates is very small and this imposes a large bandwidth. So, measuring this delay directly using a relatively low-cost oscilloscope may be difficult. An alternative method for measuring this parameter is using a ring oscillator.

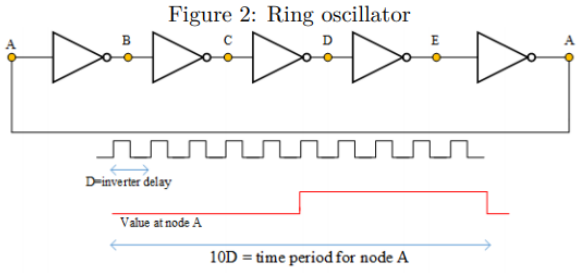


Figure 2: Ring oscillator

As you see in figure2 we design the circuit in LtPspise using 5 invertors (74HCT04).
We know that here we don't need any Vcc or Gnd source because when we talk about logic gates always we face with noise signals that cuase changing input.the effect of this issue is a current that start from left invertor and goes through the side. Then we have below circuit.

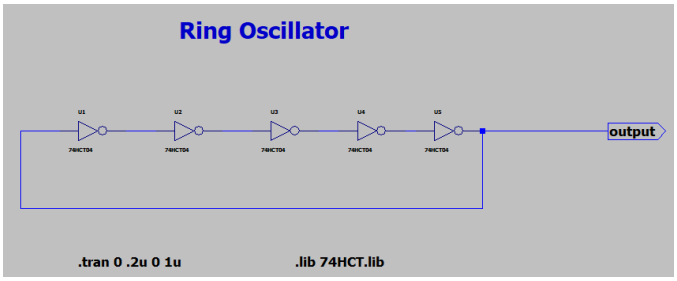


Fig. 1 Ring_oscillator circuit in Ltpspise

A ring oscillator is composed of a chain of odd number of inverters, in which output of last inverter is connected to the input of first one. It can be easily seen that adding more inverters to the chain increases the total gate delay. The time at which a value feeds back to the same node is the time period of the ring oscillator which equals $2N * Delayinv$, where N is the odd number and Delayinv is the delay of each inverter gate. The delay of each single inverter can be determined by measuring the total delay.

Questions:

1.Measure the propagation delay of the chain by measuring the period time of the output.

After simulating the circuit we can observe the period time of output easily then using cursors we can calculate the whole Period time :

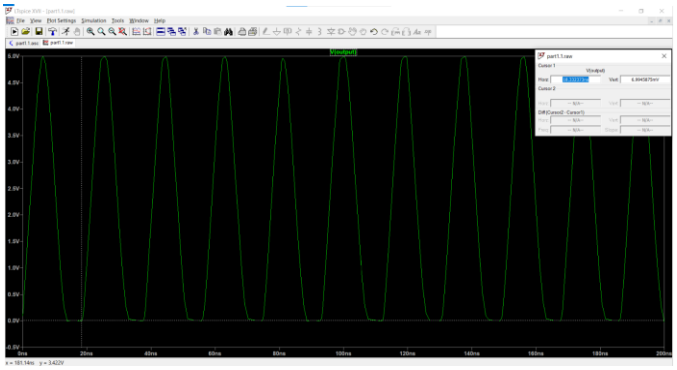


Fig. 2 Ring_oscillator output

as you see in above figure we obtain the **T=18ns**

the result don't match with datasheet that I founded in the net ☹

2.Calculate the delay of a single inverter and report this time.

Accordings to the formula that have been attached in Lab presentation we have T= 2N ∗ Delayinv

Then 18=2*5*delayinv

So Delay a single inverter =1.8ns

1.2 LM555 timer

LM555 is among the devices can be used for generating clock signal or time delays.

This IC operates in three modes: Monostable, Bistable and Astable. The astable mode that we use in this experiment allows the timer to operate as an oscillator that outputs a continuous rectangular pulse of a required frequency. For astable operation, we need two resistors and one capacitor to design a circuit that operates at the frequency required. The timing during which the output is either high or low is determined by these externally connected resistors and capacitors.

We design the below circuit with all of details in Ltpspise then many anylises must be done on the waveforms.

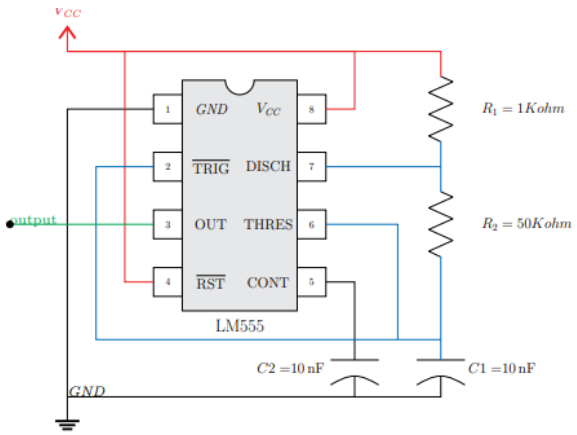


Fig. 3 LM555 timer circuit in Ltpspise

1. Implement the LM555 in astable mode using the wiring diagram from figure 4 and observe the output. Report the clock frequency and the duty cycle and include the waveform of the output in your report.

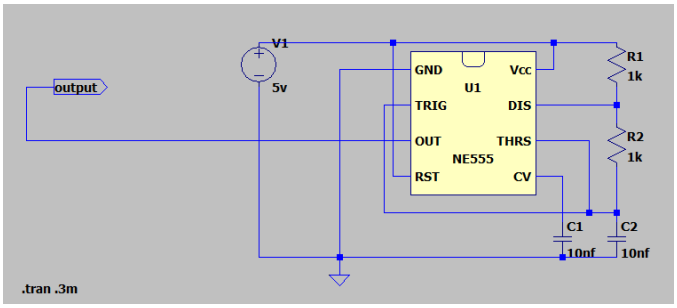


Fig. 4 LM555 timer circuit in Ltpspise

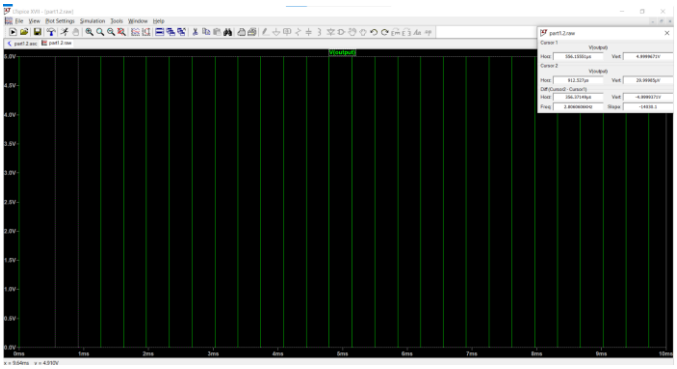


Fig. 5 LM555 timer output

As we know duty cycle equation equals to T1/T

Where the T is period of signal and T1 is times that the signal output is 1 .

Dutycycle=356us/912us = 0.4

Frequency=1/T=1.09Khz

2. Change the value of R2 resistors to produce different clock frequencies. To do so, R2 should be 1 kΩ, 10 kΩ and 100 kΩ. Calculate the frequency and duty cycle using above equations and compare them to the clock signal you see on the output.

$$T = T1 + T2 = 0.693 * (R1 + 2R2) * C$$

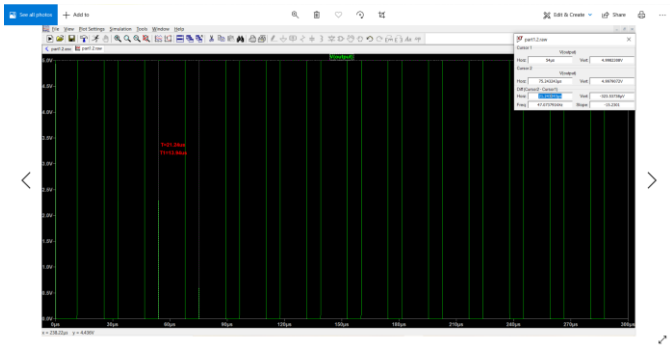


Fig. 6 R2=1k

T = T1 + T2 = 0.693 ∗ (R1 + 2R2) ∗ C
=0.693*(1+2)*10=20.79us
F=48.1 KHz

Dutycycle=13.94/21.24=0.65

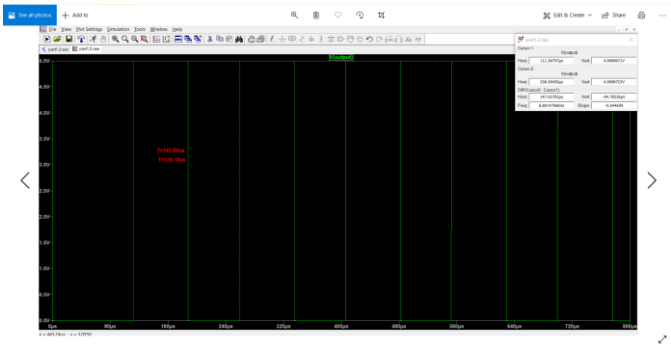


Fig. 7 R2=10k

T = T1 + T2 = 0.693 ∗ (R1 + 2R2) ∗ C
=0.693*(1+20)*10=145.5us
F=6.87 KHz

Dutycycle=76/147=0.52

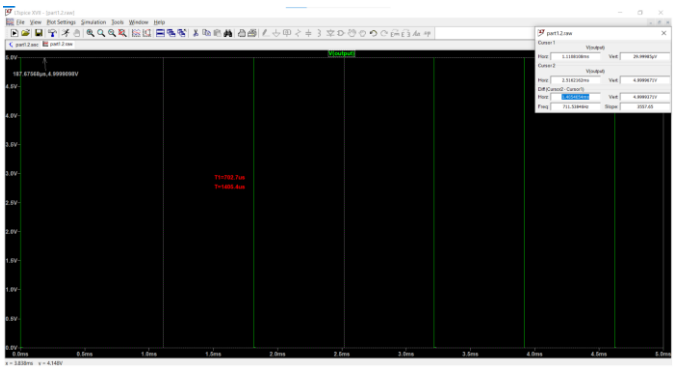


Fig. 8 R2=100k

T = T1 + T2 = 0.693 ∗ (R1 + 2R2) ∗ C
=0.693*(1+200)*10=1393us
F=717 Hz

Dutycycle=702/1405=0.5

as we see with increasing the R2 the dutycycle Wishes to 0.5

notice: as you see the frequency shown in cursor button over the figure.

1.3 Schmitt Trigger Oscillator

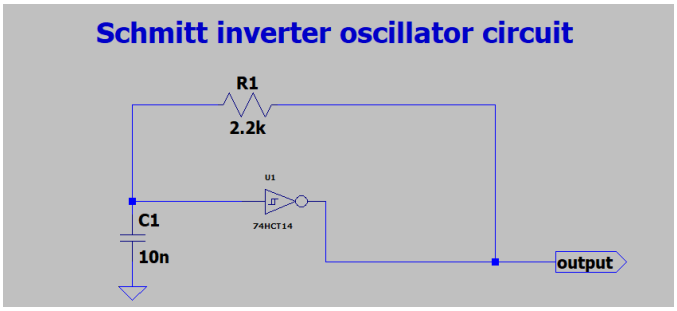


Fig. 8 Schmitt inverter occhllator circuit

In this part after designing the circuit in Ltpspsie we should obtain the value of constant a for the three different value of R.

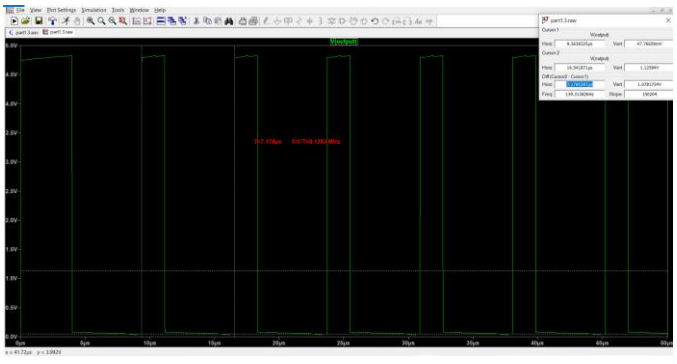


Fig. 9 R1=1k

a=R*C*f=1*10*0.139=13.9

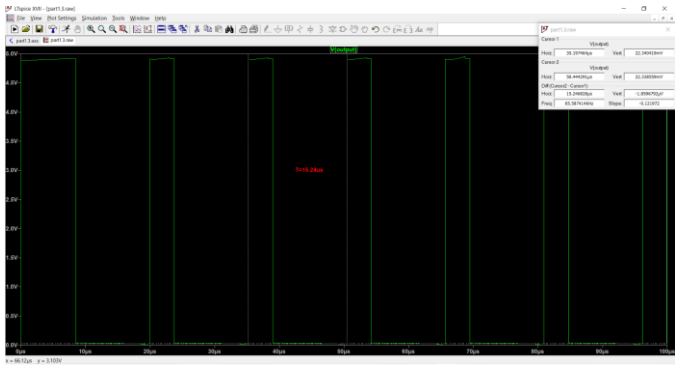


Fig. 10 R1=2.2k

a=R*C*f=2.2*10*0.065=1.43

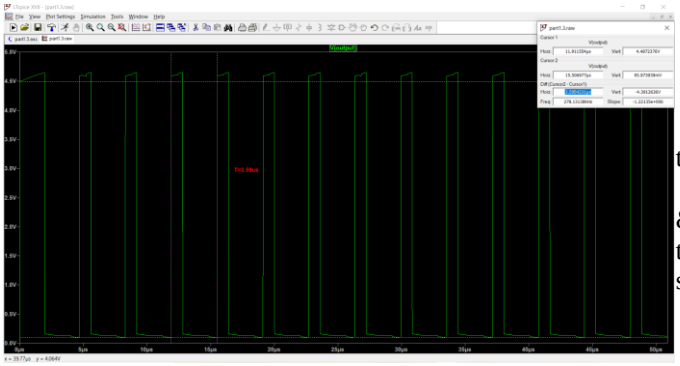


Fig. 11 R1=470

a=R*C*f=0.47*10*0.278=1.31

as we see the value of a constant approximately are the same .

2 Clock Generation using Verilog HDL

in this part we are going to generating clock using Verilog Hdl in modlesim. In this section we can simply use Verilog delay expressions, for setting the ON and OFF duration of the clock pulse. This kind of modeling cannot be synthesized in the synthesis tool but can be simulated in Modelsim which is proper enough for debugging our design.

1. Before simulating the design, first read the code completely and understand whats going on.

In first step we calculate the T1 & T0 duration of the pulse based on equation in part 1.2 , then we need 2 parameters to save the integer delays so using Logarithm we catch the number of bits require to count up and achiving the time delay.

After that we need 2 counters to count up as a fact the Verilog code has 2 parts including sequential & combinantial.

In sequential part we define enable signal with an if statement that activate when we wanna make positive pulse.

Before simulating the design, draw a block diagram of the design in your report and explain the hardware and the functionality.(you need hand drawing block diagram.)

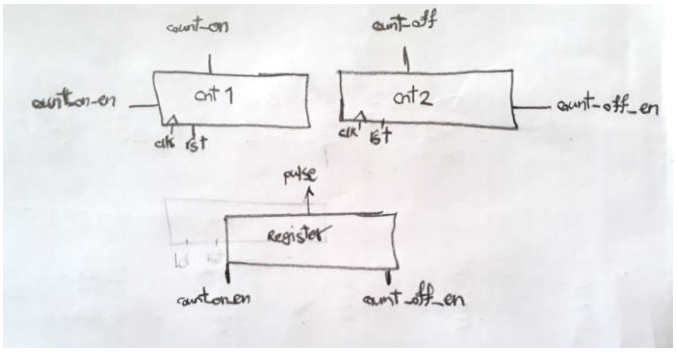


Fig. 12 datapath of timer.v

We have two counter with an enable signal that issue when the onduration & offduration have not been completed.

When the counters count exatly values of period such as T1 &T0 the assign statement which is make enale signal force that to gets 0 value after that the counters stop and the rst signal activate and the circuit gets steady state.

3. To verify this design, write a simple testbench. Make an instance of the design in the testbench and test the design by providing the parameters.

In this part will be attached completely with all details.

4. Measure the duty cycle of this circuit by setting resistor values of section 1.2 and include the waveforms of the inputs and outputs in your report.Are the results of this two sections completely matched? Explain the reason if not.

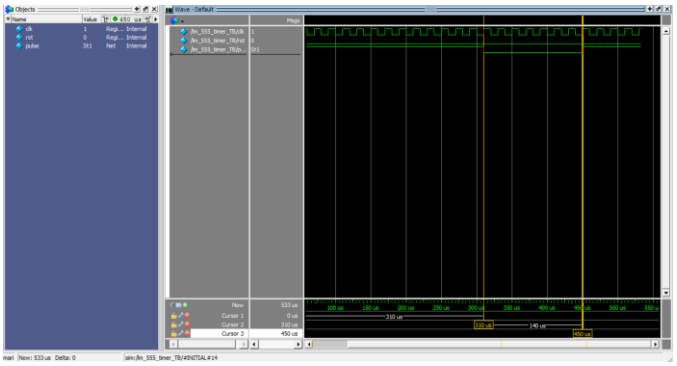


Fig. 13 timer.v with R2=1k

Dutycycle=310us/450us=0.68

The result matches with the part 1.2 but the lengh of periods are different which is due to truncating calculated values for on- and off-duration.

5. One of the alternative methods for writing this design is using from delay statements. Write the design with delay statements and run the results in Modelsim. Show the waveforms and duty cycles for this method.

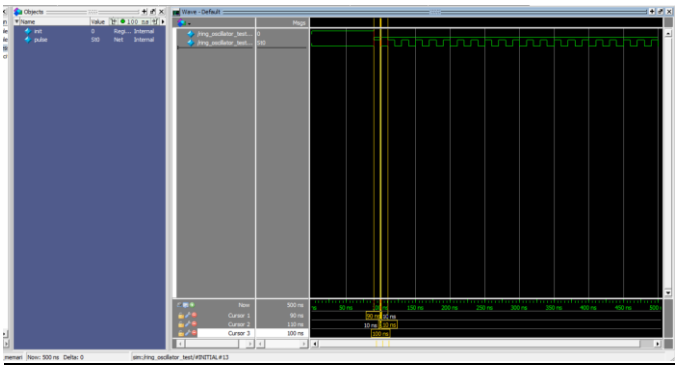
In this part as same the privous part we change a bit in the structure of the code and generate a new code with delay statement and only thing must be handle is correct use of #() for assign the delay to handle the waves.

The code has been attached.

3 FPGA Design

3.1 Ring Oscillator

All of codes and TB has been attached in zip file.
And scrrenshot are available in my final zip



3.2 Synchronous Counter as a Frequency Divider

In this part we are going to wiring many of blocks in the qaurtus software to make a frequency divider.

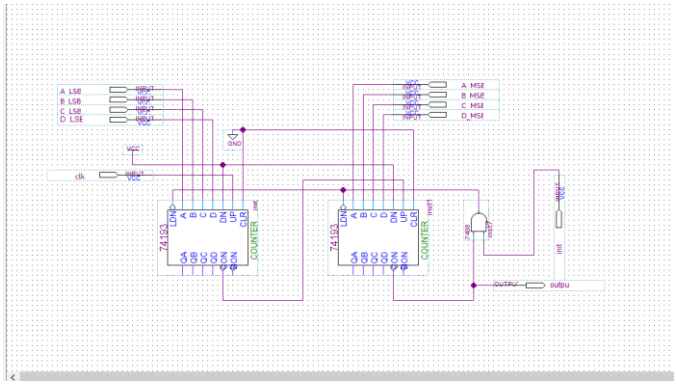


Fig. 14 frequency_divider without T_flip_flop

In this part and the next part we wanna make a frequency divider but in 3.2 we don't use Jkflipflop on the output but in part 3.3 & 3.4 we wire the block with adding display.v (after creat symbol) to the module and after that synthesis the block and gets a .vo file from qaurtus .

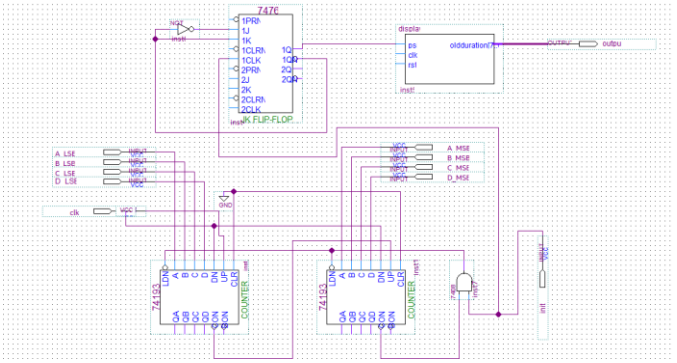


Fig. 15 frequency_divider T_flip_flop

all of the result with calculations will be attached in screenshots Folder.

CONCLUSIONS

In this ecxperiment we have studied different approaches of producing a periodic signal which is stable enough to be used as a continuous clock input of a synchronous circuit. And also we learn how to use Verilog language to make a clock generation Timer and also Ring oscillator that is one of the most important basic points to start working with Logic circuit.

Finally we investigate frequency divider and use the qaurtus to synthesis the circuit. And the effect of Jkflipflop to handle dutycycle.

REFERENCES

[1] Some entries at github

[2] Some entries at stackoverflow.com

[3] https://www.google.com/url?sa=t&source=web&rct=j&url=https://www.diodes.com/assets/Datasheets/74HCT04.pdf&ved=2ahUKEwjlm_LhjoTtAhWXQhUIHXrpAc4QFjAAegQIAxAB&usg=AOvVaw0RlOslRmXsgJTYBH_sFTXQ&cshid=1605428401733

[4] Datesheets of 74HCT04