Experiment #1 - Clock and Periodic Signal Generation

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***Abstract*: In this experiment, we are going to introduce ways of clock generating. There are many ways to do so. For simulating clock signals we have two main segments. To do analog generation we use LTspice XVII. Then we use Verilog HDL and Quartus for FPGA designing. For calculating frequencies, we use waveform analysis. Then base on observations, we compare them to find out new results.**

***Keywords*:** clock, frequency, delay

I. Clock Generation using ICs and Analog components

In this part, we simulate circuits using LTspice. First, we design circuits and then simulate them to observe the output signals. We measure clock cycle time and frequency based on output signals.

I. RING OSCILLATOR

Based on figure 1, we designed circuit in LTspice. Based output signal we measure the propagation delay of the chain is equal to 187ns, so the delay of invertor is:
187ns/10 = 18.7ns.

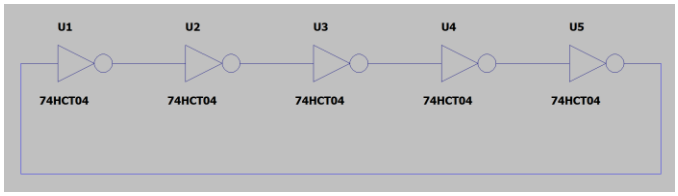

Figure1, ring oscillator design

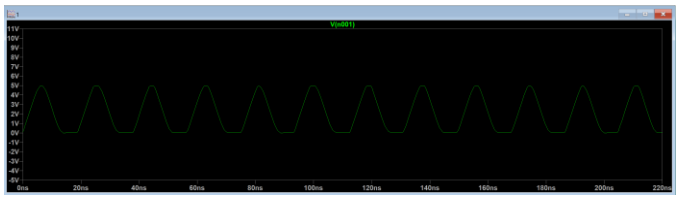

Figure2, output signal of ring oscillator

Symbol	Parameter	Guaranteed Limit			Unit
		25 °C to -55°C	≤85°C	≤125°C	
t_{PLH}	Maximum Propagation Delay, Input A	15	19	22	ns
t_{PHL}	to Output Y (Figures 1 and 2)	17	21	26	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
C_{IN}	Maximum Input Capacitance	10	10	10	pF

Figure3, 74HCT04 delay based on datasheet

II. LM555 TIMER

In this part we design LM555 in astable mode based on figure4. In this experiment, we use different resistors for R2 and observe the results. The results are shown in Table 1.

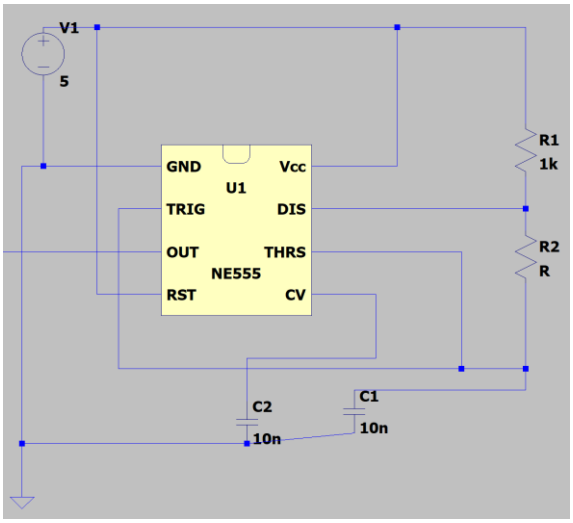

Figure4, LM555 astable mode

R2(kΩ)	Frequency(Hz)	Active high(s)	Duty cycle(%)	Waveform
100	714	1.4m	50	Figure 5
50	1428	0.7m	50	Figure 6
10	6666	0.15m	54	Figure 7
1	47619	14u	66	Figure 8

Table1, result for different resistor for LM555 based output

R2(kΩ)	Frequency(Hz)	Duty cycle(%)
100	717	50
50	1428	50
10	6871	52
1	48100	66

Table2, result for different resistor for LM555 based equations

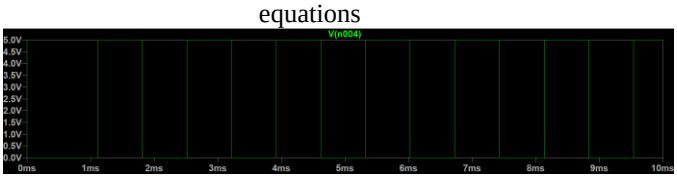

Figure5 (100 kΩ)

Figure6 (50 kΩ)

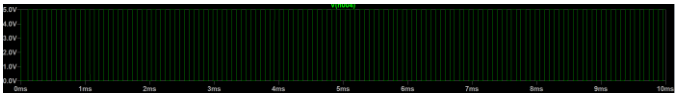

Figure7 (10 kΩ)

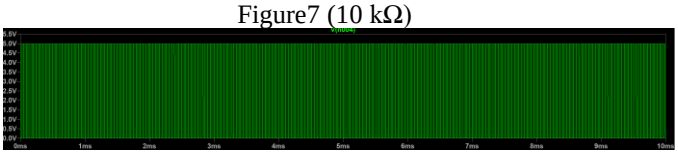

Figure8 (1 kΩ)

The difference between simulation and using equations result is for measurement error. But both of result in same order.

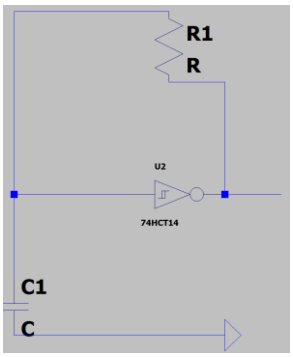

Figure9, Schmitt trigger oscillator

III. SCHMITT TRIGGER OSCILLATOR

We design circuit based on figure9 and observe outputs. Based outputs, measure the frequency and whit equation for this part, we find α parameter. Results show in table3. In all of simulations, the C is 10nf.

R(Ω)	Frequency(Hz)	α
470	277102	1.30
1000	139345	1.39
2200	65921	1.45

Table3

II. CLOCK GENERATION USING VERILOG HDL

The code describes LM555 in verilogHDL. Code using times that calculated from equations of part one. The block diagram of this component show in figure10 and figure11. We test this module whit testbench in ModelSim and observe results in outputs. Details of observation shown in table4.

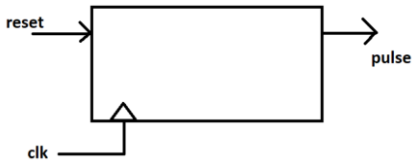

Figure10, LM555 diagram

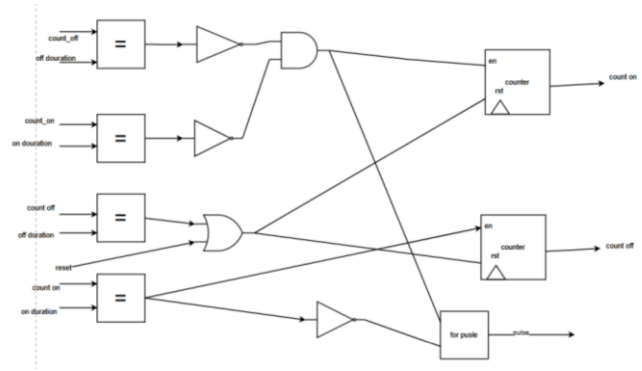

Figure11, inside LM555

R(kΩ)	Duty cycle(%)	Active high(ns)
1	66	4536
10	52	31320
100	50	300888

Table4

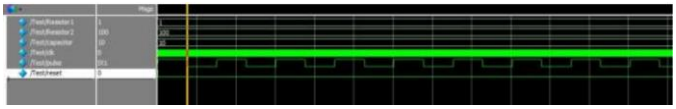

Figure12,(100 kΩ)

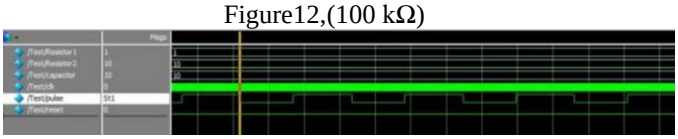

Figure 13,(10 kΩ)

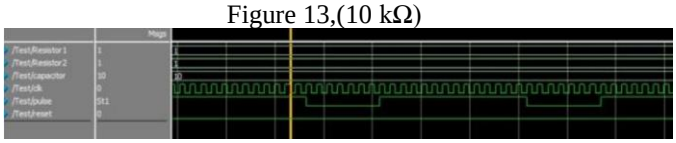

Figure14,(1 kΩ)

There are different results for R2 = 10 kΩ, because of measurement error but both of them are almost equal.
The duty cycle for the alternative methods equal to the first method and its waveform show in figure 15.

Figure 15(Altanative Lm_555)

III. FPGA Design

In this part, we use the Quartus and design diagram in this software. We will be familiar with FPGA design in this part. Then test out design with testbench in ModelSim and observe results and output signals.

I. Ring Oscillator

To describe the ring oscillator we use the generating method. It should be parametrized and we use invertor delay calculated in part one. An enable signal is provided too. Figure 16 shows the results of this part.

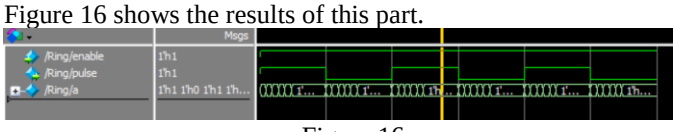

Figure 16

Results of this part equal to result of part one. The pulse time in both of parts is same.

II. SYNCHRONOUS COUNTER AS A FREQUENCY DIVIDER

In this part, we use 74LS193 from MAXPLUSE2 74 to construct a divide by 113 synchronous up-counter. But the design was given is divide by 112. First, we design this module in Quartus. This design is shown in figure18. Then we connect the ring oscillator inside testbench to this module and then test it in ModelSim and observe results and output signals. The result is shown in figure19.

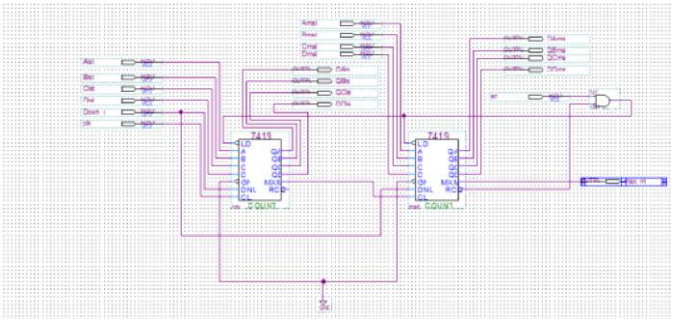

Figure 17

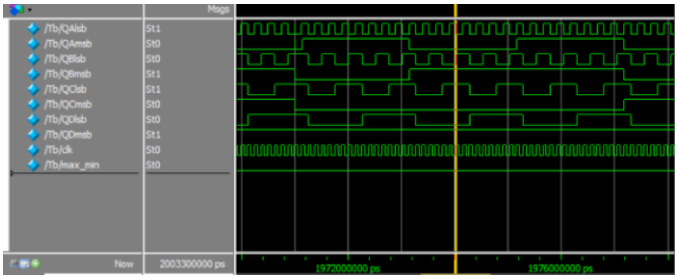

Figure 18

In this part, we run into a problem that is max_min signal doesn't change despite other signals work as expected. Therefore we can not measure the frequency. To solve this problem we use the'' QCMSB '' signal. We conclude that the output frequency is lower than the input frequency.

III. T FLIP-FLOP

We use a T Flip-Flop after counter to produce a 50 % duty cycle signal. We use 7476 IC from the MAXPLUSE2 library. 7476 is a dual D Flip-Flop that can be converted to a T Flip-Flop. Figure19 show this part design.

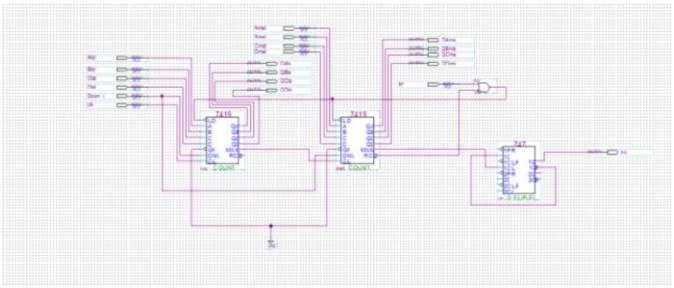

Figure 19

IV. DISPLAY MODULE IN FPGA

In this part, we should use from display code to create its symbol in Quartus and connect it to the output of the previous part to counting the number of clocks. Figure20 shows the design of this part. With the problem that was described in part 3.2 (V.2) we can't test this part and observe the output.

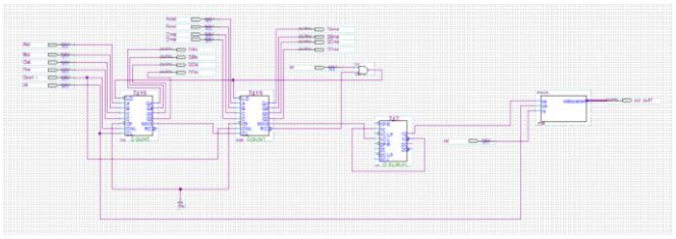

Figure 20