Experiment #2 - Frequency Regulation

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***Abstract*: Generating clock signals with specific frequency is very important in the digital system. Generating clock that its frequency is based on existing clock input is a good method for this work. The output signal(new clock signal) frequency is based on the input signal frequency and ratio that we expect.**

***Keywords*:** clock divider, frequency regulation, Frequency range specification

I. INTRODUCTION:

In this part, we simulate circuits using LTspice. First, we design circuits and then simulate them to observe the output signals. We measure clock cycle time and frequency based on output signals.

II. DESIGN DESCRIPTION AND SYNTHESIS

Figure 1 show the design of system. System consist of counter, ring oscillator, toggle (D flip-flap), and gate, inverter, preprocessing unit and frequency regulator. This system is frequency regulation and generate output based on input clock frequency and input ratio (and ring oscillator frequency). Output of this system is new clock signal, that is shown in this design with psi name. RTL design of the preprocessing unit also is shown in figure 2.

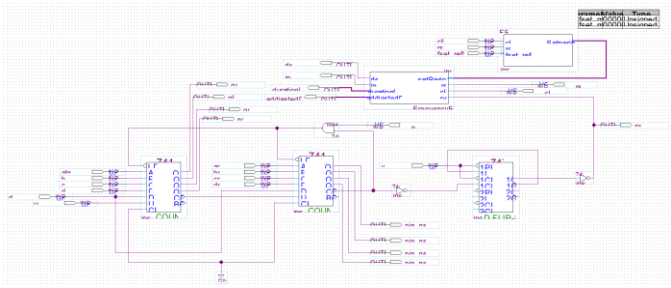

Figure1

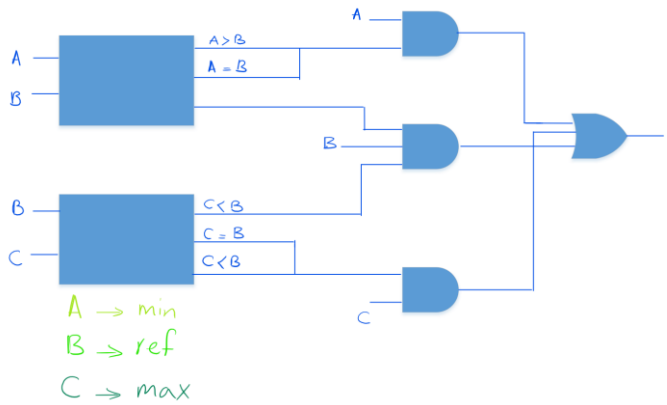

Figure2, Pre-Processing unit RTL design

x

Outputs of frequency regulator(addjastedDiv) are connected to inputs of counters in testbench code. Testbench code has been attached. Figure 3, figure 4 are shown circuit connecting and figure 5 show connecting of frequency regulator. This design has been attached (lab2.bdf file).

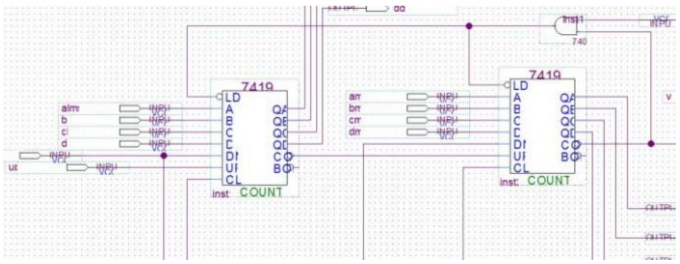

Figure 3

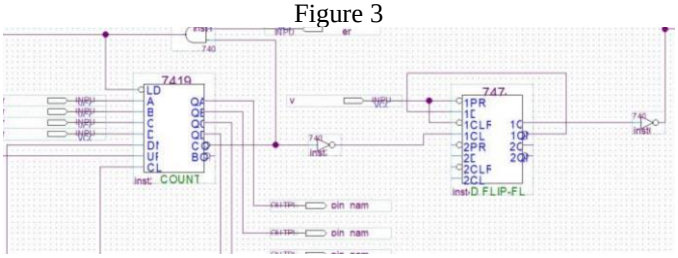

Figure 4

Figure5

III. DESIGN SIMULATION IN MODELSIM

For testing this system, we use modelsim. In our testbench, we use result of quartes (.vo file) and connected this module to ring oscillator module. In test bench we can't change ring oscillator features (inverter delay and number of them) and we are forced to use many testbench for experiment expectations. One important thing is that` when setPeriod is n, we generate output signal with 1/(2n) input clock frequency, because we compare duration with setPeriod and we count duration when psi is 1. Results that is shown below are based on this case(case1). If we want to generate clock with frequency that is 1/n input frequency, we should compare duration with setPeriod/2(case2). Table 1 show test one and output signals for this test are show in figure 5 and figure 6.

Ring oscillator frequency(MHz)	Desired frequency(kHz)	Final parallel loads	Initial parallel loads	Setperiod
20	200	205(204)	130	125

Table1

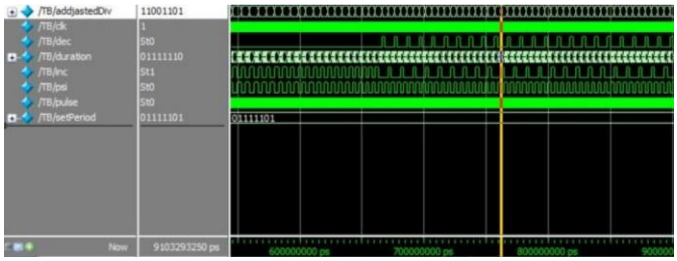

Figure6

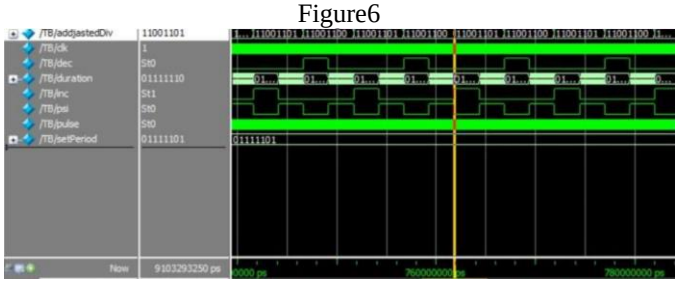

Figure7

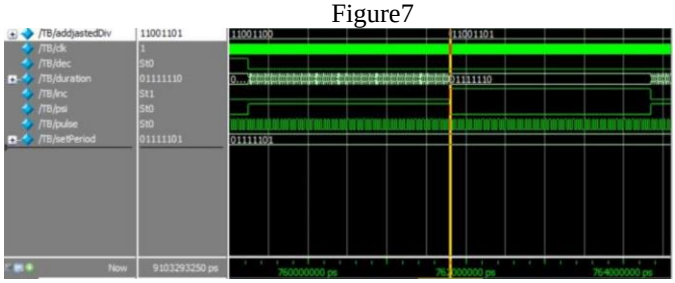

Figure8

Table 2 shows test two and output signals for this test are shown in figure 9, figure 10, and figure 11.

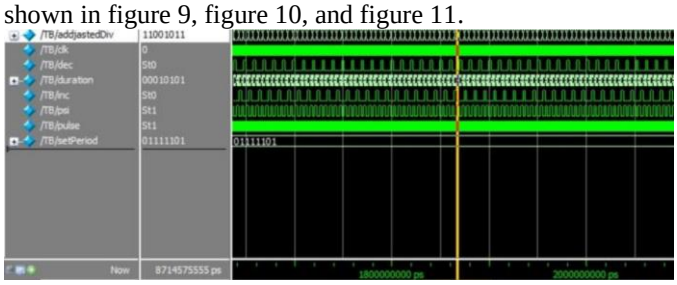

Figure 9

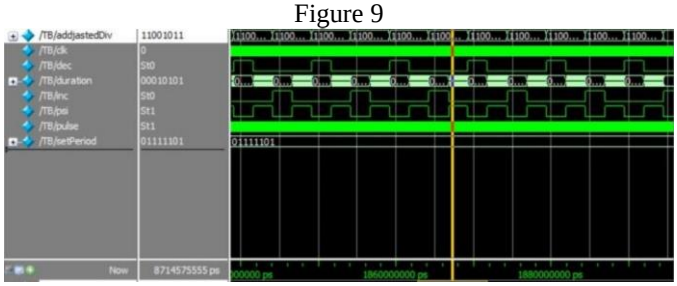

Figure10

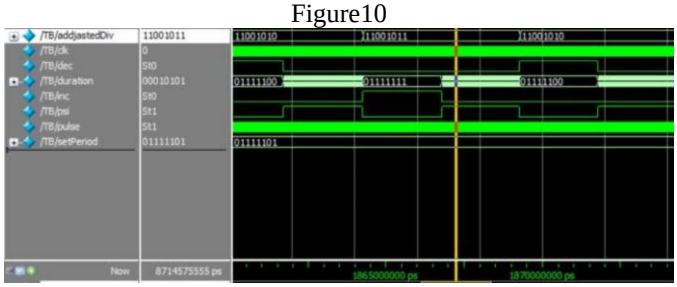

Figure11

Ring oscillator frequency(MHz)	Desired frequency(kHz)	Final parallel loads	Initial parallel loads	Setperiod
20.83	200	203(202)	130	125

Table2

Table 3 show test one and output signals for this test are show in figure 12, figure 13 and figure 14.

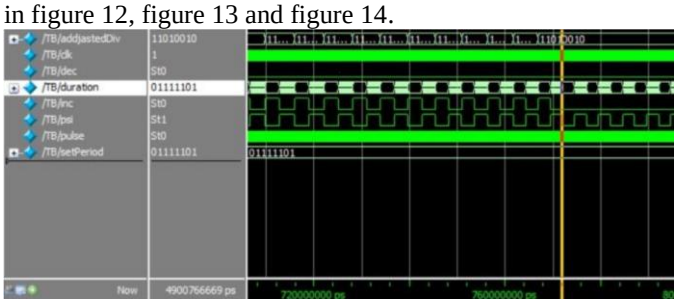

Figure12

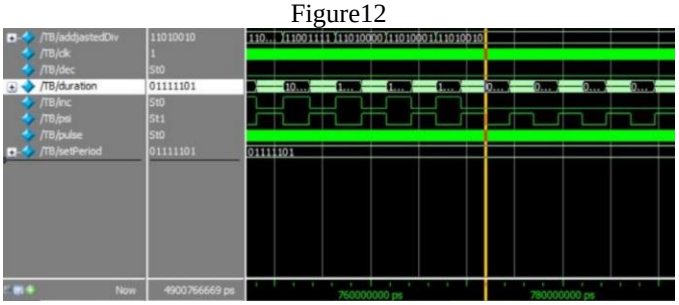

Figure13

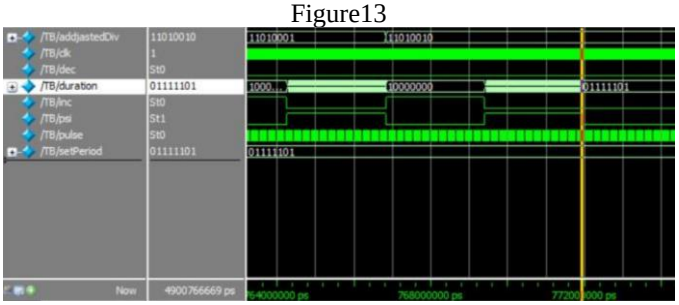

Figure14

In all test, all things are same, except ring oscillator frequency. With ring oscillator frequency changing, final parallel loads change, but desired frequency doesn't change. Because desired frequency depends on setPeriod and frequency of frequency regulator clock.