

**Faculty of Engineering and Technology**

**Department of Electrical and Computer Engineering**

ENCS 2110

Digital Electronics and Computer Organization Lab

Experiment#2 Report

**Comparators, Adders and Subtractors**

Instructor: Adnan Yahya

TA : Ibrahim Injass

Name: Mohammad raddad

ID# : 1180812

* **Abstract \ Objectives:**

This experiment is about Comparators, Adders and Subtractors,

1-To understand the construction and operating principle of digital comparators

2- To construct comparators with basic gates and ICs

3- To implement half- and full adders using basic logic gates and ICs

4-To implement a 4-bit adder unit(s)/ICs to add 4-bit numbers

5-To understand the theory of complements

6-To construct half- and full- subtractor circuits

* **The aims of the experiment:**

1. To get used to the comparator and construct it with basic gates and IC.

2. To understand the concept of half – full adder and subtractor and construct them using basic gates and IC.

* **To achieve the previous aims, I used:**

1-IT-3000 Basic Electricity Circuit Lab

2- IT-3002 Basic Gates Circuit

3- IT-3003 Adder/Subtractor Circuits

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* **Procedure & Discussion**

1. **Comparator Circuits**
   1. Constructing Comparator with Basic Logic Gates

Using a IT-3002 module block comparator 1.

As we see in figure 1 we connected A1 with F7 and F6 with B1.

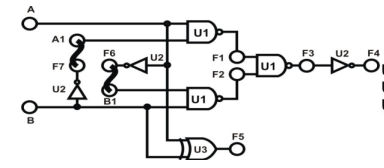


Figure 1

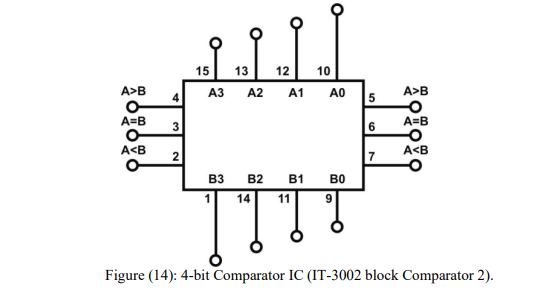
Now we will se the result of this gate

|  |  |  |
| --- | --- | --- |
| **inputs** |  | **outputs** |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Sw2 | Sw1 |  | F1 | F2 | F5 |
| 0 | 0 | A=B | 1 | 1 | 0 |
| 0 | 1 | A>B | 0 | 1 | 1 |
| 1 | 0 | A<B | 1 | 0 | 1 |
| 1 | 1 | A=B | 1 | 1 | 0 |

**2.Constructing Comparator with TTL IC:**

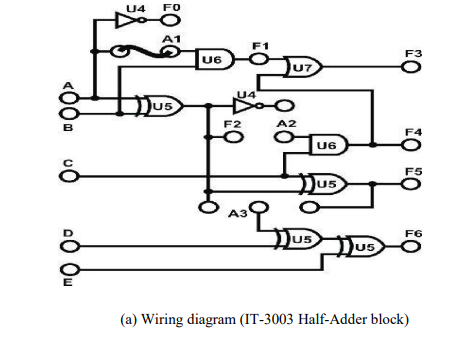
Constructing Comparator with TTL IC 1. Block (Comparator 2) of module IT-3002 will be used in this section. U5 is a 74LS85 4-bit Comparator IC shown in Figure 14.



|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **inputs** | | | **Outputs** | | |
| A>B | A=B | A<B | A>B | A=B | A<B |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 |

**3.Half- and Full-Adder Circuits**

**Half Adder:**

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Connect inputs A, B to Date Switches SW0, SW1 and connect outputs F1, F2 to logic so the output is :

|  |  |  |  |
| --- | --- | --- | --- |
| inputs | | outputs | |
| B  (Sw1) | A  (Sw0) | Carry (F1)  (L1) | Sum (F2)  (L2) |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

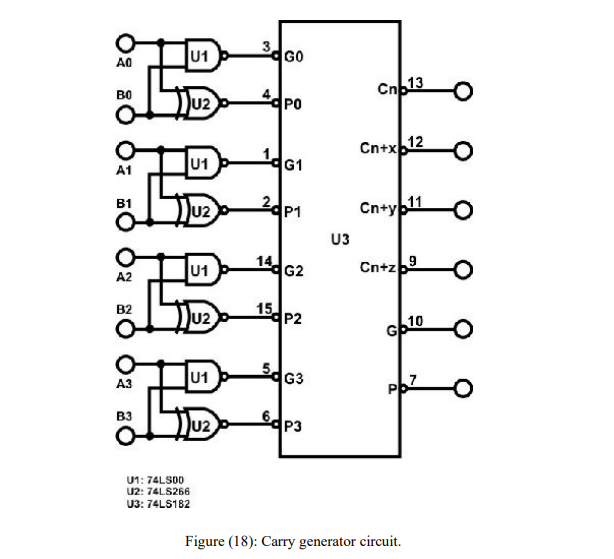
**4.Constructing 4-Bit Full-Adder with IC:**

Connect input X0~X3 (addends), Y0~Y3 (augends) to DIP switches DIP2.0~2.3 and DIP1.0~1.3 respectively as shown in Figure 17. Connect F1, Σ1, Σ2, Σ3, Σ4 to L1~L5. Follow input sequences in Table 5 and set SW0 to “0”; record F1 and Σ in binary numbers.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| C  (Sw3) | B  (Sw2) | A  (Sw1) | Carry (F3) (L1) | Sum (F5) (L2) |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

**5.** **High-Speed Adder Carry Generator Circuit:**

U3 (74182) on block High-Speed Adder of module IT-3003 is used to construct a carry generator circuit shown in Figure 18.

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The results are :

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **inputs** | | | | | | | | **OUTPUTS** | | | | |
| **y3** | **y2** | **y1** | **y0** | **x3** | **x2** | **x1** | **x0** | Σ4 | **Σ3** | **Σ2** | **Σ1** | **F1(CARRY)** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |

Note here’s an error in the carry it’s wrong because y5 5 wasn’t connected in the circuit.

2.Connect inputs A0~A3 (addends) to DIP Switches 1.0~1.3; B0~B3 (augends) to DIP2.0~2.3, connect Cn to SW0, and set SW0 to “0”. Follow the input sequences in Table 6 and record output states.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUTS** | | | | | | | | **OUTPUTS** | | | | |
| B3 | B2 | B1 | B0 | A3 | A2 | A1 | A0 | Cn+x | Cn+y | Cn+z | Gcom | Gcom |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |  |  |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 00 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUTS** | | | | | | | | **OUTPUTS** | | | | |
| B3 | B2 | B1 | B0 | A3 | A2 | A1 | A0 | Cn+x | Cn+y | Cn+z | Gcom | pcomp |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 00 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |

Using **IC** we construct **Full - Subtractor** as following:



Use Module IT-3003 block Full Adder (Figure 21). Connect inputs X3~X0 (minuend) to DIP Switch 1.3~1.0; Y3~Y0 (subtrahend) to DIP 2.3~2.0; Y5 to SW0. Connect outputs F1 to L4; F11~F8 to L3~L0. To execute the subtract operation

**The results are :**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| X3  Sw7 | X2  Sw6 | X1  Sw5 | X0  Sw4 | Y3  Sw3 | Y2  Sw2 | Y1  Sw1 | Y0  Sw0 | Borrow  F1 | F11 | F10 | F9 | F8 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |

* **Conclusion:**

From this experiment we realized how the comparator works and compares numbers bit by bit , and we knew how to construct it using gates and IC's , we got used to how half –full adders and subtractors works, for example half adder and subtractor doesn’t take the previous output unlike full adder and subtractor ( borrow for subtractor, carry for adder ) , beside that when we constructed BCD adder we noticed that when the two numbers are greater than 9 un-meaningful results occurred so we realized that we have to add 6 by using and gates to have meaningful results.

* **References :**

all of my references are from the lab manual

diagrams and pictures are from Google and the lab manual.