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CAREER OBJECTIVE:

An aspirant with immense wisdom and individuality to take wise decisions and finish any task with perfection under speculated time. Have great experience in bringing simplified version of a complicating issue. My style of work is doing tasks efficiently with much more accuracy.

EDUCATION QUALIFICATIONS:

M.Tech (Power electronics)
SR University- 2023

B.Tech (E.E.E)
Deccan College Of Engineering and Technology-(OU)-2018

TECHNICAL SKILLS:

Technical:
VLSI Design verification,
Electrical designing,
AWS & DEVOPS

Programming Languages:
Basics of C & C++, HTML, CSS, JS, Node.js, SQL, java, python, Verilog, System Verilog, Basics of UVM

Operating system:
Windows, Unix, Linux, Mac os

Tools:
Aws, git&github, Jenkins, azure, Docker, Kubernetes, Terraform, AutoCAD, Xilinx ISE, Synopsys VCS, Cadence virtuoso, Matlab, Revit, Dialux, Relux, PVsyst, Google Sketch Up

Microsoft Technologies:
MS Office

CERTIFICATION

*) AWS Cloud Practitioner Essentials
*) Object Storage - Knowledge Badge
*) Cloud Essentials - Knowledge Badge

PROFESSONAL EXPERIENCE

VLSI Design Verification Engineer
Sumedha Technosys Pvt.Ltd [2019-2020]

JOB RESPONSIBILITIES

As a VLSI (Very Large-Scale Integration) Design Verification Engineer my role is to ensure that the designs meet specifications and are free from functional and logical errors by understanding of digital design principles, ASIC/FPGA design flow, and verification methodologies.
where I must manage the tasks like

1. Verification Planning and Strategy:

Developed comprehensive verification plans outlining test strategies, methodologies, and coverage goals for complex digital designs.

2. Testbench Development:

Designed and implemented scalable and reusable verification environments and testbenches using System Verilog and UVM.

3. Functional Verification:

Executed extensive functional verification using simulation tools to ensure compliance with design specifications.

4. Assertion-Based Verification:

Implemented and validated design properties and assertions to enhance early error detection.

5. Formal Verification:

Applied formal verification techniques to prove design correctness and identify potential functional issues.

SOFT-SKILLS:

- Teamwork
- Problem solving
- Communication
- Adaptability
- Critical thinking
- Time management
- Interpersonal

6. Timing and Power Analysis:

Conducted thorough timing analysis to validate timing constraints and optimize performance.
Performed power analysis to ensure designs met power consumption requirements.

7. Gate-Level Simulation:

Conducted gate-level simulations to validate the consistency between RTL and gate-level netlists.

8. Debugging and Issue Resolution:

Identified and resolved design issues through in-depth analysis of simulation results, waveforms, and debug logs.

9. Coverage Analysis:

Utilized coverage metrics to assess and improve verification completeness, including functional and code coverage.

10. Collaboration and Communication:

Collaborated with design engineers to understand design intent and resolve issues effectively.
Participated in cross-functional team meetings to ensure alignment between design and verification efforts.

11. Documentation:

Maintained detailed documentation of test plans, methodologies, and verification results for internal and external reference.

12. Regression Testing:

Managed and expanded regression test suites to validate new design iterations and ensure backward compatibility.

13. Tool Proficiency:

Stayed current with industry-standard EDA tools and methodologies, incorporating the latest advancements into the verification flow.

14. Continuous Learning:

Actively pursued professional development opportunities and attended relevant workshops or conferences to stay abreast of emerging trends in VLSI design and verification.

DECLARATION:

I hereby declare that the above stated information is true to the best of my knowledge.

Date : **(MOHAMMAD ARIF PASHA)**

Place: