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Design of Efficient 4x4 Enhanced Pipeline multiplier Based with Various Optimization Techniques

Abstract -- In this paper, we are unveiling a novel 4x4 pipeline multiplier blueprint, set apart by its two-stage structure and innovative development techniques. The backbone of our design is operand fragmentation, where we break down complex tasks into simpler parts, significantly boosting the speed of computations. Additionally, our system cleverly adjusts the clock frequency according to the task at hand, ensuring energy efficiency while maintaining excellent performance. A notable aspect of our design is the experimental determination of a 2:1 ratio of PMOS to NMOS transistors, which harmonizes the fall and rise times of the inverter, optimizing the circuit's efficiency.

1. INTRODUCTION

In the fast-paced world of electronics, finding ways to make devices faster, more powerful, and energy-efficient is always the goal. Our project takes a big step in that direction, presenting a new 4x4 two-stage pipelined multiplier system that aims to be a game-changer in the field.

At the core of this project is a group of well-designed parts, including half-adders, and gates, full adders, and a special component called the D-Flip Flop [1]. These parts work together to create a highly efficient and fast calculating unit. We've focused on making sure it doesn't use a lot of power and can get tasks done quickly without delays, setting a new standard for how powerful yet compact multipliers can be in modern electronics [2].

In this paper, we'll take you through our journey of building this project, from the first ideas to the final product. We'll explain how each part works and comes together to form a powerful tool, showcasing its abilities with a real-life test case. Join us as we explore the potential of this new technology to speed up calculations while saving energy, showing a fresh and practical approach to modern electronics development.

2. EXISTING SYSTEM AND SIMULATION COMPARISON

A. 2-inputs NAND gate

The idea and implementation of a NAND gate, the key component of our ground-breaking 4x4 pipeline multiplier system, received a lot of attention during the project's earlier stages. The logical configuration of the gate, which is essential to the proper operation of the complete circuitry, is defined by the schematic representation, which was painstakingly created using the electric tool.

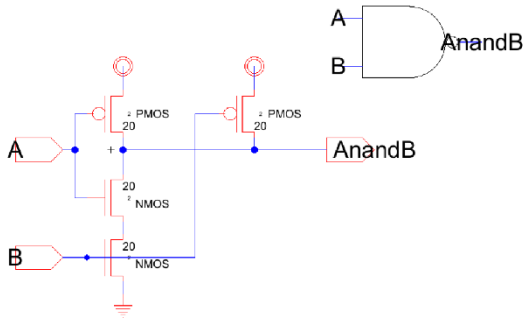

Figure 1: 2 input Nand Schematic

the layout encapsulates an arrangement that aims to minimize power consumption while maximizing efficiency, a vital consideration given our project's core focus on enhancing speed and power conservation.

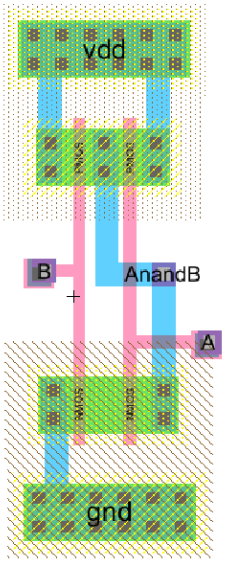

Figure 2: 2 input Nand Layout

B. Inverter

Our 4x4 pipeline multiplier system's inverter, which can be schematically represented using the Electric tool, is essential to its effective operation. In order to govern signal paths and guarantee accurate computations in the larger circuit network, this conversion is essential. The layout of the device, which specifies the physical characteristics and configurations of the transistors and connections, is optimized for low power and area consumption. With this design, the project's primary goals of increased speed, power efficiency, and space efficiency will be advanced. Smooth and quick signal transitions are essential for completing high-speed computations.

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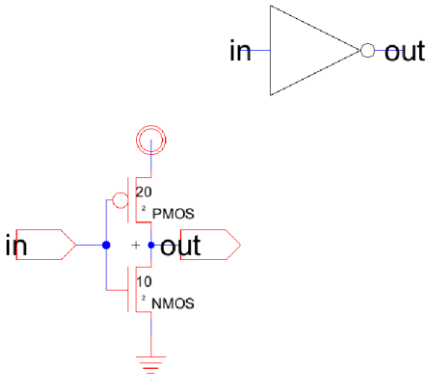

Figure 3: Inverter Schematic

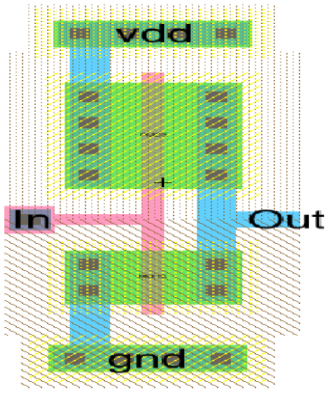

Figure 4: Inverter Layout

C. 2- input AND gate

The AND gate in our circuit exhibits a creative and resource-efficient design, being constructed using a combination of a NAND gate followed by an inverter. The 2-inputs NAND gate implementation will be used to find the multiplication between two bits in the full adder.

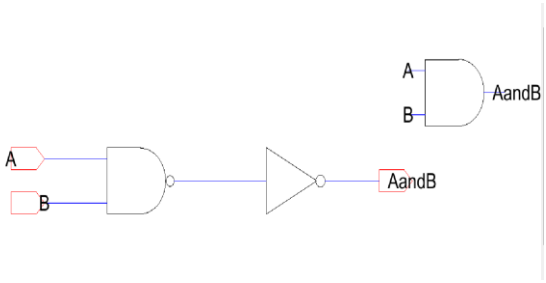

Figure 5: 2 input AND Schematic

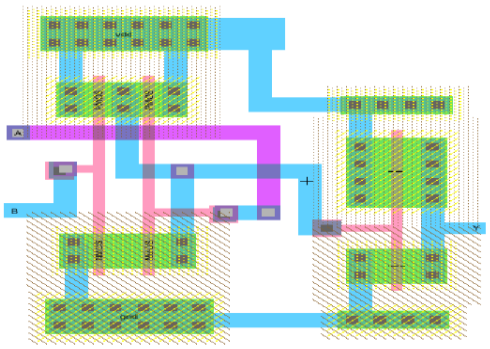

Figure 6: 2 input AND Layout

D. 2-input XOR gate

The XOR gate within our project is a testament to engineering precision and optimization, utilizing a structure that incorporates 12 transistors to achieve its function. The utilization of 12 transistors in its construction is a strategic choice, optimizing the balance between power consumption and performance speed. This detailed configuration allows for a streamlined and efficient operation, minimizing the lag that is often associated with complex gate configurations, hence fostering faster computation times. This component thus stands as a vital cog in the full and half adder that's used in the advanced 4x4 pipeline multiplier system, promising reliability and efficiency in operations.

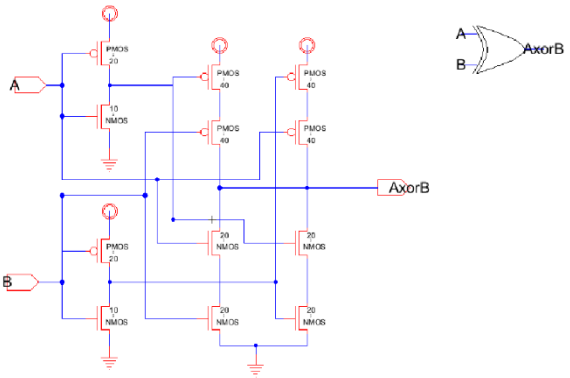

Figure 7: 2 input XOR schematic

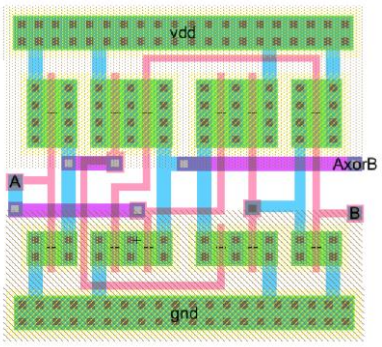

Figure 8: 2 input XOR Layout

Mohammad Abu Shams 1200549, Mohammed Owda 1200089, Hamza Najjar 1192605

E. Half Adder

The half adder, a fundamental unit in the arithmetic logic circuitry of our project, is adeptly designed using XOR and AND gates, a combination that allows for the efficient execution of binary addition. In this design, the XOR gate is utilized to perform the binary addition of the two input bits, generating a sum output. Concurrently, the AND gate processes the same input bits to produce a carry output

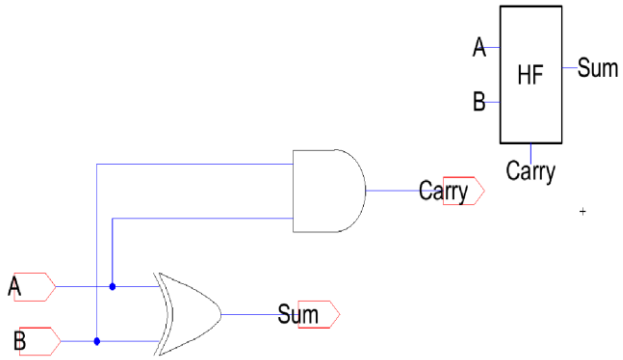

Figure 9: Half Adder Schematic

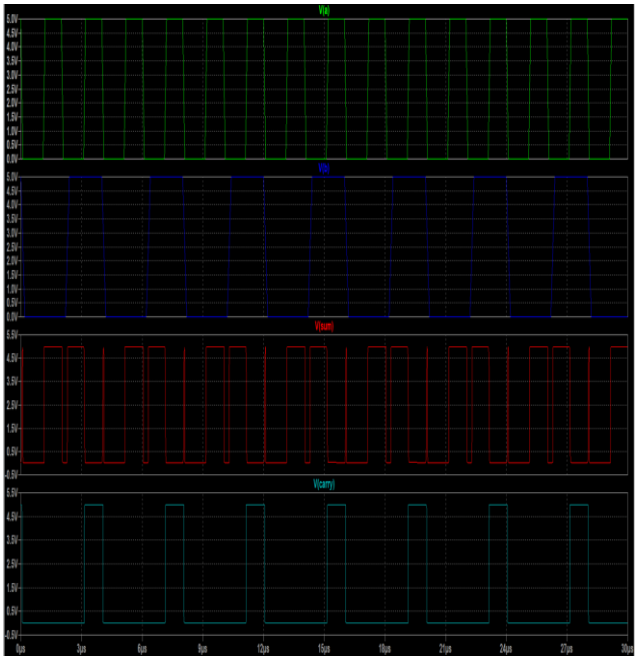

Figure 10: Half Adder Waveform

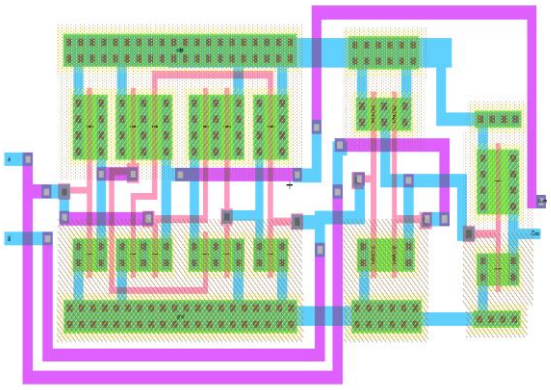

Figure 11: Half Adder Layout

F. Full Adder

The full adder component of our project, instrumental in executing complex binary calculations, is meticulously designed utilizing two XOR gates and three NAND gates.

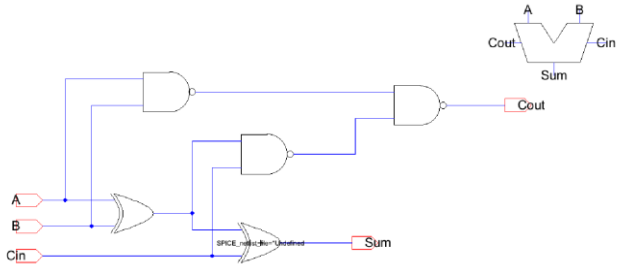

Figure 12: Full Adder Schematic

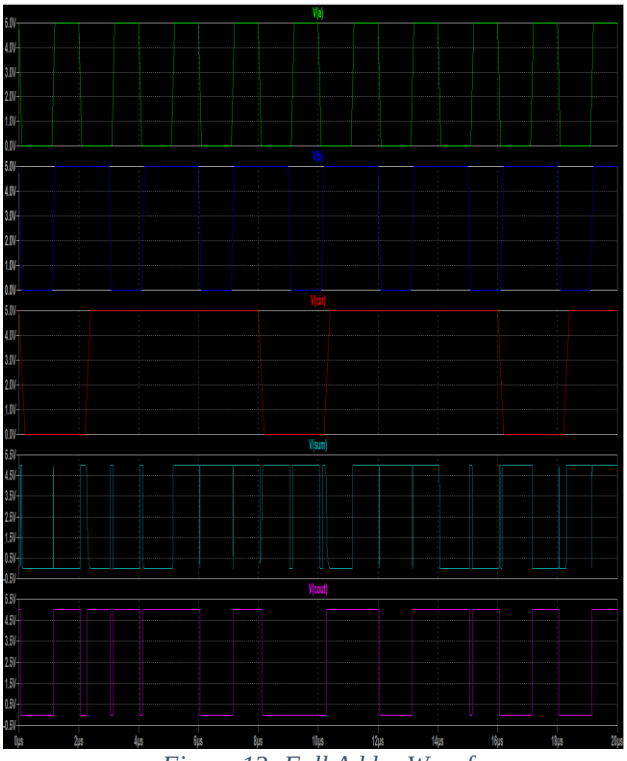

Figure 13: Full Adder Waveform

In this layout, a clear emphasis is placed on minimizing the distances between interconnected gates to reduce signal propagation delays, thereby accelerating computation speed.

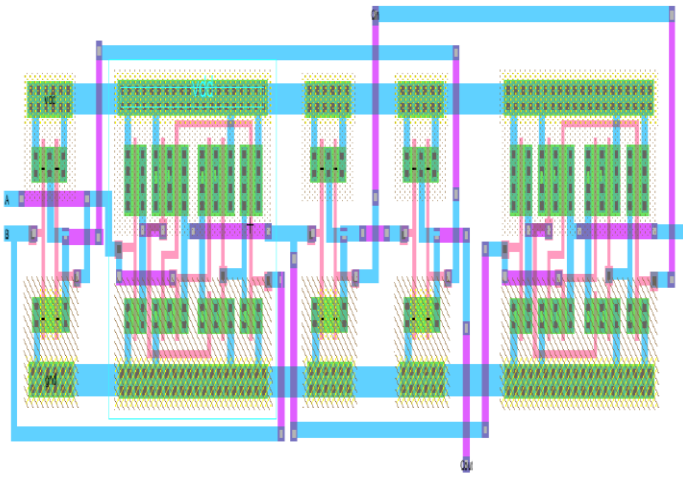

Figure 14: Full Adder Layout

G. P Latch

In our 4x4 pipeline multiplier project, the P latch stands as a fundamental component of D-Flip Flop, embodying both innovation and efficiency in its design, which utilizes 10 transistors. This specific layout ensures a robust and dependable latch system capable of precise data flow control and minimal leakage currents, thereby guaranteeing signal integrity throughout operations.

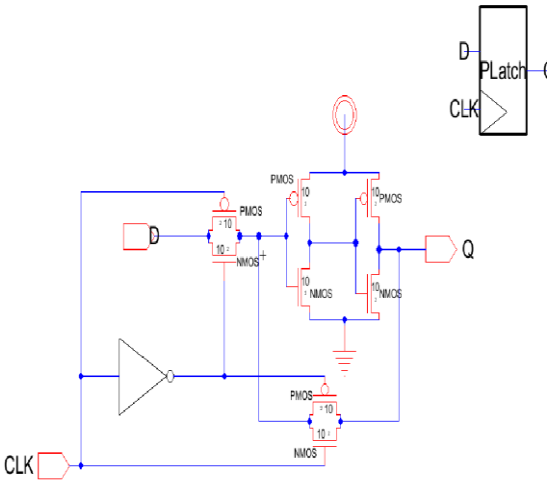

Figure 15: P Latch Schematic

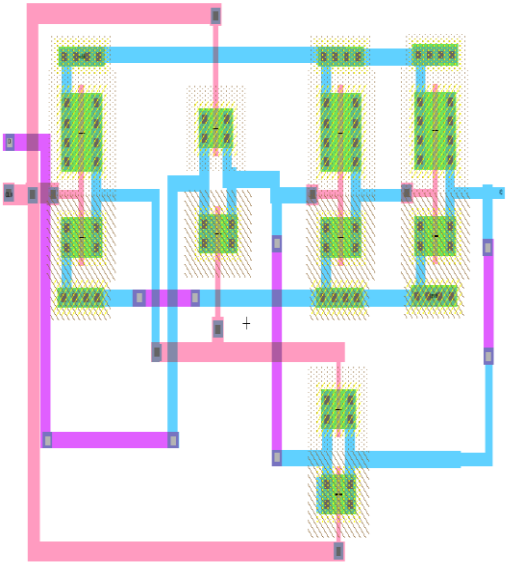

Figure 16: P Latch Layout

H. N Latch

In the design blueprint of our 4x4 pipeline multiplier, the N latch holds a significant position, specially crafted using 10 transistors, mirroring the complexity and efficiency found in the P latch. It's designed same as P latch, but we inverted the clock on the two pass gates.

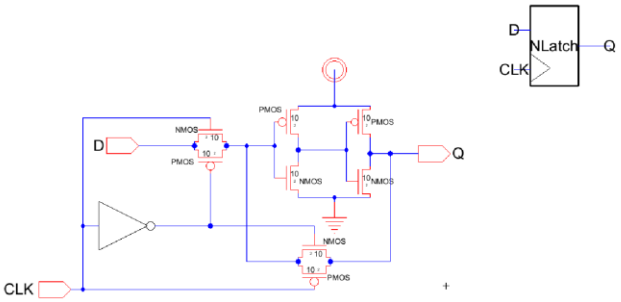

Figure 17: N Latch Schematic

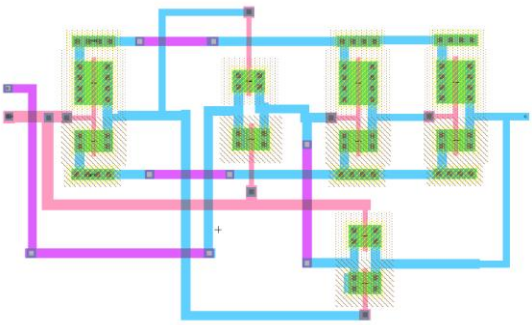

Figure 18: N Latch Layout

Mohammad Abu Shams 1200549, Mohammed Owda 1200089, Hamza Najjar 1192605

I. D Flip Flop

D-Flip Flop is a key component that brings together the strengths of both the N and P latches, helping to make our 4x4 pipeline multiplier fast and efficient. This setup is like a team where each member has a specific role, working together seamlessly to handle data in the best possible way. This combined approach not only saves space but also makes sure that the data moves smoothly and quickly without any hitches, contributing to a highly efficient and streamlined multiplier system that's easy to implement in various applications.

D-Flip Flop serves a crucial role in creating a two-staged pipeline multiplier, acting like a reliable storage unit that safely holds onto data at each stage of the pipeline. By doing this, it ensures that the data is organized and ready for the next step in the process, making the whole system run more smoothly and quickly.

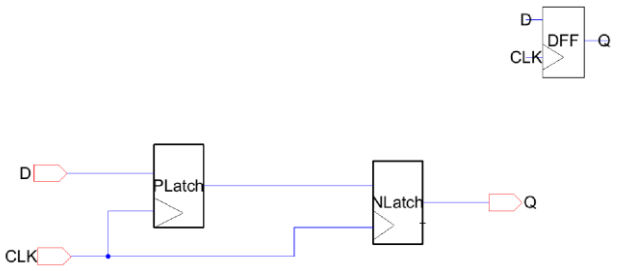

Figure 19: D Flip-flop Schematic

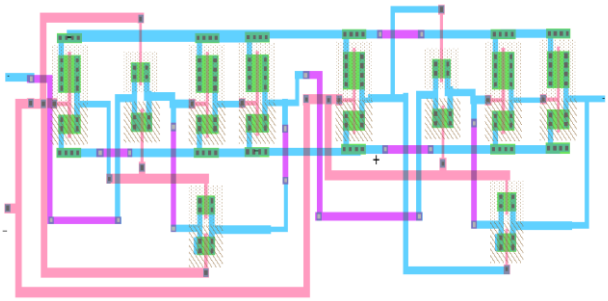

Figure 20: D flip flop Layout

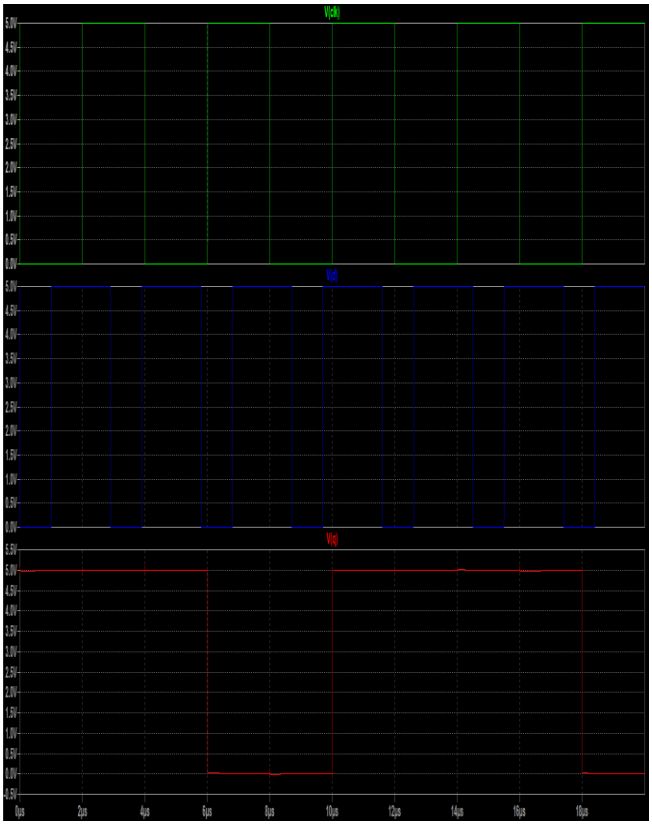

Figure 21: D Flip Flop Waveform

J. 4x4 Two-stage Pipelined Multiplier

In our project, the 4x4 two-stage pipelined multiplier serves as the core component, intelligently integrating the functions of previously discussed elements: the half-adder, and gate, full adder, and the D-Flip Flop. Initially, the and gates and half-adders manage the primary calculations, simplifying complex multiplications into easier operations. This facilitates a smoother computational process right from the first stage.

Subsequently, the second stage takes over, where the full adder synthesizes partial products, crafting the final results from the data accumulated in the initial phase. Here, the D-Flip Flop is indispensable, functioning as a reliable bridge between the two stages by securely storing intermediate data and ensuring an uninterrupted, streamlined flow of information.

These parts work as an integrated system that is capable of processing massive amounts of data rapidly and accurately. This multiplier represents a significant achievement in the field of modern electronic system designs because it not only demonstrates effectiveness and speed but also flexibility.

Mohammad Abu Shams 1200549, Mohammed Owda 1200089, Hamza Najjar 1192605

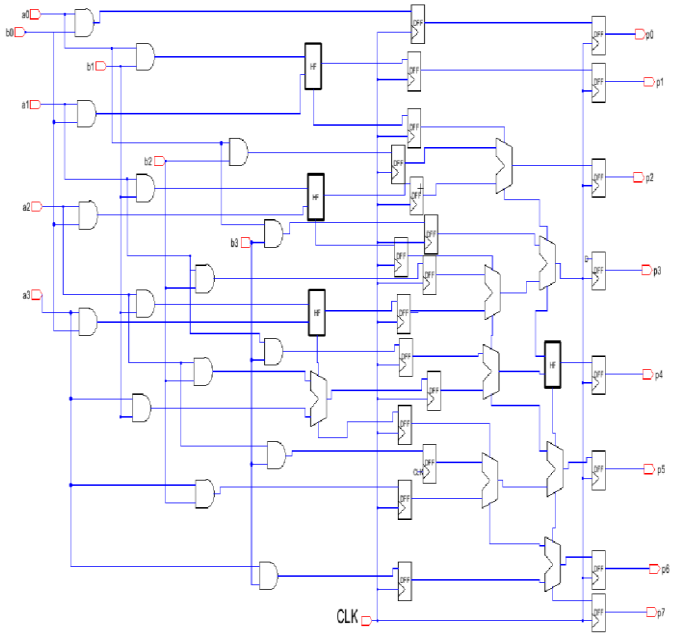

Figure 22: 4x4 Two-stage Pipelined Multiplier Schematic

```
VA a0 0 pulse 5 0 0 0n 0n 2u 40u
VA1 a1 0 pulse 5 0 0 0n 0n 2u 30u
VA2 a2 0 pulse 0 0 0 0n 0n 2u 30u
VA3 a3 0 pulse 0 0 0 0n 0n 2u 30u
Vb0 b0 0 pulse 0 0 0 0n 0n 2u 30u
Vb1 b1 0 pulse 5 0 0 0n 0n 2u 30u
Vb2 b2 0 pulse 0 0 0 0n 0n 2u 30u
Vb3 b3 0 pulse 0 0 0 0n 0n 2u 30u
Vclk CLK 0 pulse 5 0 0 0n 0n 3u 6u
.tran 0 50u
.include D:\Program\Electric\C5_models.txt
.END
```

Figure 24: Test case for the 4x4 multiplier

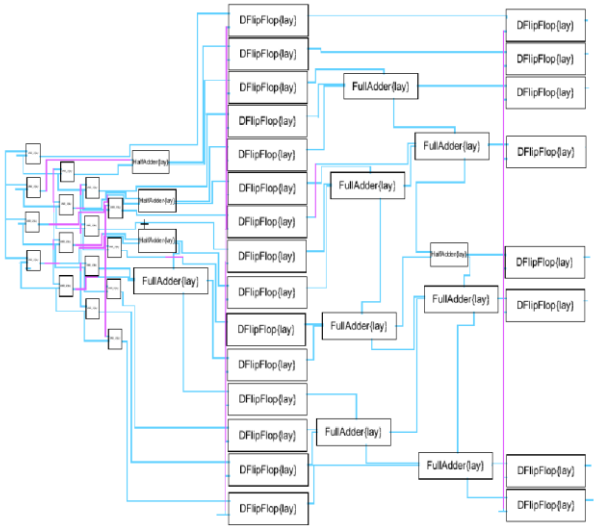

Figure 23: 4x4 Two-stage Pipelined Multiplier Layout

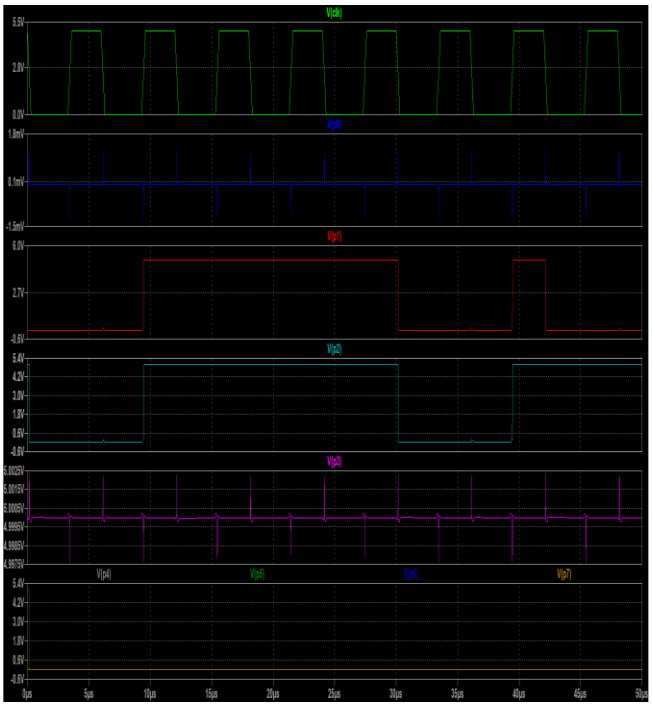

Figure 25: Output Waveform of the 4x4 multiplier

In a practical demonstration of the system's capability, a test case was conducted where the numbers 3 and 2 were multiplied. In binary terms, 3 is represented as 0011 (a3a2a1a0) and 2 as 0010 (b3b2b1b0). The 4x4 two-stage pipelined multiplier executed this operation impeccably, delivering the correct output in a two-cycle process, which is characteristic of a 2-stage pipelined system. The result,

highlighted in the output string p7p6p5p4p3p2p1p0, was 00000110, which accurately translates to 6 in decimal, showcasing the system's efficiency and accuracy in real-time computations. This test case effectively illustrates the multiplier's reliability and speed, promising robust performance in more complex, real-world applications.

3. Power and Delay results

In this section, we provide a comprehensive analysis of the power consumption and delay characteristics of our newly developed 4x4 two-stage pipelined multiplier, in comparison to a traditional 4x4 multiplier.

Figure 26, 27 shows the delay time of rising and falling time of the 4x4 two-stage pipelined multiplier

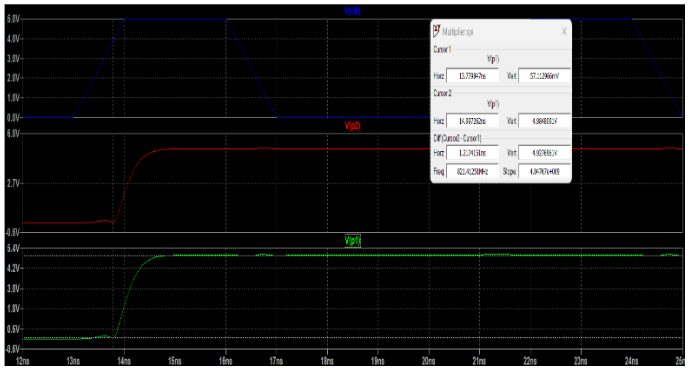

Figure 26: rise time delay

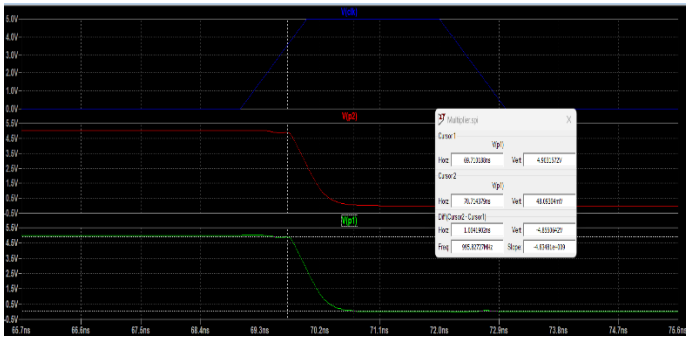

Figure 27: Fall down delay

Figure 28 shows the maximum and minimum time of rising and falling time of the 4x4 two-stage pipelined multiplier

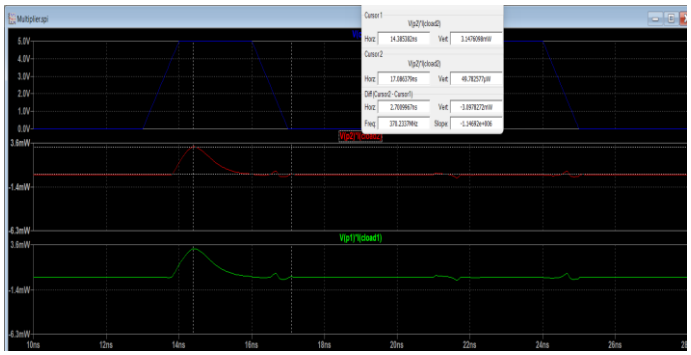

Table 1 shows the comparison between our multiplier and 90-T 4x4 Multiplier

	90-T 4x4 Multiplier 65-nm technology.	Our 4x4 Multiplier 300-nm technology.
Avg Power	18.156mW	1.59839mW
Max Power	0.2267W	3.147mW
Min Power	0.6970mW	49.78uW
Rise Time Delay	1.3875ns	1.23ns
Fall Time Delay	1.2046ns	1.004ns

4. CONCLUSION

We created a new 4x4 pipeline multiplier that is both fast and saves energy. This project brings together small but vital parts, like half-adders and full adders, to work quickly without using much power. This is a big step forward in modern electronics, making devices better and more environmentally friendly.

Also, our design smartly uses different sizes of transistors and a new method for calculating carries, making multiplication tasks much faster. As we finish, we hope our project shows a bright path forward for creating technology that is both powerful and good for the planet.

5. REFERENCES

[1] A.Venkatesh, N.Rathan, R.Saranya. (2017) Design of Power Efficient 4x4 Multiplier Based On Various Power Optimizing Techniques. Asian Journal of Applied Science and Technology (AJAST). Volume 1, Issue 2, Pages 115-119, March 2017.

[2] Vijayakumar, V., Ilayarajaa, K. T., Ravi, T., & Sugadev, M. (2021). Analysis of High Speed Hybrid Full Adder. 2021 International Conference on Artificial Intelligence and Smart Systems (ICAIS).

[3] Shing Jie, Lee & Ruslan, Siti Hawa. (2017). A 4x4 bit vedic multiplier with different voltage supply in 90 nm CMOS technology. International Journal of Integrated Engineering. 9. 114-117.

[4] Mukherjee, B., & Ghosal, A. (2019). Counter Based Low Power, Low Latency Wallace Tree Multiplier Using GDI Technique for On-chip Digital Filter Applications. 2019 Devices for Integrated Circuit (DevIC).

[5] Agwa, S., Yahya, E., & Ismail, Y. (2013). Variability mitigation using correction function technique. 2013 IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS).

[6] *cmosedu*. (2023, September 1). Retrieved from https://cmosedu.com/jbaker/courses/ee421L/f13/students/wolvert9/Lab%206/Lab6.html