# **CodeBreaker:** A Morse Challenge on FPGA

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## Introduction

This project presents the design and implementation of a password-protected Morse code training game on the DE0-CV FPGA development board using Verilog HDL. The system is intended to reinforce both digital design principles and user interaction through a hardware-based gamified learning environment. It integrates secure multi-user authentication, difficulty-based gameplay, real-time visual feedback, and score tracking, all operating within a self-contained FPGA architecture.

The system begins with an authentication phase in which the user enters a unique 4-digit ID followed by a 4-digit password using a set of switches and a button. These credentials are verified against values stored in ROM. Upon successful login, the user is granted access to the game. A difficulty level is selected, determining the pool of words used for gameplay. Each game session is limited to two minutes, enforced by an internal countdown timer built from modular hardware timers and a 1ms-resolution pseudo-random LFSR timer.

During gameplay, randomly selected 5-letter words are displayed sequentially on a VGA monitor. The user must input each letter using a 4-step Morse code entry system via buttons representing dot, dash, and gap. Each symbol is encoded and compared against the correct Morse sequence, with feedback provided through five LEDs to indicate per-letter correctness. A successful match contributes to the user's score, which is tracked in real time and displayed at the end of the session.

The design is modular, with separate components handling authentication, game control, Morse decoding, visual rendering, and timing. All modules are synchronized through a unified top-level module (TopModule). Key subsystems include finite state machines for control flow, ROM modules for ID, password, and word storage, a VGA renderer for textual output, a seven-segment display driver for timing, and LFSR-based pseudo-random generators for word selection and delay control.

This project showcases the application of hardware design methodologies in constructing an interactive, time-sensitive digital system that combines control logic, user input handling, randomization, memory access, and real-time display generation. It demonstrates a comprehensive approach to FPGA-based embedded system design, emphasizing both functionality and user experience.

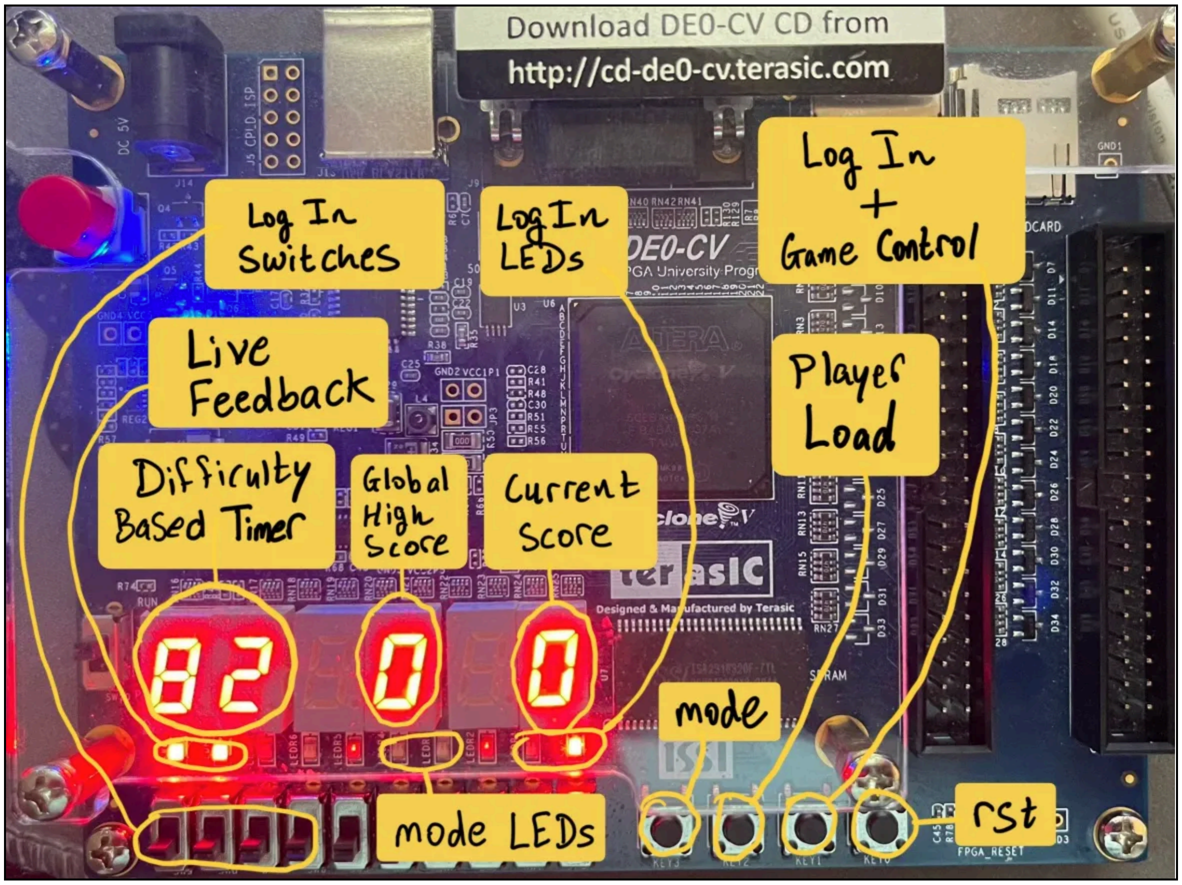

**Figure 1:** FPGA for CodeBreaker Game.

## System Architecture Design

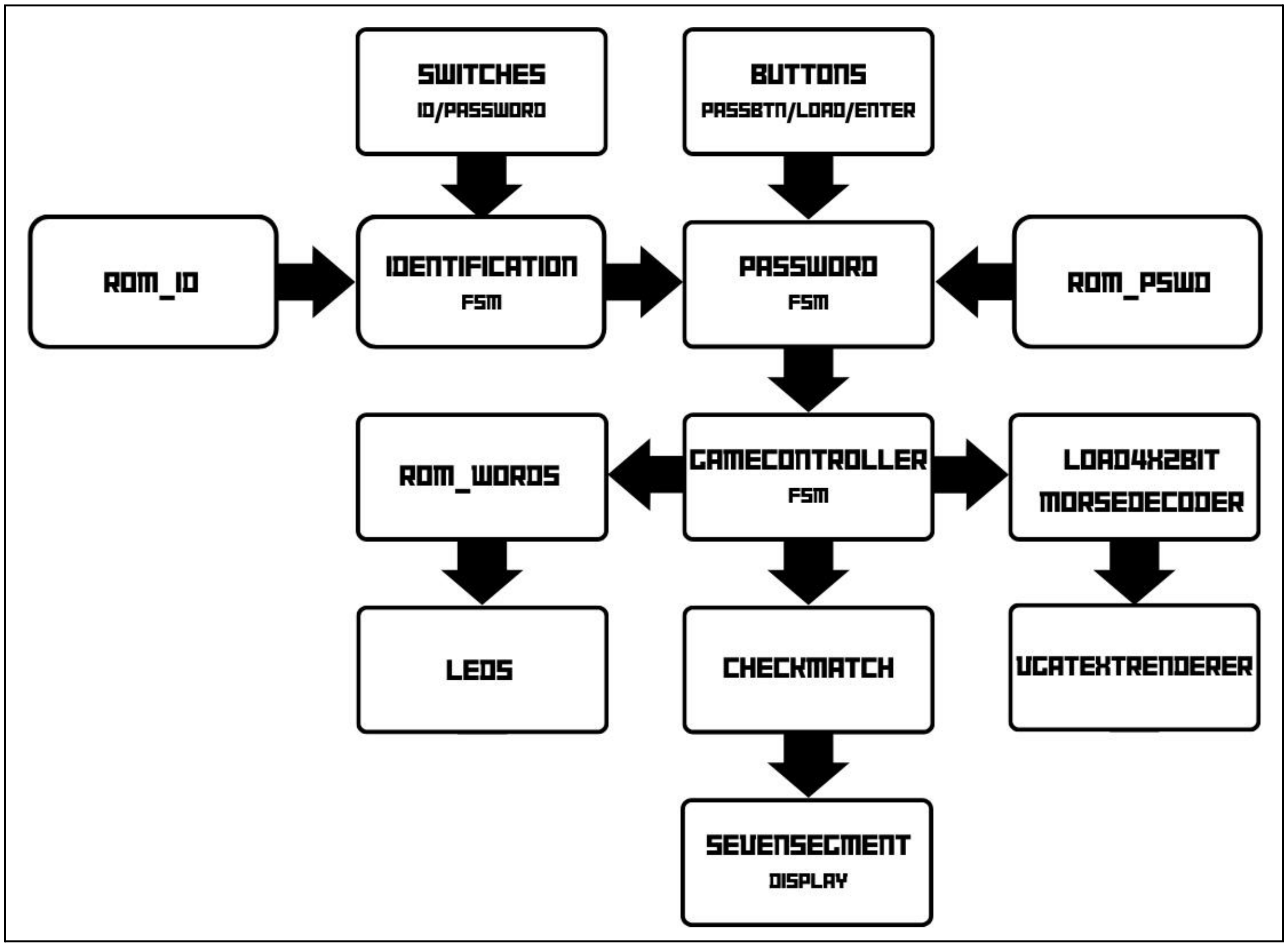

**Figure 2:** Top-Level System Architecture of Game.

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**Module**: ROM_ID
**Inputs**:
- **Clock**: Clock Signal.
- **Address**: Address of the ID digit at the given address.

**Outputs**:
- **q**: 4-bit ID digit at the given address.

**Functionality**:
- Stores a predefined set of 4-bit ID digits in ROM. On each clock cycle, outputs the digit at the specified address to be matched during ID verification.

**Module**: ROM_PSWD

**Inputs**:

- **Clock**: Clock Signal.
- Address: Address of the password digit at the given address.

**Outputs**:

- **q**: 4-bit password digit at the given address.

**Functionality**:

- Stores a predefined set of 4-bit password digits in ROM. On each clock cycle, outputs the digit at the specified address to be matched during password authentication.

**Module**: LoadRegister

**Inputs**:

- clk: Clock Signal.
- **rst**: Reset Signal.
- **Load**: Load signal to latch input.
- **D_in**: 4-bit user input.

**Outputs**:

- **D_out**: 4-bit latched output.

**Functionality**:

- Temporarily stores a 4-bit input from switches when the load signal is asserted. Provides stable output for comparison or processing.

**Module**: ButtonShaper

**Inputs**:

- **clk**: Clock Signal.
- **rst**: Reset Signal.
- **B_in**: Raw mechanical button input.

**Outputs**:

- **B_out**: Clean, debounced button pulse.

**Functionality**:

- Debounces a mechanical button press using a clocked filter mechanism. Produces a single-cycle pulse on B_out when a valid rising edge is detected on B_in.

**Module**: Identification

**Inputs**:

- **clk**: Clock Signal.
- **rst**: Reset Signal.
- **PassBtn**: Button press signal to load each digit of the ID.
- **InputID**: 4-bit input digit from user.
- **mode**: 2-bit user selection input.

- Timeout: External timeout signal.

**Outputs**:

- **CheckPassword**: Signal asserted when ID verification is complete and successful.
- **MatchedID**: 3-bit output index indicating the matched ID slot.
- **letterLEDs**: 5-bit output showing which ID digits matched correctly.

**Functionality**:

- Finite State Machine that processes four sequential ID digits entered by the user and compares them against five stored ID combinations in ROM_ID. If a match is found, it asserts CheckPassword and outputs the index of the matched ID. If verification fails or times out, it resets.

**Module**: Password

**Inputs**:

- **clk**: Clock Signal.
- **rst**: Reset Signal.
- **CheckPassword**: Signal to begin password checking after ID verification.
- **PassBtn**: Button press to load each digit of the password.
- **InputPassword**: 4-bit user input for password digit.
- **MatchedID**: 3-bit index of the verified ID from Identification.
- **mode**: 2-bit input to select user profile.
- **timeout**: Signal to indicate timeout/reset condition.

**Outputs**:

- **LoggedIn**: High when the entered password matches the ROM entry.
- **letterLEDs**: 5-bit output indicating which password digits were correct.

**Functionality**:

- FSM that accepts four 4-bit password digits and compares them against the password associated with the MatchedID and mode. If all digits match, asserts LoggedIn. During entry, each digit's correctness is shown via letterLEDs. Resets on timeout or incorrect entry.

**Module**: GameController

**Inputs**:

- **clk**: Clock Signal.
- **rst**: Reset Signal.
- **PassEnter**: Button signal to start the game after login.
- **LoggedIn**: High when user authentication is successful.
- **Timeout**: High when the game duration has ended.
- **mode**: 2-bit input to indicate selected difficulty level.

**Outputs**:

- **ReconfigTimer**: Pulse to reconfigure/reset the game timer.
- **enable**: High when the game is active and Morse input is allowed.

**Functionality**:

- FSM that transitions from idle to active gameplay upon successful login and PassEnter. While active, it asserts enable to allow user Morse input. When Timeout occurs, it deactivates the game and asserts ReconfigTimer to reset the timer logic.

**Module**: ROM_WORDS

**Inputs**:

- **Clock**: Clock Signal.
- **Address**: 7-bit address input used to select a specific ASCII character from stored words.

**Outputs**:

- **q**: 8-bit ASCII character corresponding to the current address.

**Functionality**:

- Implements a read-only memory block using Altera's altsyncram megafunction to store a list of characters that make up 5-letter words. Each character is 8-bit ASCII, and each word is stored in 5 consecutive addresses. Outputs one letter per clock cycle based on the input address, supporting sequential word retrieval for the Morse game.

**Module**: ModeRotator

**Inputs**:

- **clk:** Clock Signal.
- **rst:** Reset Signal
- **button**: Debounced button press.

**Outputs**:

- **mode**: 2-bit user output (dot, dash, gap).

**Functionality**:

- Rotates user 2-bit output (dot, dash, gap).

**Module**: MorseDecoder

**Inputs**:

- **MorseInput**: 8-bit packed Morse code sequence representing 4 symbols (each 2 bits: 0 = gap, 1 = dot, 3 = dash), ordered as {b0, b1, b2, b3}.

**Outputs**:

- **ASCIIOutput**: 8-bit ASCII value corresponding to the decoded letter.

**Functionality**:

- Combinational decoder that maps a 4-symbol Morse sequence encoded in 8 bits to its corresponding uppercase ASCII letter (A–Z). Supports only valid Morse patterns and outputs the matching character directly based on case patterns.

**Module**: Load4x2bit

**Inputs**:

- **clk**: Clock Signal.
- **rst**: Reset Signal.
- **enable**: Enables the shift/load operation.
- **load**: Asserted to load a new 2-bit symbol.
- **in**: 2-bit Morse code symbol (0 = gap, 1 = dot, 3 = dash).

**Outputs**:

- **out**: 8-bit packed Morse sequence {b0, b1, b2, b3}.
- **ready**: High when all 4 symbols have been loaded.

**Functionality**:

- Sequentially loads four 2-bit Morse symbols into an 8-bit register. Each time load is asserted while enable is high, a new symbol is stored. Once all four entries are collected, ready is asserted and the packed sequence is output via out.

**Module**: CheckMatch

**Inputs**:

- **clk**: Clock Signal.
- **rst**: Reset Signal.
- **LetterEnter**: Signal indicating a new decoded letter is ready.
- **ASCIIOutput**: 8-bit decoded letter from MorseDecoder.
- **mode**: 2-bit difficulty level.
- **timeout**: Game timeout signal.
- **Button**: External button signal for resetting post-timeout.
- **rand**: 5-bit random index used to select a word from ROM_WORDS.

**Outputs**:

- **Match**: High when a full 5-letter word is entered correctly.
- **letterLEDs**: 5-bit signal showing per-letter correctness.
- **Points**: 4-bit score counter, incremented on successful word match.
- **HighScore**: Tracks and stores the highest score achieved.

**Functionality**:

- FSM that compares each user-entered ASCII letter against the expected letters in a target word from ROM_WORDS (addressed using rand and letterIndex). It updates letterLEDs to reflect per-letter correctness. Upon matching all five letters, it asserts Match, increments Points, and resets for the next word. It resets on timeout + button press and updates HighScore when Points exceed the previous maximum.

**Module**: LFSRRNG

**Inputs**:

- **clk**: Clock Signal.
- **rst**: Reset Signal.
- **enable**: Enables the LFSR to shift and generate new output values.

**Outputs**:

- **rand**: 4-bit pseudo-random output.

**Functionality**:

- Generates a pseudo-random number between 0 and 15 using a 5-bit Linear Feedback Shift Register. When enabled, the LFSR shifts on each clock edge, and the lower 4 bits are output as rand. Used to select a random word index during gameplay.

**Module**: LFSR1ms

**Inputs**:

- **clk**: Clock Signal.
- **rst**: Reset Signal.
- **enable**: Enable signal to start countdown.
- **mode**:  2-bit input to select the target timeout value.
- **ReconfigTimer**: Loads a new timeout value from mode.

**Outputs**:

- **timeout**: High when LFSR reaches the target count.

Functionality:

- Implements a pseudo-random countdown timer using a 17-bit Linear Feedback Shift Register. When ReconfigTimer is asserted and enable is low, it loads a new TimeoutNumber based on the selected mode. Once enable is high, the LFSR begins shifting and asserts timeout when its state matches the loaded TimeoutNumber

**Module**: CountTo100

**Inputs**:

- **clk**: Clock signal (driven by LFSR1ms timeout).
- **rst**: Reset Signal.

**Outputs**:

- **timeout**: High for one cycle after 100 LFSR timeouts.

**Functionality**:

- Counts up to 100 clock pulses from LFSR1ms. Once 100 pulses are reached, it asserts timeout for one cycle and resets internally to begin counting again. Used as an intermediate scaler in a timebase chain.

**Module**: CountTo10

**Inputs**:

- **clk**: Clock signal (driven by CountTo100 timeout).

- **rst**: Reset Signal.

**Outputs**:

- **timeout**: High for one cycle after 10 pulses from CountTo100.

**Functionality**:

- **Counts** 10 pulses from CountTo100. On reaching 10, asserts timeout for one cycle and resets. Serves as the final stage in the 1-second pulse generator.

**Module**: OneSecTimer

**Inputs**:

- **clk**: System clock signal.
- **rst**: Reset Signal.
- **enable**: Enables the timer chain.
- **mode**: 2-bit input selecting timeout duration for LFSR1ms.
- **ReconfigTimer**: Re-initializes the LFSR timeout based on mode.

**Outputs**:

- **timeout**: High for one cycle every second when fully enabled.

**Functionality**:

- Generates a 1Hz (1-second) timeout pulse by chaining LFSR1ms, CountTo100, and CountTo10. When enabled, this module provides a consistent 1-second timing reference for countdown or control FSMs.

**Module**: digitTimer

**Inputs**:

- **clk**: Clock signal.
- **rst**: Reset Signal.
- **reconfig**: Sets the current digit value to 9 when high.
- **enable**: Enables the countdown operation.
- **BorrowDown**: Triggers a single countdown event when high.
- **NoBorrowUp**: Indicates whether the previous digit is allowed to borrow.

**Outputs**:

- **BorrowUp**: Asserted when the digit rolls under from 0 to 9, signaling the next digit to decrement.
- **NoBorrowDown**: Low when the current digit is at 0, preventing further borrowing.

**Functionality**:

- Implements a 0–9 single-digit countdown with rollover support. When enabled and triggered by BorrowDown, the digit decrements. If it rolls below 0, it resets to 9 and asserts BorrowUp. Used in multi-digit timers for cascading countdown behavior, with reconfig support for manual reset to 9.

**Module**: SevenSegmentDisplay
**Inputs**:
- **digit**: 4-bit binary digit (0–9),

**Outputs**:
- **seg**: 7-bit output controlling segments a–g of the display.

**Functionality**:
- Combinational decoder that translates a 4-bit binary digit into the corresponding 7-segment pattern for decimal display. The output seg determines which segments light up to represent digits 0–9 on a common-cathode or common-anode 7-segment display.

**Module**: VGATextRenderer
**Inputs**:
- **clk**: 25 MHz VGA clock.
- **rst**: Reset signal.
- **LoggedIn**: High when the user has successfully logged in.
- **CheckPassword**: Indicates system is in password check phase.
- **enable**: When high, disables the screen output.
- **GameTimeout**: Indicates game session has ended.
- **Points**: 4-bit score input used to select displayed word or final score.

**Outputs**:
- **hsync**: Horizontal sync signal for VGA.
- **vsync**: Vertical sync signal for VGA.
- **red**: 4-bit red video output.
- **green**: 4-bit green video output.
- **blue**: 4-bit blue video output.
-

**Functionality**:
- Renders ASCII text to a VGA display based on the system state. Displays login prompts, active game word (from Points), and final score at game end. Uses a character ROM and internal counters to map characters to pixel output for standard 640×480 VGA resolution.

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## Simulation Results

### 1. Timer Modules (LFSR1ms, CountTo100, CountTo10, OneSecTimer, digitTimer)

**Objective**:
- Verify correct timing behavior and cascade interaction among the timer modules to produce accurate 1-second pulses and countdown logic

**Key Observations**:

- **LFSR1ms**: Successfully generated a pseudo-random timeout based on the selected mode. Timeout pulses occurred after the configured number of clock cycles. On ReconfigTimer, the internal TimeoutNumber was correctly updated, and the LFSR reset to 0x1FFFF.
- **CountTo100 & CountTo10**: Properly chained with LFSR1ms. CountTo100 generated a pulse every 100 rising edges of LFSR1ms.timeout. In turn, CountTo10 triggered once every 10 CountTo100.timeouts, accurately producing a 1-second timeout.

- **CountTo100 & CountTo10**: Properly chained with LFSR1ms. CountTo100 generated a pulse every 100 rising edges of LFSR1ms.timeout. In turn, CountTo10 triggered once every 10 CountTo100.timeouts, accurately producing a 1-second timeout.

- **OneSecTimer**: As expected, emitted a single-cycle timeout every 1 second (assuming the LFSR base frequency is scaled correctly). When enable was deasserted, no timeouts were generated. The ReconfigTimer pulse correctly restarted the internal cascade.
- **digitTimer**: Decremented the displayed digit on each BorrowDown edge while enable was high. Reset to 9 when reconfig was asserted. Correctly rolled over to 9 and set BorrowUp when the digit reached 0

**Conclusion**:

- All timing modules functioned accurately in isolation and when integrated. Timing pulses were properly spaced, cascaded counters functioned as expected, and control signals (enable, reconfig) correctly affected output behavior.

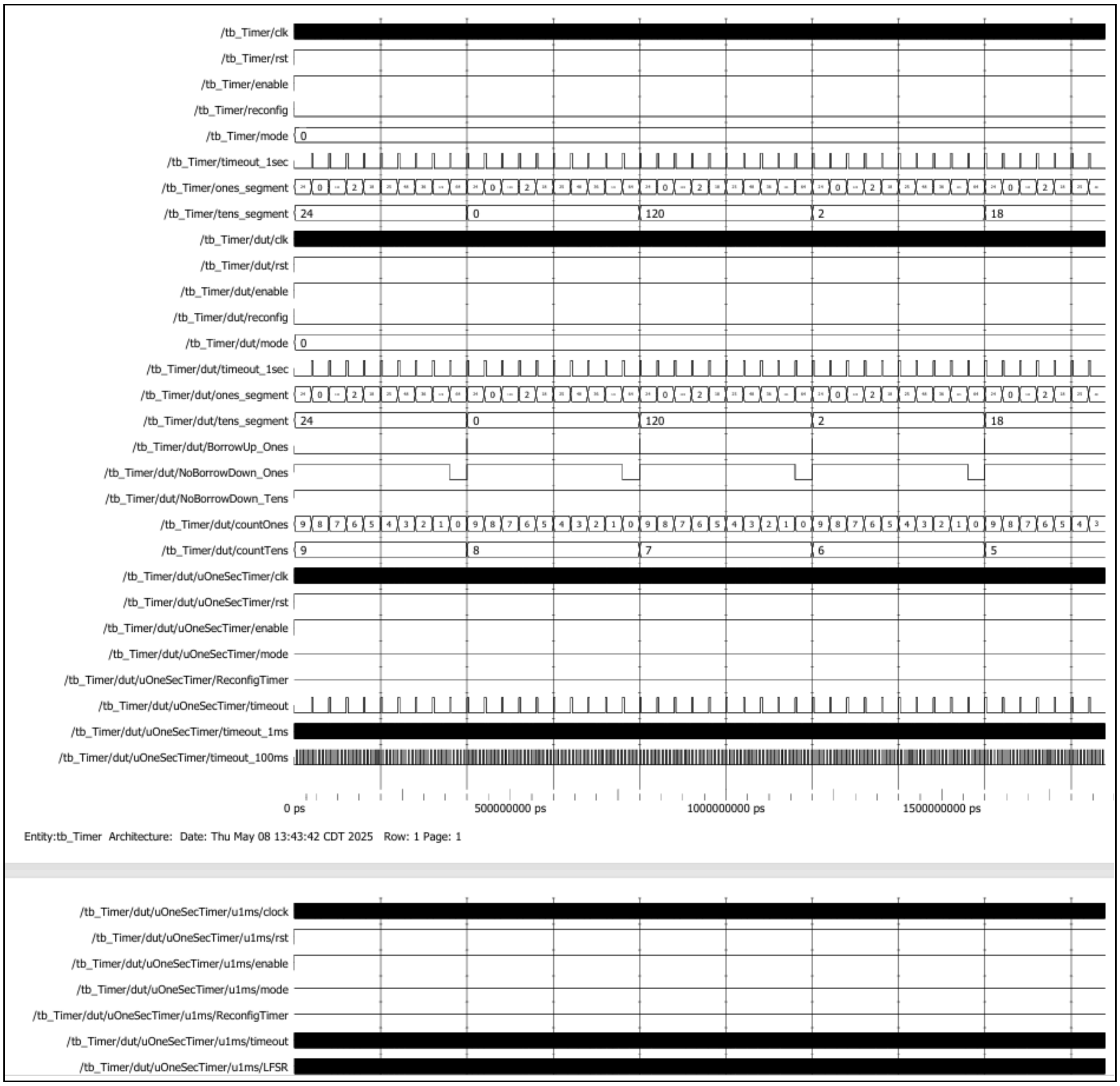

/tb_Timer/clk
/tb_Timer/rst
/tb_Timer/enable
/tb_Timer/reconfig
/tb_Timer/mode
/tb_Timer/timeout_1sec
/tb_Timer/ones_segment
/tb_Timer/tens_segment
/tb_Timer/dut/clk
/tb_Timer/dut/rst
/tb_Timer/dut/enable
/tb_Timer/dut/reconfig
/tb_Timer/dut/mode
/tb_Timer/dut/timeout_1sec
/tb_Timer/dut/ones_segment
/tb_Timer/dut/tens_segment
/tb_Timer/dut/BorrowUp_Ones
/tb_Timer/dut/NoBorrowDown_Ones
/tb_Timer/dut/NoBorrowDown_Tens
/tb_Timer/dut/countOnes
/tb_Timer/dut/countTens
/tb_Timer/dut/uOneSecTimer/clk
/tb_Timer/dut/uOneSecTimer/rst
/tb_Timer/dut/uOneSecTimer/enable
/tb_Timer/dut/uOneSecTimer/mode
/tb_Timer/dut/uOneSecTimer/ReconfigTimer
/tb_Timer/dut/uOneSecTimer/timeout
/tb_Timer/dut/uOneSecTimer/timeout_1ms
/tb_Timer/dut/uOneSecTimer/timeout_100ms
0 ps
500000000 ps
1000000000 ps
1500000000 ps
Entity:tb_Timer Architecture: Date: Thu May 08 13:43:42 CDT 2025 Row: 1 Page: 1
/tb_Timer/dut/uOneSecTimer/u1ms/clock
/tb_Timer/dut/uOneSecTimer/u1ms/rst
/tb_Timer/dut/uOneSecTimer/u1ms/enable
/tb_Timer/dut/uOneSecTimer/u1ms/mode
/tb_Timer/dut/uOneSecTimer/u1ms/ReconfigTimer
/tb_Timer/dut/uOneSecTimer/u1ms/timeout
/tb_Timer/dut/uOneSecTimer/u1ms/LFSR

**Figure 3:** Timer Modules Simulation.

**2. Authentication (ROM_ID, ROM_PSWD, Identification, Password, ButtonShaper, LoadRegister)**

**Objective**:

- Verify successful multi-user login flow, including ID/password matching using ROMs and per-digit verification indicators.

**Key Observations**:

- **ROM_ID and ROM_PSWD**: Correctly output 4-bit stored digits upon address input changes. ROM access was synchronous with the clock and matched expected values from mem initialization
- **LoadRegister**: Latched switch input data only when load was high. Output (D_out) was stable and held across clock cycles until reloaded.
- **ButtonShaper**: Converted noisy B_in pulses into clean, single-cycle B_out pulses. Prevented multiple detections of a single press in the testbench waveform.
- **Identification FSM**:
  Processed four sequential digits. When a correct ID was entered, MatchedID was set, and CheckPassword was asserted.
    - If digits mismatched or timeout asserted, FSM returned to idle.
    - letterLEDs correctly reflected per-digit correctness.
- **Password FSM**: Enabled after CheckPassword. Stored four digits, compared them against ROM_PSWD at MatchedID. Asserted LoggedIn on full match.
    - Incorrect entries reset state machine.
    - letterLEDs showed which digits were matched in real time.
    - DoneChecking pulsed to signal completion.

**Conclusion**:
- Authentication simulation confirmed proper sequential behavior, signal gating, ROM access, and LED feedback. Edge cases like early timeout and incorrect ID/password were also validated.

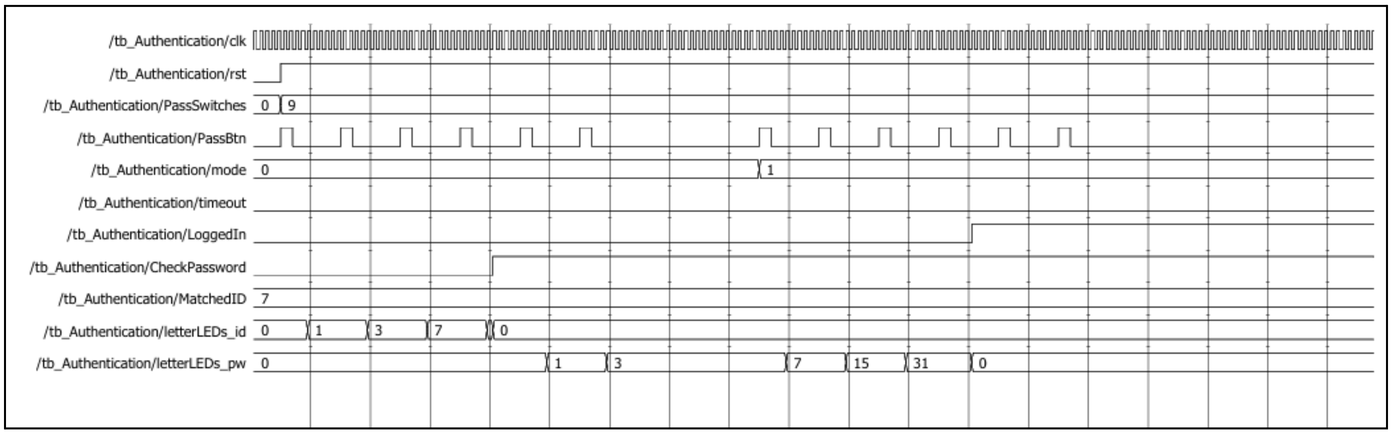


**Figure 4:** Authentication Modules Simulation.

## 3. Game Access Control (GameController)

**Objective**:
- Validate that the game starts upon correct authentication and PassEnter, and ends on Timeout.

**Key Observations**:
- FSM transitioned from IDLE → RUN → TIMEOUT as expected.

- enable was asserted only in the RUN state, allowing Morse input.
- When Timeout was pulsed, FSM entered the TIMEOUT state and asserted ReconfigTimer.
- FSM reset back to IDLE after a logout button hold (as simulated).

**Conclusion**:

- GameController responded to state changes correctly and issued the appropriate control signals to timer, decoder, and word generator modules.

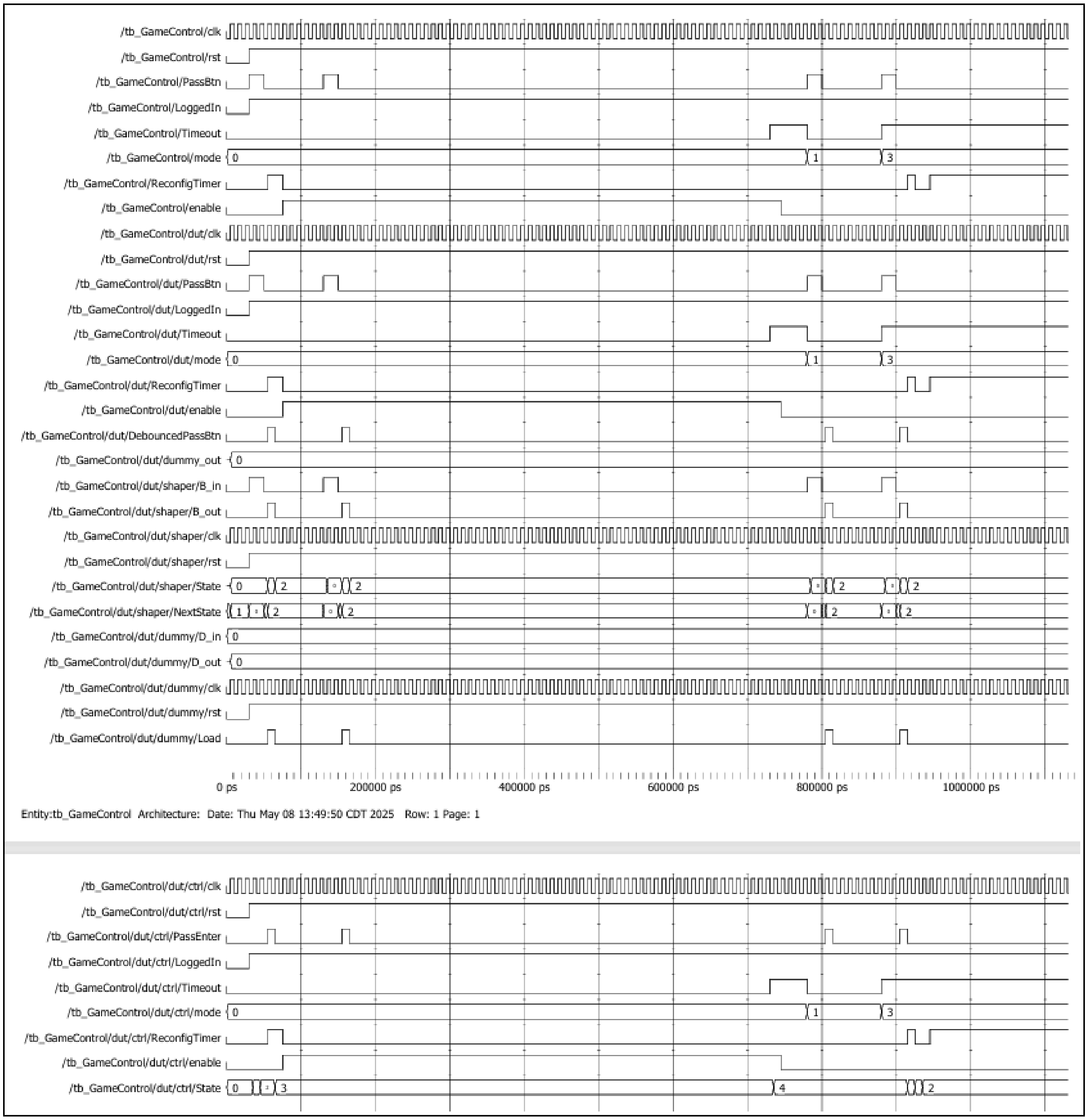


**Figure 5:** Game Control Modules Simulation.

### 4. Decoding (Load4x2bit + MorseDecoder)

**Objective:**

- Verify that user button inputs are correctly packed and decoded into ASCII letters.

**Key Observations:**

- **Load4x2bit:** Collected four 2-bit in symbols on each load while enable was high. ready was asserted after fourth symbol, and out held the full 8-bit Morse code sequence.
- **MorseDecoder:** Decoded valid 8-bit Morse patterns into expected ASCII codes.
  - Example: {1, 3, 0, 0} (dot-dash-gap-gap) → "A"
  - Patterns not matching any letter (e.g., all gaps) resulted in no output or default ASCII (space).

**Conclusion:**

- Symbol packing and decoding worked correctly. Morse input logic properly timed and synchronized. Simulation validated that correct button sequences result in valid letter decoding.

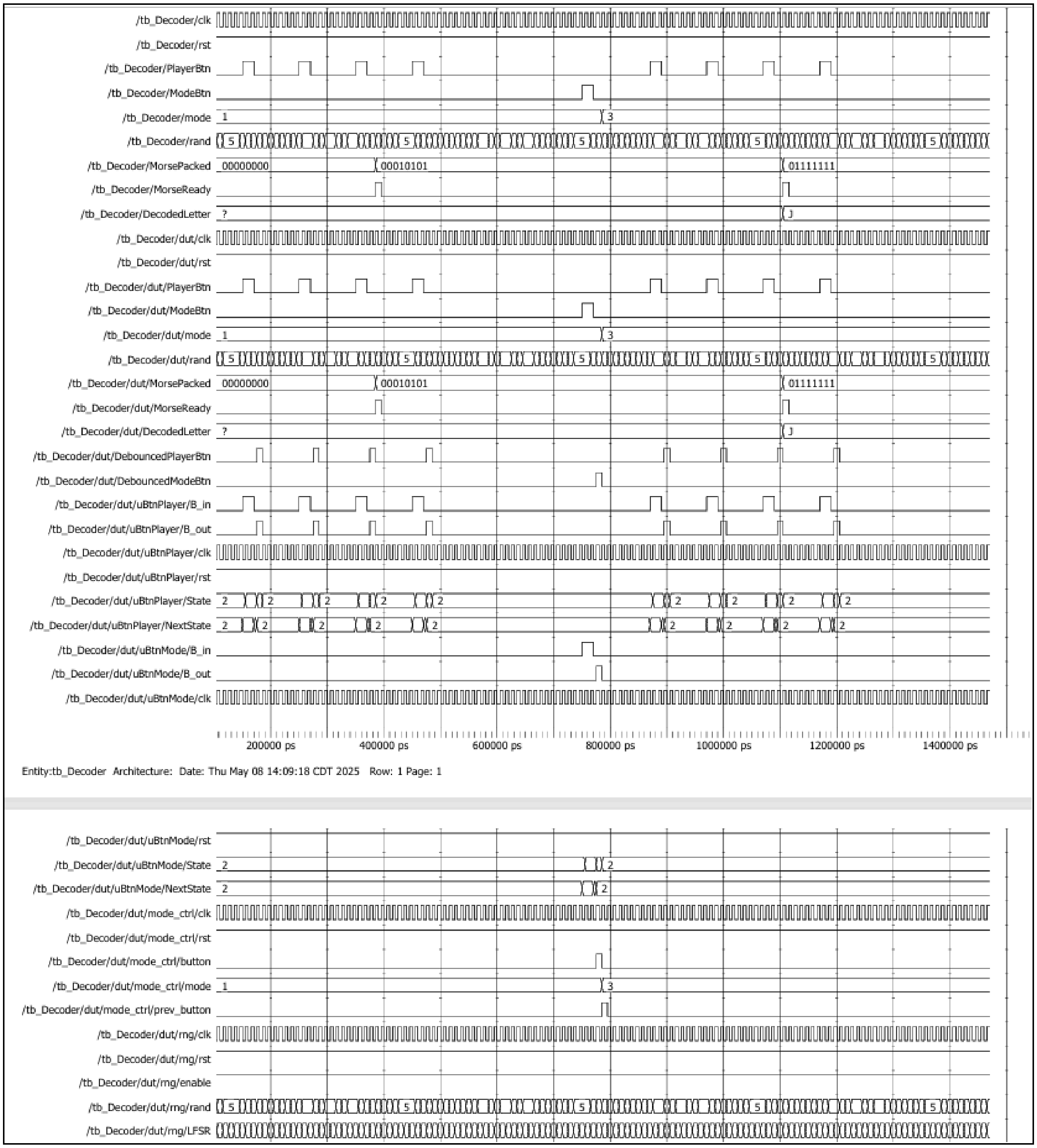


**Figure 6:** Decoder Modules Simulation.

**5. Matching and Output (CheckMatch)**

**Objective:**

- Ensure that decoded letters are compared to target word.

**Key Observations:**

- **CheckMatch:** On each LetterEnter, compared ASCIIOutput to expected letter from ROM_WORDS.
    - Correct letters triggered letterLEDs[x] = 1.
    - After 5 matches, Match pulsed and Points incremented.
    - HighScore updated only if Points exceeded previous best.
    - On incorrect entry, letterIndex reset and LEDs cleared.

**Conclusion:**

- Match logic, scoring, display, and feedback mechanisms worked as intended. Real-time feedback was accurate and responsive, and score tracking logic behaved correctly under repeated matches.

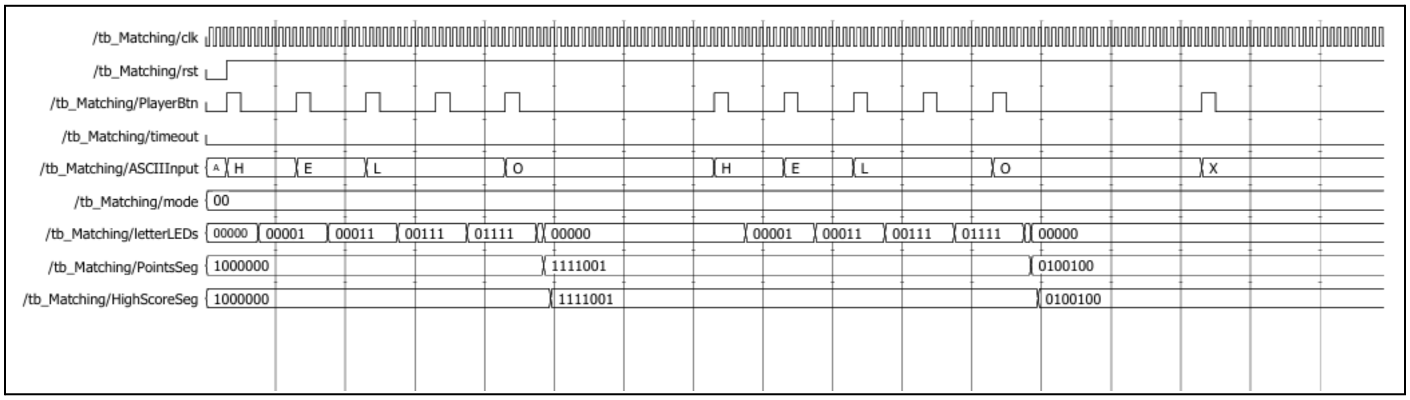


**Figure 7:** Matching Modules Simulation.

# FPGA Board Testing Results

The FPGA implementation of the Morse code training game was tested thoroughly in hardware to verify full functionality across all modules. Upon power-up, the system initialized correctly, holding at the login screen until a valid 4-digit ID and password were entered using physical switches and a shared input button. The Identification and Password FSMs accurately processed user entries, with ROM-stored data compared in real time and letterLEDs providing immediate feedback for each digit. Once authenticated, the GameController transitioned seamlessly into gameplay mode, activating VGA output and input control.

During gameplay, timer modules including LFSR1ms, CountTo100, CountTo10, and OneSecTimer worked in cascade to produce reliable 1-second pulses, verified visually through the countdown on the seven-segment display. The digitTimer module correctly managed countdown logic with rollover and borrow behavior observable through connected LED chains. Users entered Morse code symbols using physical buttons for dot and dash; each symbol was latched via Load4x2bit, packed, and decoded through the MorseDecoder. Correct sequences generated accurate ASCII output, which was displayed on VGA alongside the current target word.

Each decoded letter was checked against the expected ROM_WORDS output via the CheckMatch module. Matches were reflected in letterLEDs, with the Match signal and Points counter incrementing only after all five letters were entered correctly. High scores persisted across rounds and were displayed on both the seven-segment display and VGA screen. All subsystems performed consistently with simulation results, confirming the full correctness of the design in a live FPGA environment.

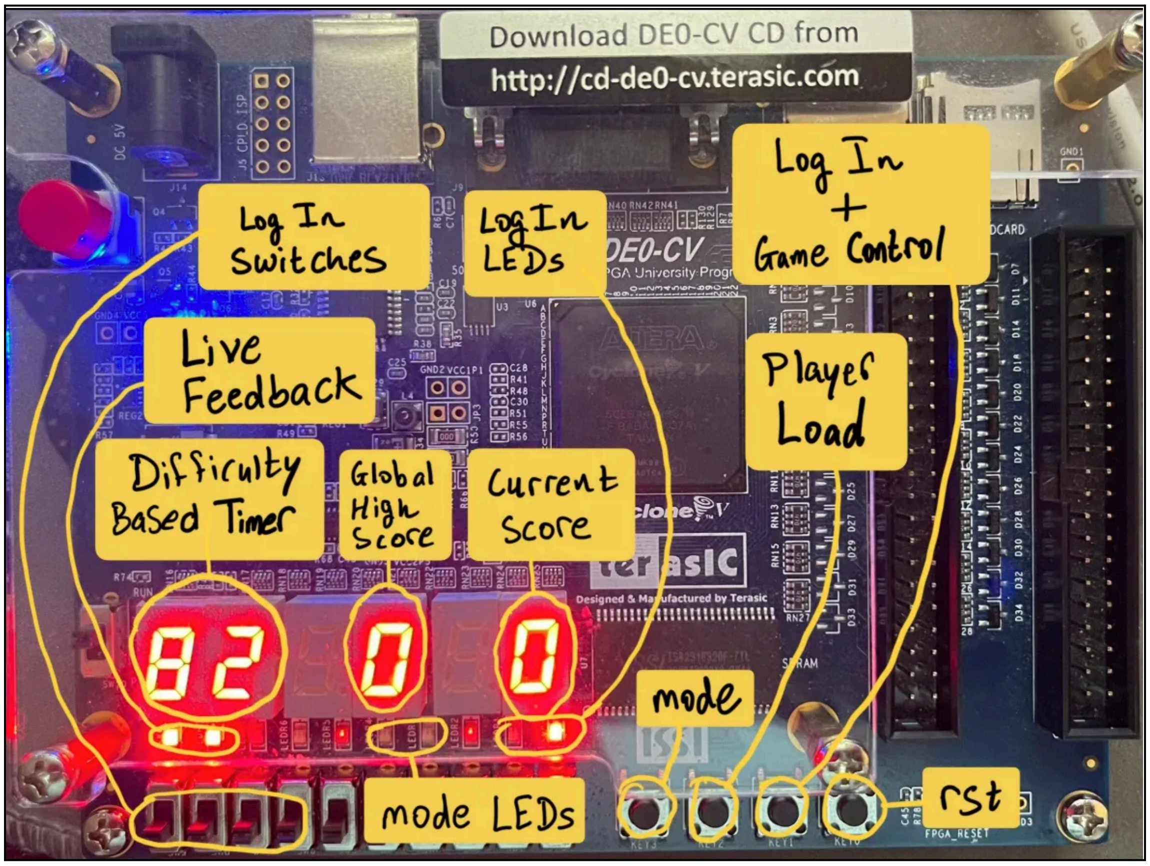


**Figure 8:** FPGA for CodeBreaker Game.

## Conclusion

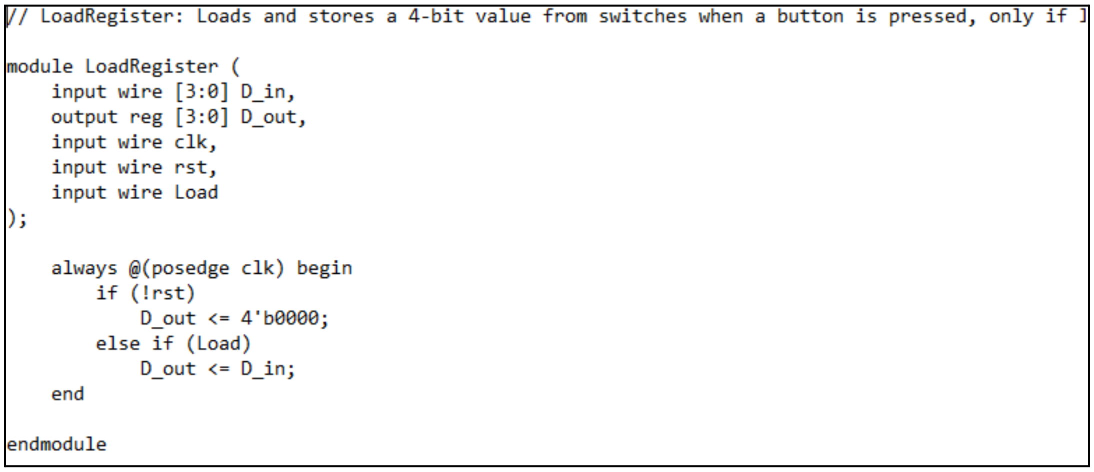
This project implemented a complete FPGA-based Morse code training game using Verilog on the DE0-CV development board. The system integrated secure multi-user authentication, real-time Morse code decoding, ROM-based word storage, and VGA output rendering, forming a cohesive timed gameplay experience. At startup, users were prompted to enter a 4-digit ID and a corresponding 4-digit password. These values were verified through finite state machines that compared each digit against ROM-stored credentials, with per-digit feedback displayed through a 5-bit LED array. Upon successful login, the GameController transitioned the system to active gameplay.

The game selected a random five-letter word from one of three difficulty levels using a mode-controlled ROM and a pseudo-random index generator. This word was stored internally and rendered on the VGA display one letter at a time. Users entered Morse code through physical buttons mapped to dot and dash inputs. Each input was packed into a 4-symbol sequence using the Load4x2bit module and then decoded via a combinational MorseDecoder. A decoded ASCII character was displayed on VGA, and the system compared each letter to the expected word using the CheckMatch module. Per-letter correctness was indicated in real time using LEDs, and once all five letters were entered correctly, a point was awarded. The Points counter tracked game progress, and the system updated and retained the HighScore throughout the session.

Timing control was handled through a cascaded system of modules: LFSR1ms generated a pseudo-random timing base, which was scaled through CountTo100 and CountTo10 to create a precise 1 Hz signal. This fed into a OneSecTimer module that counted down a 2-minute session using a pair of digitTimer modules, with output shown on dual 7-segment displays. The timer was reconfigurable and reset upon logout or game end.
All modules—ranging from authentication to input decoding, word matching, score tracking, timing logic, and output drivers—were designed modularly, verified through waveform simulation, and tested thoroughly on hardware. The system handled invalid inputs, partial sequences, logout requests, and timeout events with stable and predictable behavior. The VGA output provided real-time prompts, decoded feedback, and final score display, ensuring user engagement and clarity.

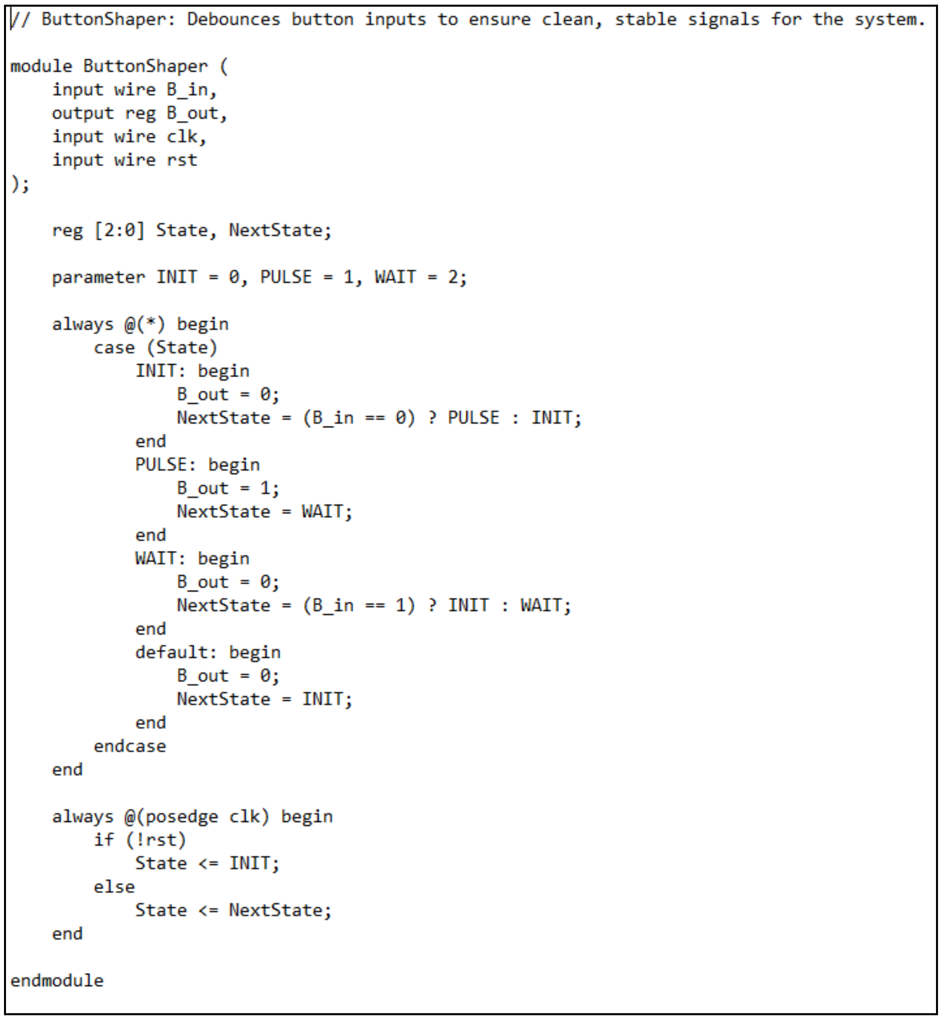
This lab reinforced advanced digital design principles including modular FSM development, hierarchical timing control, memory-mapped word selection, signal synchronization, and user interface implementation. The final hardware validation confirmed that all functional and timing requirements were met, making the project a complete, robust real-time training platform that demonstrated deep integration of control logic, data flow, and hardware-driven interaction.

# Appendix



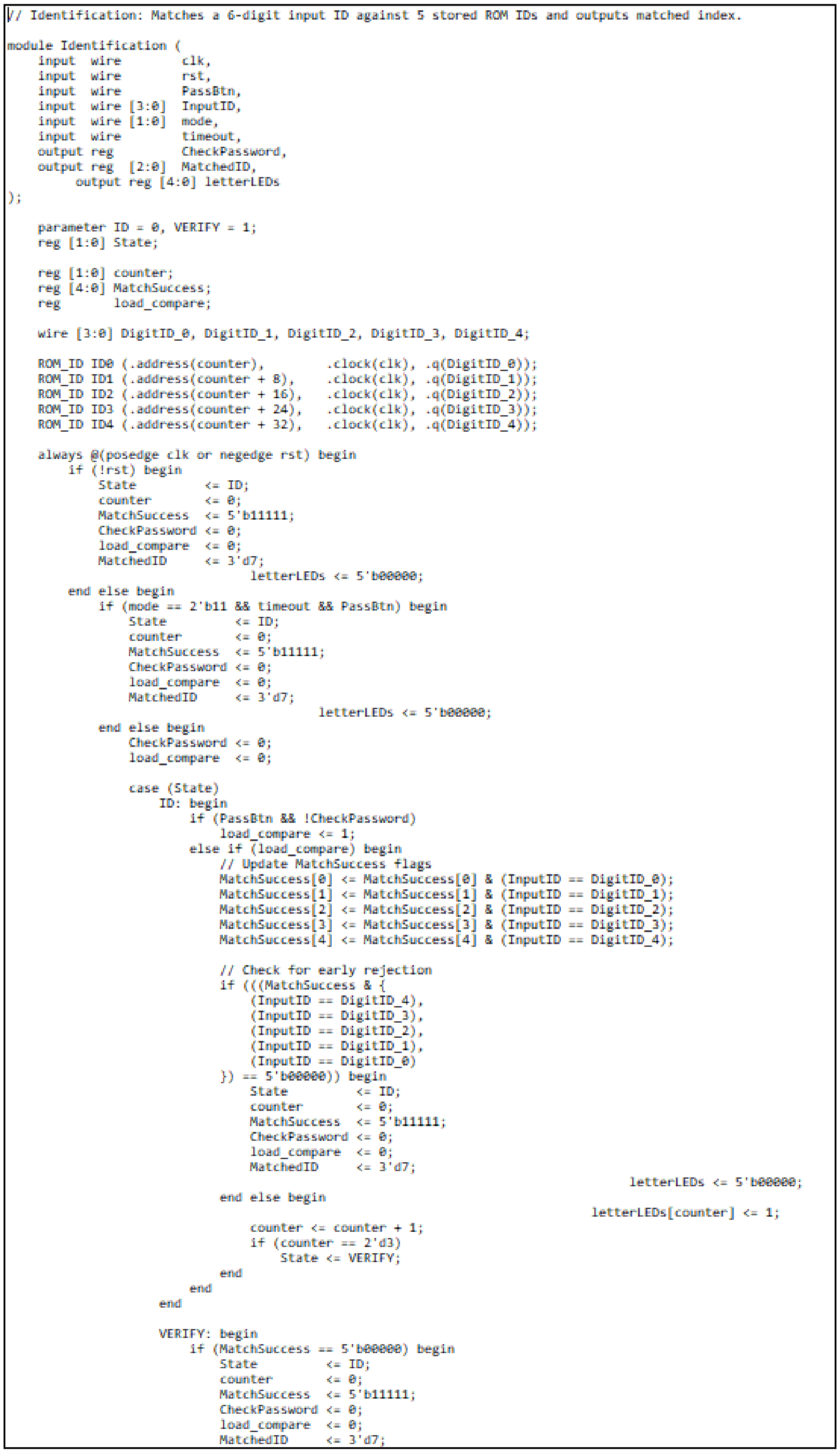
```
// LoadRegister: Loads and stores a 4-bit value from switches when a button is pressed, only if

module LoadRegister (
    input wire [3:0] D_in,
    output reg [3:0] D_out,
    input wire clk,
    input wire rst,
    input wire Load
);

    always @(posedge clk) begin
        if (!rst)
            D_out <= 4'b0000;
        else if (Load)
            D_out <= D_in;
    end

endmodule
```

**Figure 9:** Verilog Code for LoadRegister.



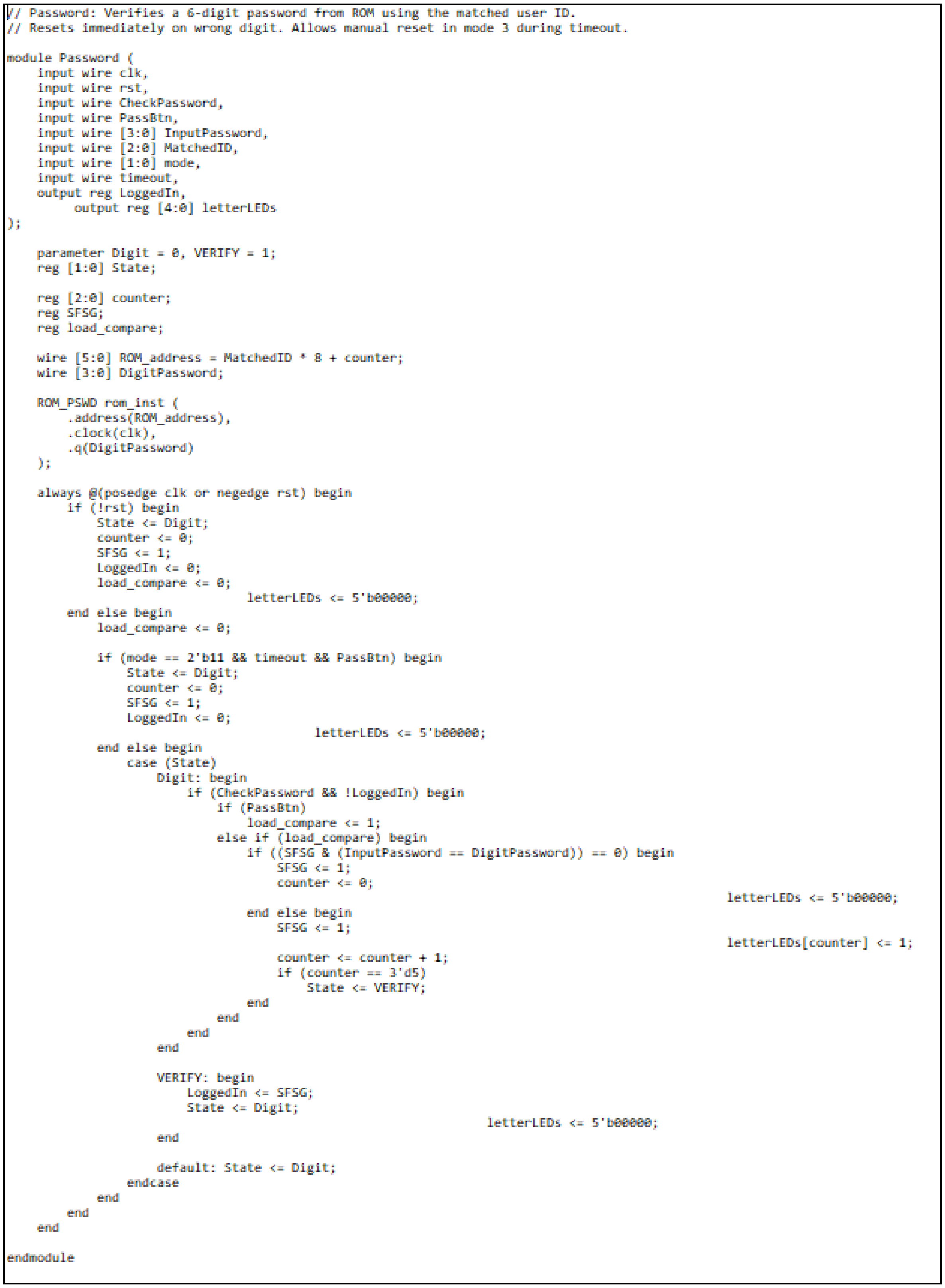
```
// ButtonShaper: Debounces button inputs to ensure clean, stable signals for the system.

module ButtonShaper (
    input wire B_in,
    output reg B_out,
    input wire clk,
    input wire rst
);

    reg [2:0] State, NextState;

    parameter INIT = 0, PULSE = 1, WAIT = 2;

    always @(*) begin
        case (State)
            INIT: begin
                B_out = 0;
                NextState = (B_in == 0) ? PULSE : INIT;
            end
            PULSE: begin
                B_out = 1;
                NextState = WAIT;
            end
            WAIT: begin
                B_out = 0;
                NextState = (B_in == 1) ? INIT : WAIT;
            end
            default: begin
                B_out = 0;
                NextState = INIT;
            end
        endcase
    end

    always @(posedge clk) begin
        if (!rst)
            State <= INIT;
        else
            State <= NextState;
    end

endmodule
```

**Figure 10:** Verilog Code for ButtonShaper.



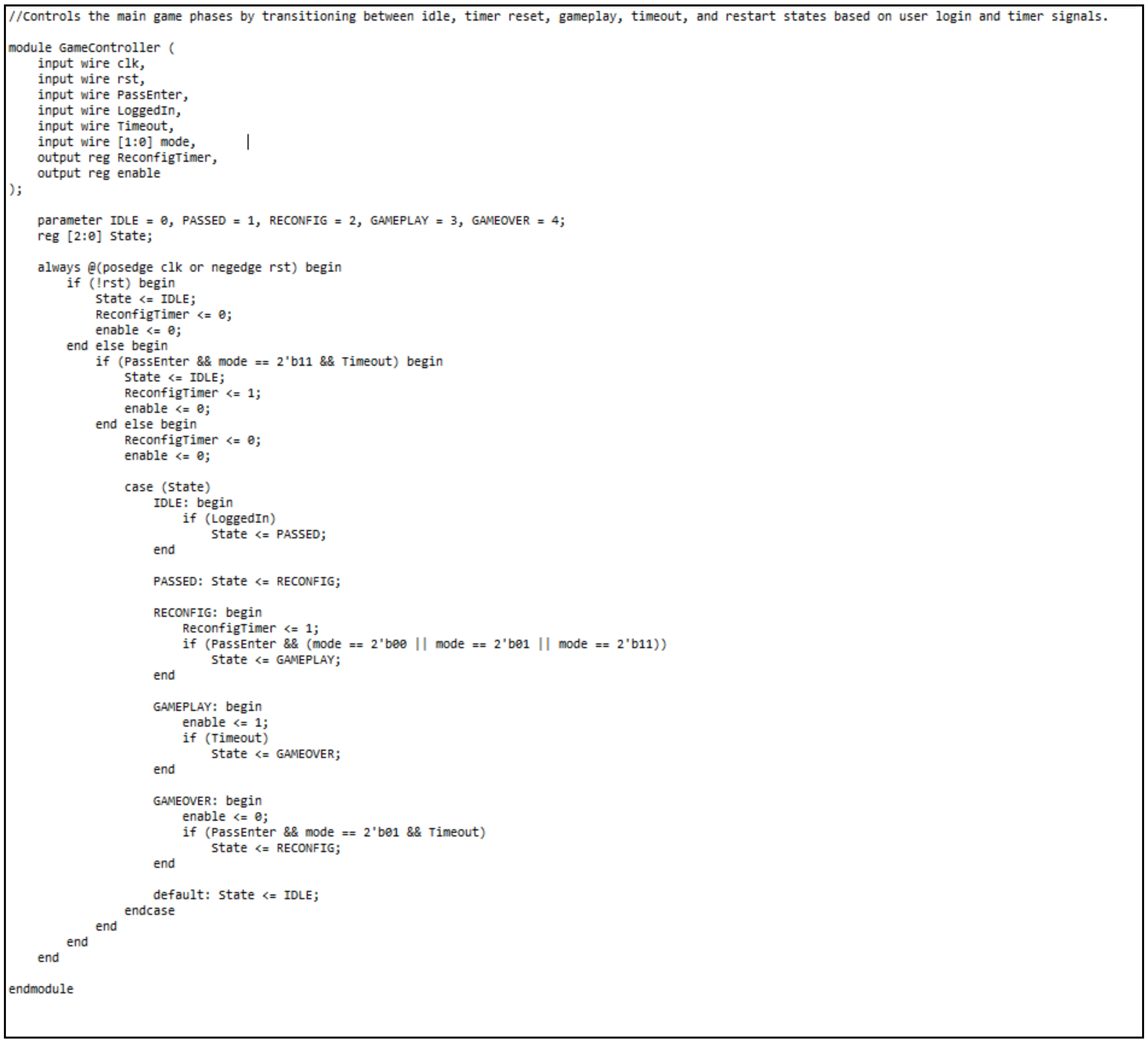
```verilog
// Identification: Matches a 6-digit input ID against 5 stored ROM IDs and outputs matched index.

module Identification (
    input  wire        clk,
    input  wire        rst,
    input  wire        PassBtn,
    input  wire [3:0]  InputID,
    input  wire [1:0]  mode,
    input  wire        timeout,
    output reg         CheckPassword,
    output reg  [2:0]  MatchedID,
         output reg [4:0] letterLEDs
);

    parameter ID = 0, VERIFY = 1;
    reg [1:0] State;

    reg [1:0] counter;
    reg [4:0] MatchSuccess;
    reg       load_compare;

    wire [3:0] DigitID_0, DigitID_1, DigitID_2, DigitID_3, DigitID_4;

    ROM_ID ID0 (.address(counter),        .clock(clk), .q(DigitID_0));
    ROM_ID ID1 (.address(counter + 8),    .clock(clk), .q(DigitID_1));
    ROM_ID ID2 (.address(counter + 16),   .clock(clk), .q(DigitID_2));
    ROM_ID ID3 (.address(counter + 24),   .clock(clk), .q(DigitID_3));
    ROM_ID ID4 (.address(counter + 32),   .clock(clk), .q(DigitID_4));

    always @(posedge clk or negedge rst) begin
        if (!rst) begin
            State         <= ID;
            counter       <= 0;
            MatchSuccess  <= 5'b11111;
            CheckPassword <= 0;
            load_compare  <= 0;
            MatchedID     <= 3'd7;
                                letterLEDs <= 5'b00000;
        end else begin
            if (mode == 2'b11 && timeout && PassBtn) begin
                State         <= ID;
                counter       <= 0;
                MatchSuccess  <= 5'b11111;
                CheckPassword <= 0;
                load_compare  <= 0;
                MatchedID     <= 3'd7;
                                         letterLEDs <= 5'b00000;
            end else begin
                CheckPassword <= 0;
                load_compare  <= 0;

                case (State)
                    ID: begin
                        if (PassBtn && !CheckPassword)
                            load_compare <= 1;
                        else if (load_compare) begin
                            // Update MatchSuccess flags
                            MatchSuccess[0] <= MatchSuccess[0] & (InputID == DigitID_0);
                            MatchSuccess[1] <= MatchSuccess[1] & (InputID == DigitID_1);
                            MatchSuccess[2] <= MatchSuccess[2] & (InputID == DigitID_2);
                            MatchSuccess[3] <= MatchSuccess[3] & (InputID == DigitID_3);
                            MatchSuccess[4] <= MatchSuccess[4] & (InputID == DigitID_4);

                            // Check for early rejection
                            if (((MatchSuccess & {
                                (InputID == DigitID_4),
                                (InputID == DigitID_3),
                                (InputID == DigitID_2),
                                (InputID == DigitID_1),
                                (InputID == DigitID_0)
                            }) == 5'b00000)) begin
                                State         <= ID;
                                counter       <= 0;
                                MatchSuccess  <= 5'b11111;
                                CheckPassword <= 0;
                                load_compare  <= 0;
                                MatchedID     <= 3'd7;
                                                                                letterLEDs <= 5'b00000;
                            end else begin
                                                                           letterLEDs[counter] <= 1;
                                counter <= counter + 1;
                                if (counter == 2'd3)
                                    State <= VERIFY;
                            end
                        end
                    end

                    VERIFY: begin
                        if (MatchSuccess == 5'b00000) begin
                            State         <= ID;
                            counter       <= 0;
                            MatchSuccess  <= 5'b11111;
                            CheckPassword <= 0;
                            load_compare  <= 0;
                            MatchedID     <= 3'd7;
```

**Figure 11:** Verilog Code for Identification.



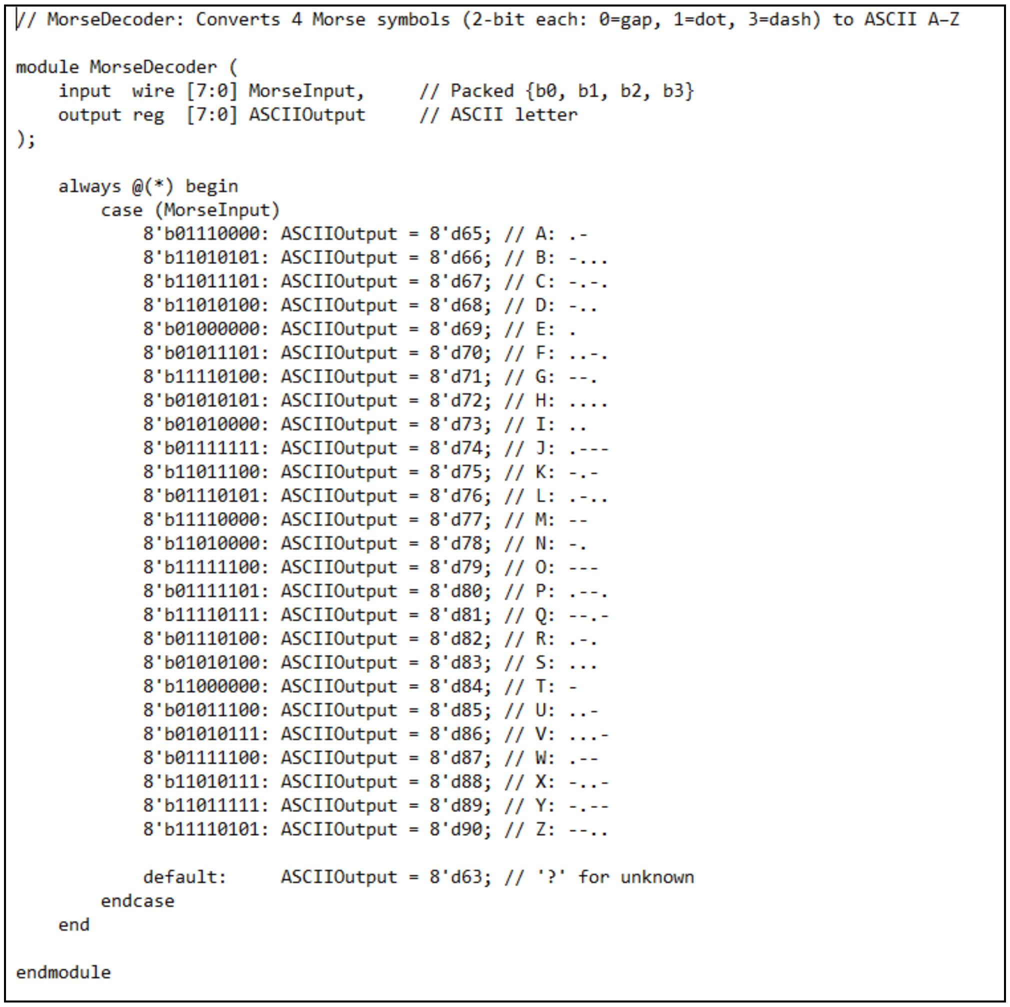
```
// Password: Verifies a 6-digit password from ROM using the matched user ID.
// Resets immediately on wrong digit. Allows manual reset in mode 3 during timeout.

module Password (
    input wire clk,
    input wire rst,
    input wire CheckPassword,
    input wire PassBtn,
    input wire [3:0] InputPassword,
    input wire [2:0] MatchedID,
    input wire [1:0] mode,
    input wire timeout,
    output reg LoggedIn,
         output reg [4:0] letterLEDs
);

    parameter Digit = 0, VERIFY = 1;
    reg [1:0] State;

    reg [2:0] counter;
    reg SFSG;
    reg load_compare;

    wire [5:0] ROM_address = MatchedID * 8 + counter;
    wire [3:0] DigitPassword;

    ROM_PSWD rom_inst (
        .address(ROM_address),
        .clock(clk),
        .q(DigitPassword)
    );

    always @(posedge clk or negedge rst) begin
        if (!rst) begin
            State <= Digit;
            counter <= 0;
            SFSG <= 1;
            LoggedIn <= 0;
            load_compare <= 0;
                                letterLEDs <= 5'b00000;
        end else begin
            load_compare <= 0;

            if (mode == 2'b11 && timeout && PassBtn) begin
                State <= Digit;
                counter <= 0;
                SFSG <= 1;
                LoggedIn <= 0;
                                         letterLEDs <= 5'b00000;
            end else begin
                case (State)
                    Digit: begin
                        if (CheckPassword && !LoggedIn) begin
                            if (PassBtn)
                                load_compare <= 1;
                            else if (load_compare) begin
                                if ((SFSG & (InputPassword == DigitPassword)) == 0) begin
                                    SFSG <= 1;
                                    counter <= 0;
                                                                                            letterLEDs <= 5'b00000;

                                end else begin
                                    SFSG <= 1;
                                                                                            letterLEDs[counter] <= 1;

                                    counter <= counter + 1;
                                    if (counter == 3'd5)
                                        State <= VERIFY;
                                end
                            end
                        end
                    end

                    VERIFY: begin
                        LoggedIn <= SFSG;
                        State <= Digit;
                                                                letterLEDs <= 5'b00000;
                    end

                    default: State <= Digit;
                endcase
            end
        end
    end

endmodule
```

**Figure 12:** Verilog Code for Password.



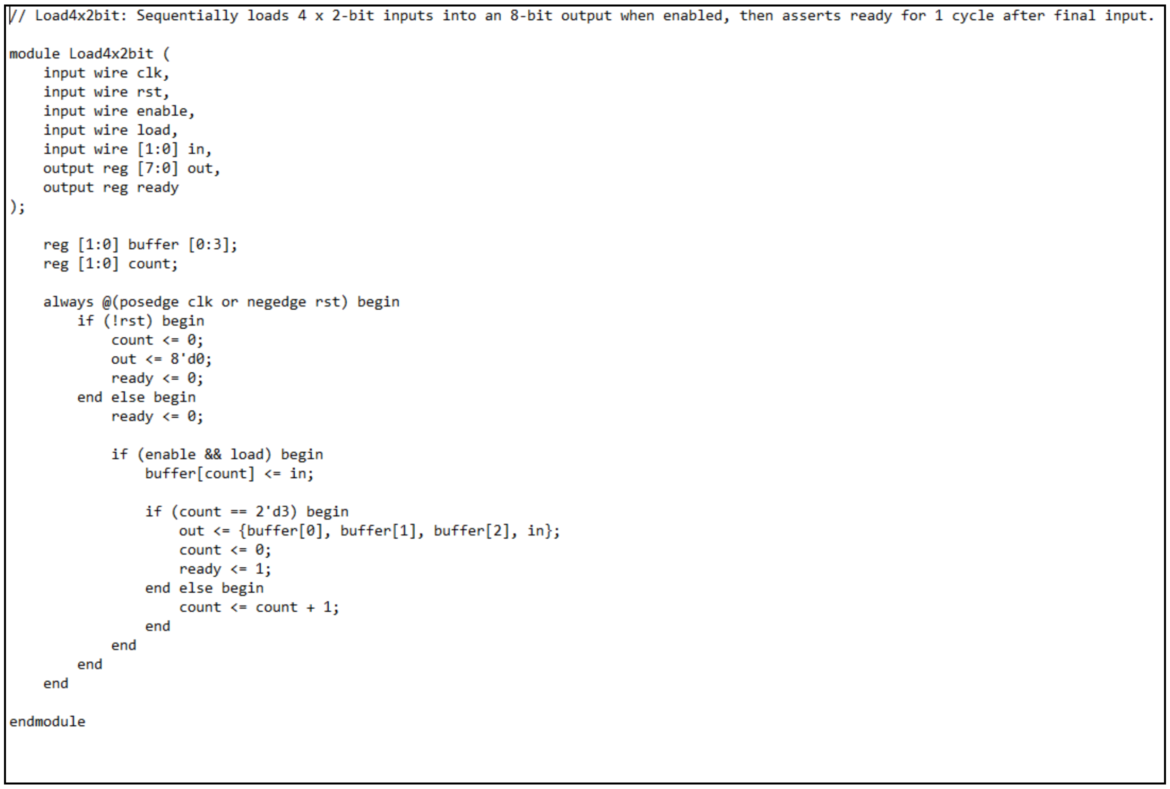
```verilog
//Controls the main game phases by transitioning between idle, timer reset, gameplay, timeout, and restart states based on user login and timer signals.

module GameController (
    input wire clk,
    input wire rst,
    input wire PassEnter,
    input wire LoggedIn,
    input wire Timeout,
    input wire [1:0] mode,
    output reg ReconfigTimer,
    output reg enable
);

    parameter IDLE = 0, PASSED = 1, RECONFIG = 2, GAMEPLAY = 3, GAMEOVER = 4;
    reg [2:0] State;

    always @(posedge clk or negedge rst) begin
        if (!rst) begin
            State <= IDLE;
            ReconfigTimer <= 0;
            enable <= 0;
        end else begin
            if (PassEnter && mode == 2'b11 && Timeout) begin
                State <= IDLE;
                ReconfigTimer <= 1;
                enable <= 0;
            end else begin
                ReconfigTimer <= 0;
                enable <= 0;

                case (State)
                    IDLE: begin
                        if (LoggedIn)
                            State <= PASSED;
                    end

                    PASSED: State <= RECONFIG;

                    RECONFIG: begin
                        ReconfigTimer <= 1;
                        if (PassEnter && (mode == 2'b00 || mode == 2'b01 || mode == 2'b11))
                            State <= GAMEPLAY;
                    end

                    GAMEPLAY: begin
                        enable <= 1;
                        if (Timeout)
                            State <= GAMEOVER;
                    end

                    GAMEOVER: begin
                        enable <= 0;
                        if (PassEnter && mode == 2'b01 && Timeout)
                            State <= RECONFIG;
                    end

                    default: State <= IDLE;
                endcase
            end
        end
    end

endmodule
```

**Figure 13:** Verilog Code for GameController.



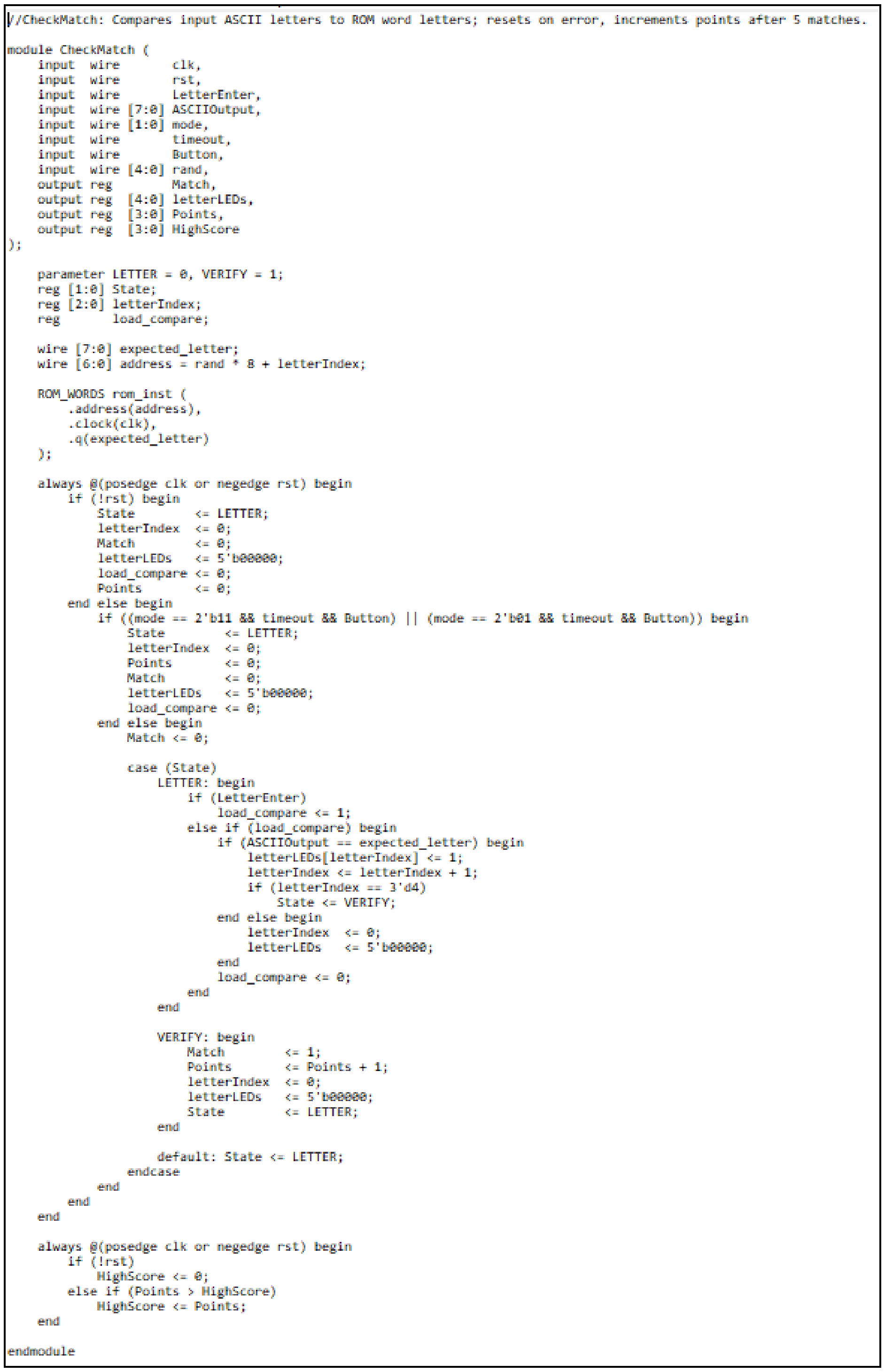
```verilog
// MorseDecoder: Converts 4 Morse symbols (2-bit each: 0=gap, 1=dot, 3=dash) to ASCII A-Z

module MorseDecoder (
    input  wire [7:0] MorseInput,     // Packed {b0, b1, b2, b3}
    output reg  [7:0] ASCIIOutput     // ASCII letter
);

    always @(*) begin
        case (MorseInput)
            8'b01110000: ASCIIOutput = 8'd65; // A: .-
            8'b11010101: ASCIIOutput = 8'd66; // B: -...
            8'b11011101: ASCIIOutput = 8'd67; // C: -.-.
            8'b11010100: ASCIIOutput = 8'd68; // D: -..
            8'b01000000: ASCIIOutput = 8'd69; // E: .
            8'b01011101: ASCIIOutput = 8'd70; // F: ..-.
            8'b11110100: ASCIIOutput = 8'd71; // G: --.
            8'b01010101: ASCIIOutput = 8'd72; // H: ....
            8'b01010000: ASCIIOutput = 8'd73; // I: ..
            8'b01111111: ASCIIOutput = 8'd74; // J: .---
            8'b11011100: ASCIIOutput = 8'd75; // K: -.-
            8'b01110101: ASCIIOutput = 8'd76; // L: .-..
            8'b11110000: ASCIIOutput = 8'd77; // M: --
            8'b11010000: ASCIIOutput = 8'd78; // N: -.
            8'b11111100: ASCIIOutput = 8'd79; // O: ---
            8'b01111101: ASCIIOutput = 8'd80; // P: .--.
            8'b11110111: ASCIIOutput = 8'd81; // Q: --.-
            8'b01110100: ASCIIOutput = 8'd82; // R: .-.
            8'b01010100: ASCIIOutput = 8'd83; // S: ...
            8'b11000000: ASCIIOutput = 8'd84; // T: -
            8'b01011100: ASCIIOutput = 8'd85; // U: ..-
            8'b01010111: ASCIIOutput = 8'd86; // V: ...-
            8'b01111100: ASCIIOutput = 8'd87; // W: .--
            8'b11010111: ASCIIOutput = 8'd88; // X: -..-
            8'b11011111: ASCIIOutput = 8'd89; // Y: -.--
            8'b11110101: ASCIIOutput = 8'd90; // Z: --..

            default:     ASCIIOutput = 8'd63; // '?' for unknown
        endcase
    end

endmodule
```

**Figure 14:** Verilog Code for MorseDecoder.



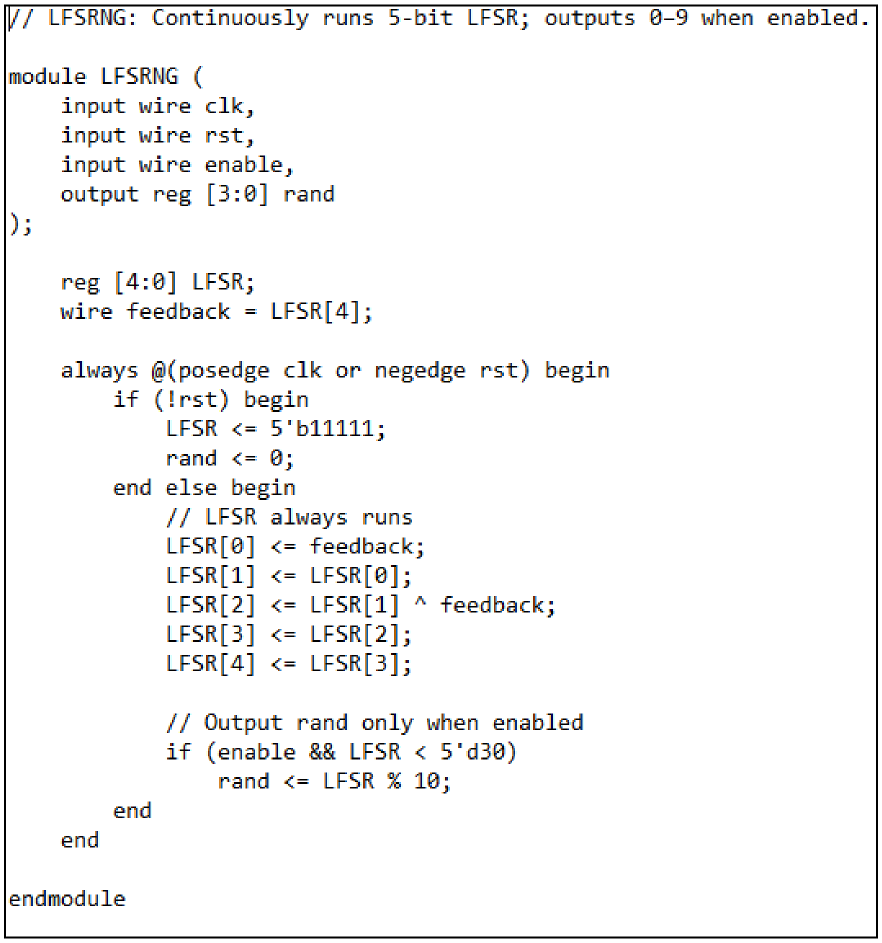
```
// Load4x2bit: Sequentially loads 4 x 2-bit inputs into an 8-bit output when enabled, then asserts ready for 1 cycle after final input.

module Load4x2bit (
    input wire clk,
    input wire rst,
    input wire enable,
    input wire load,
    input wire [1:0] in,
    output reg [7:0] out,
    output reg ready
);

    reg [1:0] buffer [0:3];
    reg [1:0] count;

    always @(posedge clk or negedge rst) begin
        if (!rst) begin
            count <= 0;
            out <= 8'd0;
            ready <= 0;
        end else begin
            ready <= 0;

            if (enable && load) begin
                buffer[count] <= in;

                if (count == 2'd3) begin
                    out <= {buffer[0], buffer[1], buffer[2], in};
                    count <= 0;
                    ready <= 1;
                end else begin
                    count <= count + 1;
                end
            end
        end
    end

endmodule
```

**Figure 15:** Verilog Code for Load4x2bit.



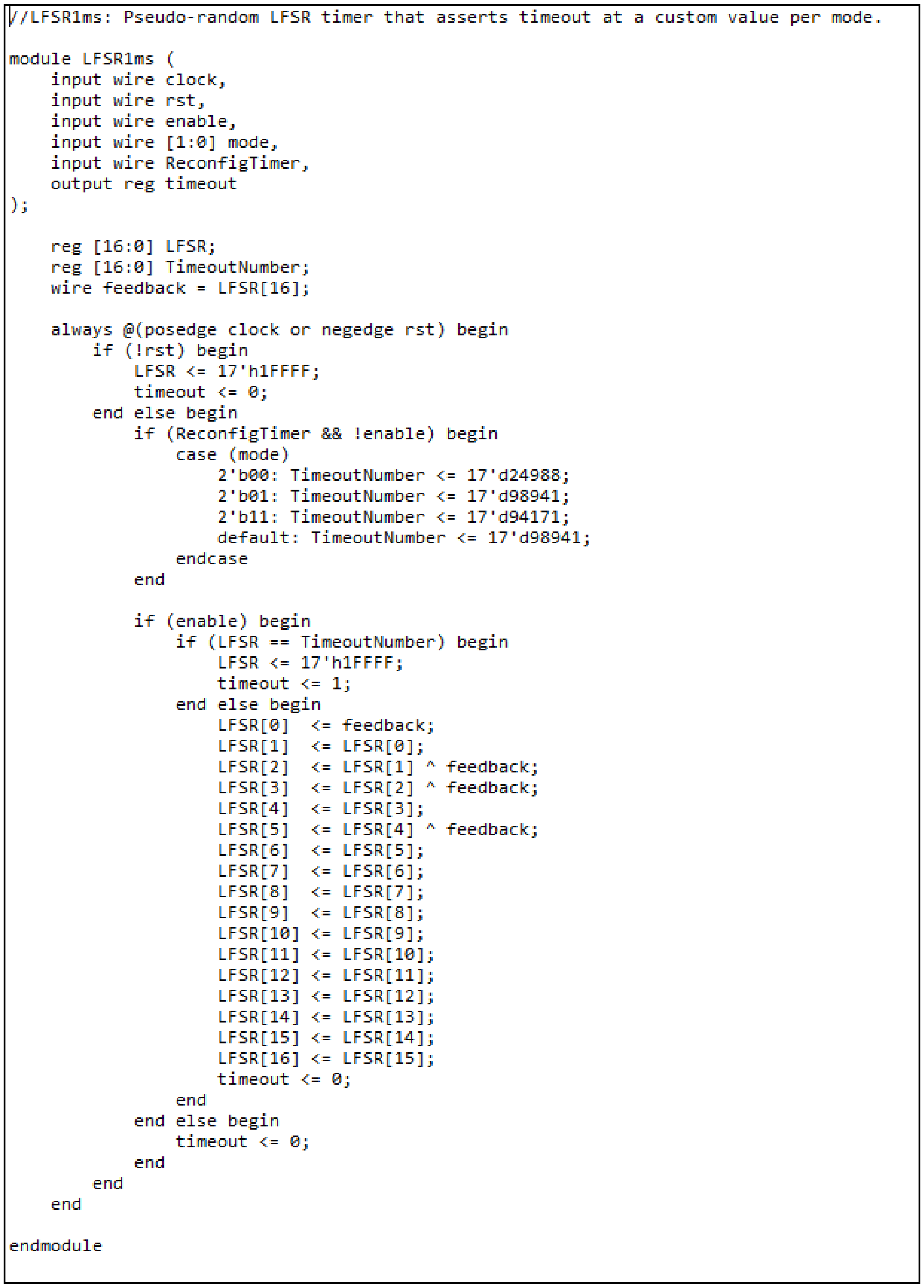
```verilog
//CheckMatch: Compares input ASCII letters to ROM word letters; resets on error, increments points after 5 matches.

module CheckMatch (
    input  wire       clk,
    input  wire       rst,
    input  wire       LetterEnter,
    input  wire [7:0] ASCIIOutput,
    input  wire [1:0] mode,
    input  wire       timeout,
    input  wire       Button,
    input  wire [4:0] rand,
    output reg        Match,
    output reg  [4:0] letterLEDs,
    output reg  [3:0] Points,
    output reg  [3:0] HighScore
);

    parameter LETTER = 0, VERIFY = 1;
    reg [1:0] State;
    reg [2:0] letterIndex;
    reg       load_compare;

    wire [7:0] expected_letter;
    wire [6:0] address = rand * 8 + letterIndex;

    ROM_WORDS rom_inst (
        .address(address),
        .clock(clk),
        .q(expected_letter)
    );

    always @(posedge clk or negedge rst) begin
        if (!rst) begin
            State        <= LETTER;
            letterIndex  <= 0;
            Match        <= 0;
            letterLEDs   <= 5'b00000;
            load_compare <= 0;
            Points       <= 0;
        end else begin
            if ((mode == 2'b11 && timeout && Button) || (mode == 2'b01 && timeout && Button)) begin
                State        <= LETTER;
                letterIndex  <= 0;
                Points       <= 0;
                Match        <= 0;
                letterLEDs   <= 5'b00000;
                load_compare <= 0;
            end else begin
                Match <= 0;

                case (State)
                    LETTER: begin
                        if (LetterEnter)
                            load_compare <= 1;
                        else if (load_compare) begin
                            if (ASCIIOutput == expected_letter) begin
                                letterLEDs[letterIndex] <= 1;
                                letterIndex <= letterIndex + 1;
                                if (letterIndex == 3'd4)
                                    State <= VERIFY;
                            end else begin
                                letterIndex  <= 0;
                                letterLEDs   <= 5'b00000;
                            end
                            load_compare <= 0;
                        end
                    end

                    VERIFY: begin
                        Match        <= 1;
                        Points       <= Points + 1;
                        letterIndex  <= 0;
                        letterLEDs   <= 5'b00000;
                        State        <= LETTER;
                    end

                    default: State <= LETTER;
                endcase
            end
        end
    end

    always @(posedge clk or negedge rst) begin
        if (!rst)
            HighScore <= 0;
        else if (Points > HighScore)
            HighScore <= Points;
    end

endmodule
```

**Figure 16:** Verilog Code for CheckMatch.



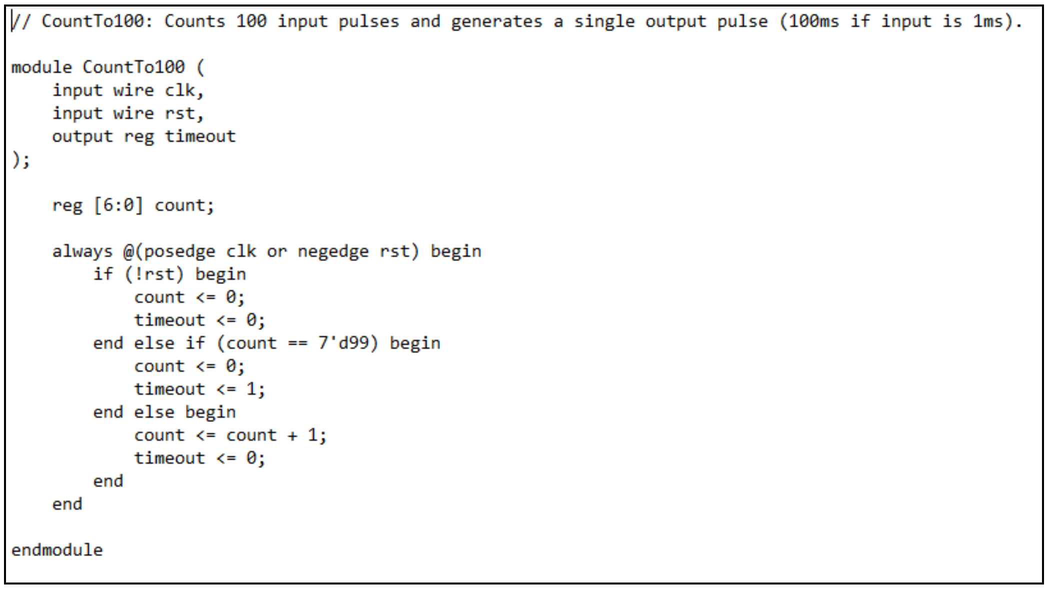
```verilog
// LFSRNG: Continuously runs 5-bit LFSR; outputs 0-9 when enabled.

module LFSRNG (
    input wire clk,
    input wire rst,
    input wire enable,
    output reg [3:0] rand
);

    reg [4:0] LFSR;
    wire feedback = LFSR[4];

    always @(posedge clk or negedge rst) begin
        if (!rst) begin
            LFSR <= 5'b11111;
            rand <= 0;
        end else begin
            // LFSR always runs
            LFSR[0] <= feedback;
            LFSR[1] <= LFSR[0];
            LFSR[2] <= LFSR[1] ^ feedback;
            LFSR[3] <= LFSR[2];
            LFSR[4] <= LFSR[3];

            // Output rand only when enabled
            if (enable && LFSR < 5'd30)
                rand <= LFSR % 10;
        end
    end

endmodule
```

**Figure 17:** Verilog Code for LFSRNG.



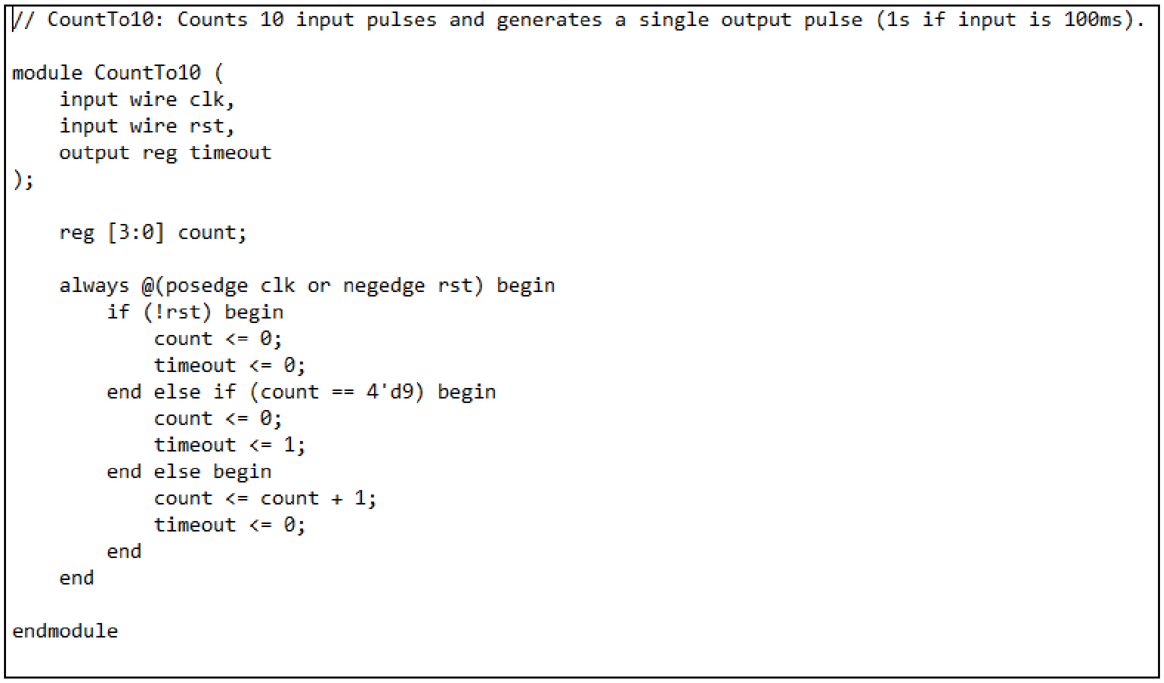
```
//LFSR1ms: Pseudo-random LFSR timer that asserts timeout at a custom value per mode.

module LFSR1ms (
    input wire clock,
    input wire rst,
    input wire enable,
    input wire [1:0] mode,
    input wire ReconfigTimer,
    output reg timeout
);

    reg [16:0] LFSR;
    reg [16:0] TimeoutNumber;
    wire feedback = LFSR[16];

    always @(posedge clock or negedge rst) begin
        if (!rst) begin
            LFSR <= 17'h1FFFF;
            timeout <= 0;
        end else begin
            if (ReconfigTimer && !enable) begin
                case (mode)
                    2'b00: TimeoutNumber <= 17'd24988;
                    2'b01: TimeoutNumber <= 17'd98941;
                    2'b11: TimeoutNumber <= 17'd94171;
                    default: TimeoutNumber <= 17'd98941;
                endcase
            end

            if (enable) begin
                if (LFSR == TimeoutNumber) begin
                    LFSR <= 17'h1FFFF;
                    timeout <= 1;
                end else begin
                    LFSR[0]  <= feedback;
                    LFSR[1]  <= LFSR[0];
                    LFSR[2]  <= LFSR[1] ^ feedback;
                    LFSR[3]  <= LFSR[2] ^ feedback;
                    LFSR[4]  <= LFSR[3];
                    LFSR[5]  <= LFSR[4] ^ feedback;
                    LFSR[6]  <= LFSR[5];
                    LFSR[7]  <= LFSR[6];
                    LFSR[8]  <= LFSR[7];
                    LFSR[9]  <= LFSR[8];
                    LFSR[10] <= LFSR[9];
                    LFSR[11] <= LFSR[10];
                    LFSR[12] <= LFSR[11];
                    LFSR[13] <= LFSR[12];
                    LFSR[14] <= LFSR[13];
                    LFSR[15] <= LFSR[14];
                    LFSR[16] <= LFSR[15];
                    timeout <= 0;
                end
            end else begin
                timeout <= 0;
            end
        end
    end

endmodule
```

**Figure 18:** Verilog Code for LFSR1ms.



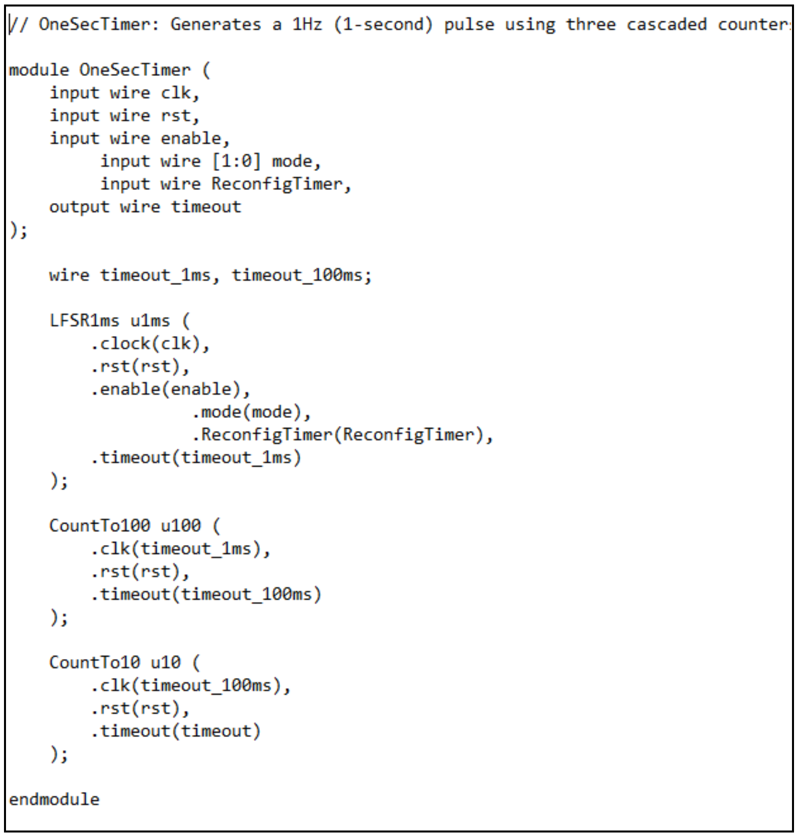
```verilog
// CountTo100: Counts 100 input pulses and generates a single output pulse (100ms if input is 1ms).

module CountTo100 (
    input wire clk,
    input wire rst,
    output reg timeout
);

    reg [6:0] count;

    always @(posedge clk or negedge rst) begin
        if (!rst) begin
            count <= 0;
            timeout <= 0;
        end else if (count == 7'd99) begin
            count <= 0;
            timeout <= 1;
        end else begin
            count <= count + 1;
            timeout <= 0;
        end
    end

endmodule
```

**Figure 19:** Verilog Code for CountTo100.



```verilog
// CountTo10: Counts 10 input pulses and generates a single output pulse (1s if input is 100ms).

module CountTo10 (
    input wire clk,
    input wire rst,
    output reg timeout
);

    reg [3:0] count;

    always @(posedge clk or negedge rst) begin
        if (!rst) begin
            count <= 0;
            timeout <= 0;
        end else if (count == 4'd9) begin
            count <= 0;
            timeout <= 1;
        end else begin
            count <= count + 1;
            timeout <= 0;
        end
    end

endmodule
```

**Figure 20:** Verilog Code for CountTo10.

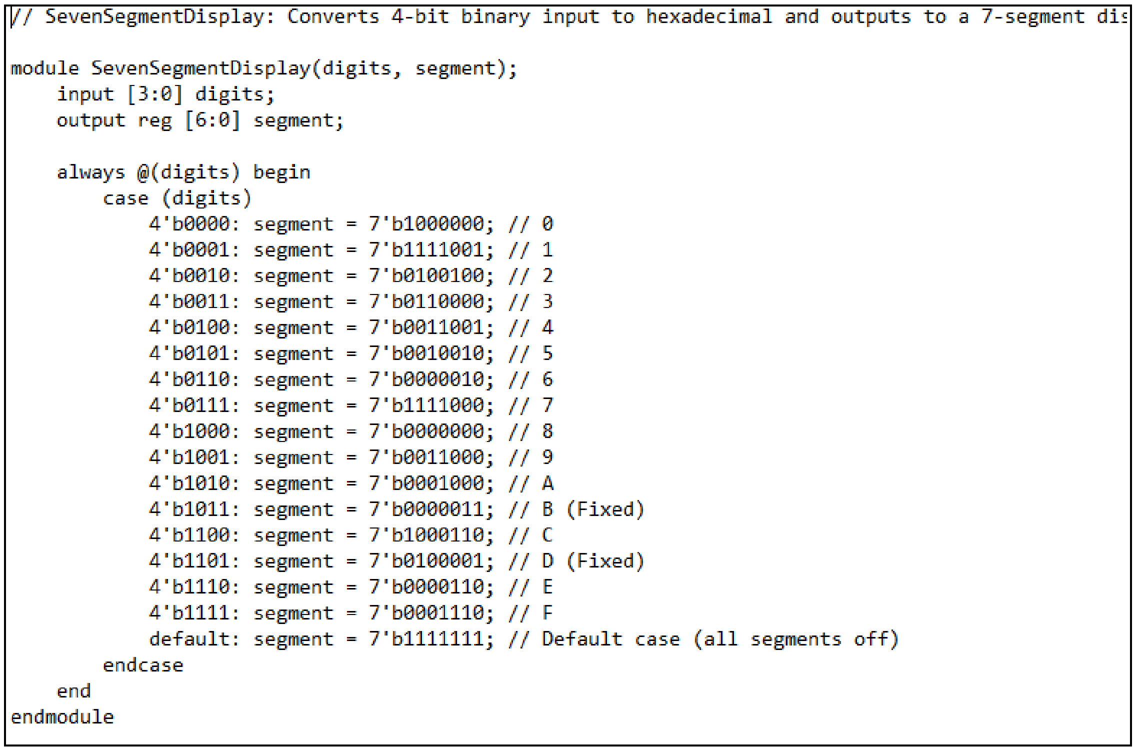


```
// OneSecTimer: Generates a 1Hz (1-second) pulse using three cascaded counter

module OneSecTimer (
    input wire clk,
    input wire rst,
    input wire enable,
         input wire [1:0] mode,
         input wire ReconfigTimer,
    output wire timeout
);

    wire timeout_1ms, timeout_100ms;

    LFSR1ms u1ms (
        .clock(clk),
        .rst(rst),
        .enable(enable),
                  .mode(mode),
                  .ReconfigTimer(ReconfigTimer),
        .timeout(timeout_1ms)
    );

    CountTo100 u100 (
        .clk(timeout_1ms),
        .rst(rst),
        .timeout(timeout_100ms)
    );

    CountTo10 u10 (
        .clk(timeout_100ms),
        .rst(rst),
        .timeout(timeout)
    );

endmodule
```

**Figure 21:** Verilog Code for OneSecTimer.

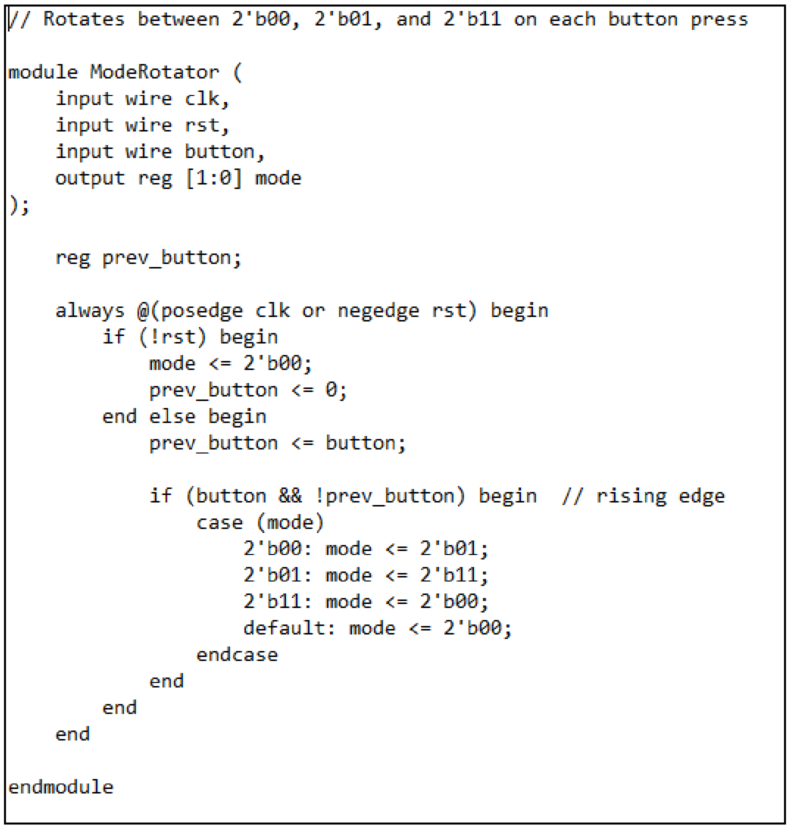
```verilog
// digitTimer: Single digit countdown timer with rollover and borrow signaling.
// Rolls from 0 to 9 and asserts BorrowUp. Reconfig sets digit to 9.

module digitTimer (
    input wire clk,
    input wire rst,
    input wire reconfig,
    input wire enable,
    input wire BorrowDown,
    input wire NoBorrowUp,
    output reg BorrowUp,
    output reg NoBorrowDown,
    output reg [3:0] Digit
);

    reg BorrowDown_prev;

    always @(posedge clk or negedge rst) begin
        if (!rst) begin
            Digit <= 4'd0;
            BorrowUp <= 0;
            NoBorrowDown <= 1;
            BorrowDown_prev <= 0;
        end else begin
            BorrowDown_prev <= BorrowDown;

            if (reconfig) begin
                Digit <= 4'd9;
                NoBorrowDown <= 1;
            end else if (enable && BorrowDown && !BorrowDown_prev) begin
                if (Digit == 0) begin
                    Digit <= 4'd9;
                    BorrowUp <= 1;
                    NoBorrowDown <= 1;
                end else begin
                    Digit <= Digit - 1;
                    BorrowUp <= 0;
                    NoBorrowDown <= (Digit - 1 != 0);
                end
            end else begin
                BorrowUp <= 0;
            end
        end
    end

endmodule
```

**Figure 22:** Verilog Code for digitTimer.



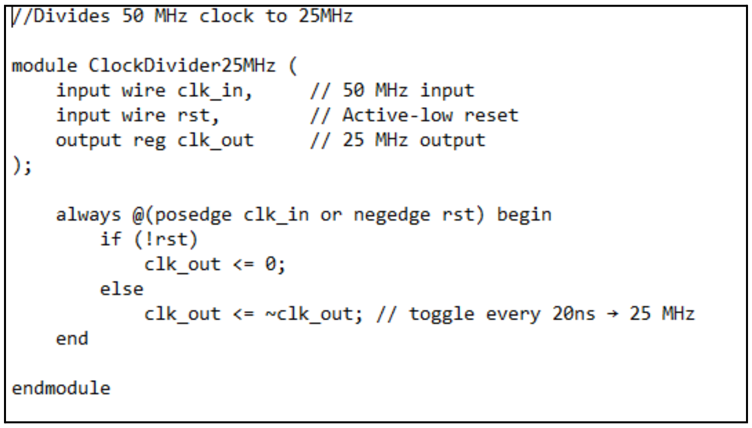
```
// SevenSegmentDisplay: Converts 4-bit binary input to hexadecimal and outputs to a 7-segment dis

module SevenSegmentDisplay(digits, segment);
    input [3:0] digits;
    output reg [6:0] segment;

    always @(digits) begin
        case (digits)
            4'b0000: segment = 7'b1000000; // 0
            4'b0001: segment = 7'b1111001; // 1
            4'b0010: segment = 7'b0100100; // 2
            4'b0011: segment = 7'b0110000; // 3
            4'b0100: segment = 7'b0011001; // 4
            4'b0101: segment = 7'b0010010; // 5
            4'b0110: segment = 7'b0000010; // 6
            4'b0111: segment = 7'b1111000; // 7
            4'b1000: segment = 7'b0000000; // 8
            4'b1001: segment = 7'b0011000; // 9
            4'b1010: segment = 7'b0001000; // A
            4'b1011: segment = 7'b0000011; // B (Fixed)
            4'b1100: segment = 7'b1000110; // C
            4'b1101: segment = 7'b0100001; // D (Fixed)
            4'b1110: segment = 7'b0000110; // E
            4'b1111: segment = 7'b0001110; // F
            default: segment = 7'b1111111; // Default case (all segments off)
        endcase
    end
endmodule
```

**Figure 23:** Verilog Code for SevenSegmentDisplay.



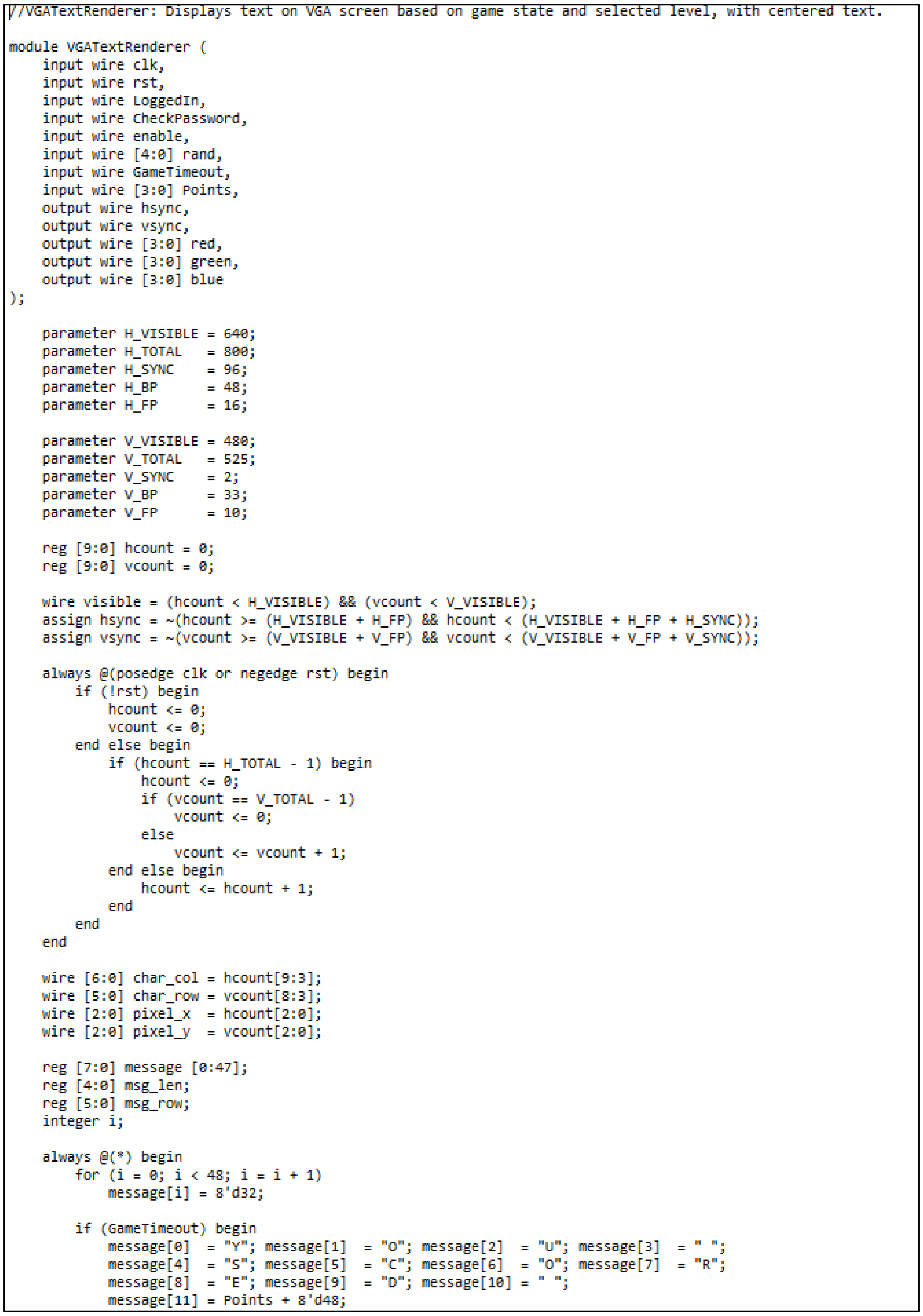
```
// Rotates between 2'b00, 2'b01, and 2'b11 on each button press

module ModeRotator (
    input wire clk,
    input wire rst,
    input wire button,
    output reg [1:0] mode
);

    reg prev_button;

    always @(posedge clk or negedge rst) begin
        if (!rst) begin
            mode <= 2'b00;
            prev_button <= 0;
        end else begin
            prev_button <= button;

            if (button && !prev_button) begin  // rising edge
                case (mode)
                    2'b00: mode <= 2'b01;
                    2'b01: mode <= 2'b11;
                    2'b11: mode <= 2'b00;
                    default: mode <= 2'b00;
                endcase
            end
        end
    end

endmodule
```

**Figure 23:** Verilog Code for ModeRotator.



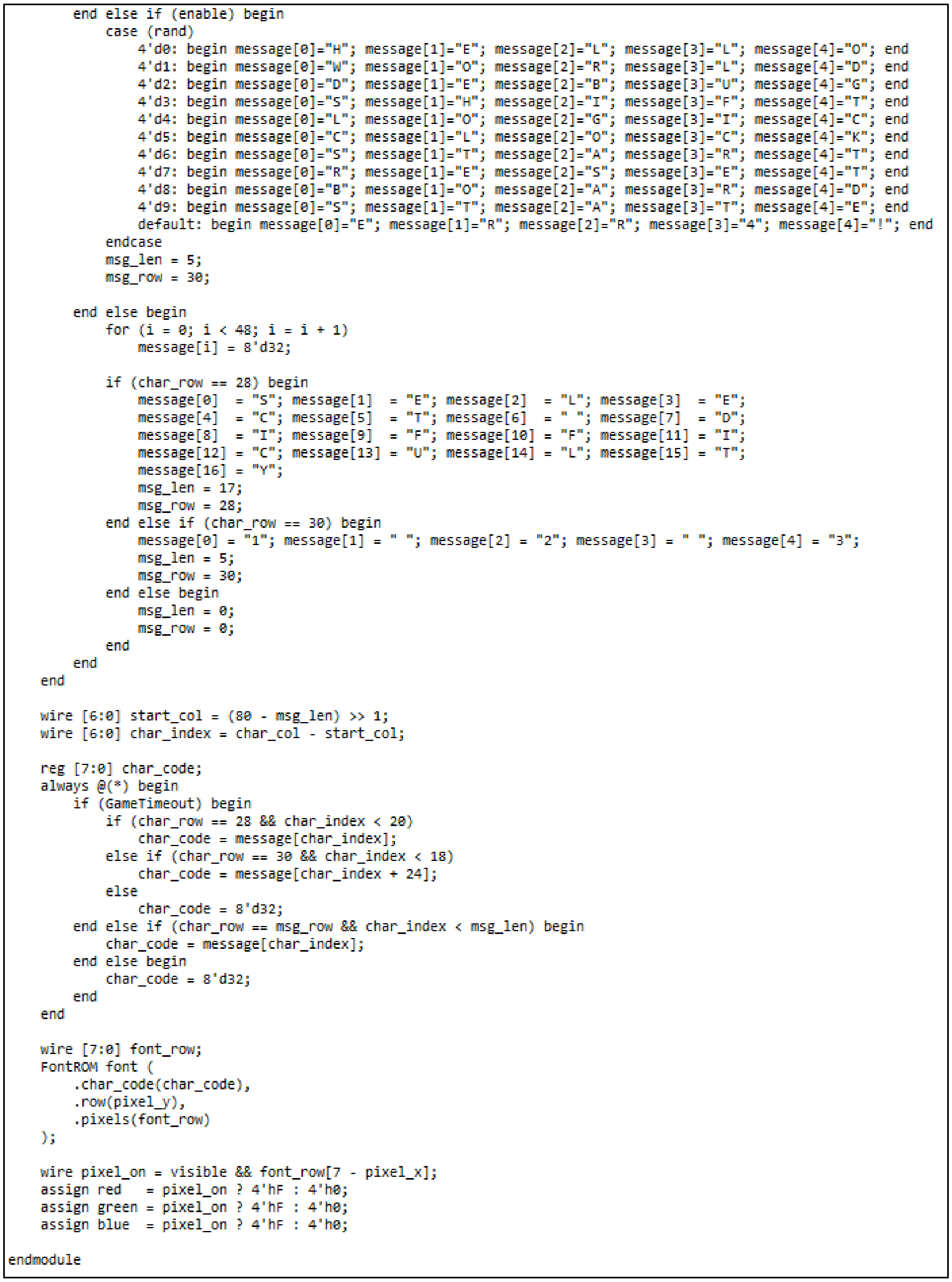
```verilog
//Divides 50 MHz clock to 25MHz

module ClockDivider25MHz (
    input wire clk_in,      // 50 MHz input
    input wire rst,         // Active-low reset
    output reg clk_out      // 25 MHz output
);

    always @(posedge clk_in or negedge rst) begin
        if (!rst)
            clk_out <= 0;
        else
            clk_out <= ~clk_out; // toggle every 20ns → 25 MHz
    end

endmodule
```

**Figure 23:** Verilog Code for ClockDivider.



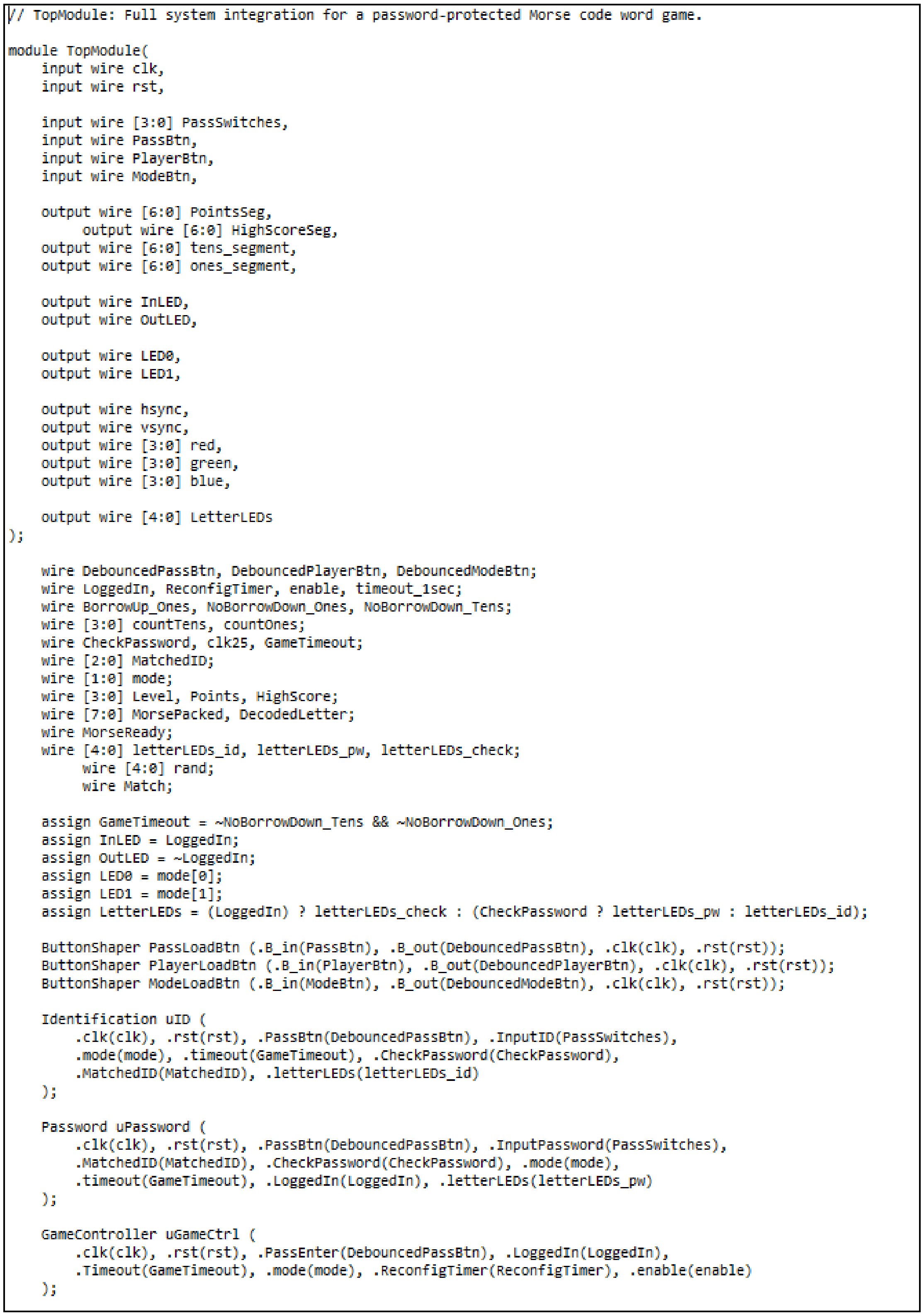
```
//VGATextRenderer: Displays text on VGA screen based on game state and selected level, with centered text.

module VGATextRenderer (
    input wire clk,
    input wire rst,
    input wire LoggedIn,
    input wire CheckPassword,
    input wire enable,
    input wire [4:0] rand,
    input wire GameTimeout,
    input wire [3:0] Points,
    output wire hsync,
    output wire vsync,
    output wire [3:0] red,
    output wire [3:0] green,
    output wire [3:0] blue
);

    parameter H_VISIBLE = 640;
    parameter H_TOTAL   = 800;
    parameter H_SYNC    = 96;
    parameter H_BP      = 48;
    parameter H_FP      = 16;

    parameter V_VISIBLE = 480;
    parameter V_TOTAL   = 525;
    parameter V_SYNC    = 2;
    parameter V_BP      = 33;
    parameter V_FP      = 10;

    reg [9:0] hcount = 0;
    reg [9:0] vcount = 0;

    wire visible = (hcount < H_VISIBLE) && (vcount < V_VISIBLE);
    assign hsync = ~(hcount >= (H_VISIBLE + H_FP) && hcount < (H_VISIBLE + H_FP + H_SYNC));
    assign vsync = ~(vcount >= (V_VISIBLE + V_FP) && vcount < (V_VISIBLE + V_FP + V_SYNC));

    always @(posedge clk or negedge rst) begin
        if (!rst) begin
            hcount <= 0;
            vcount <= 0;
        end else begin
            if (hcount == H_TOTAL - 1) begin
                hcount <= 0;
                if (vcount == V_TOTAL - 1)
                    vcount <= 0;
                else
                    vcount <= vcount + 1;
            end else begin
                hcount <= hcount + 1;
            end
        end
    end

    wire [6:0] char_col = hcount[9:3];
    wire [5:0] char_row = vcount[8:3];
    wire [2:0] pixel_x  = hcount[2:0];
    wire [2:0] pixel_y  = vcount[2:0];

    reg [7:0] message [0:47];
    reg [4:0] msg_len;
    reg [5:0] msg_row;
    integer i;

    always @(*) begin
        for (i = 0; i < 48; i = i + 1)
            message[i] = 8'd32;

        if (GameTimeout) begin
            message[0]  = "Y"; message[1]  = "O"; message[2]  = "U"; message[3]  = " ";
            message[4]  = "S"; message[5]  = "C"; message[6]  = "O"; message[7]  = "R";
            message[8]  = "E"; message[9]  = "D"; message[10] = " ";
            message[11] = Points + 8'd48;
```

**Figure 24:** Verilog Code for VGATextRenderer[1].



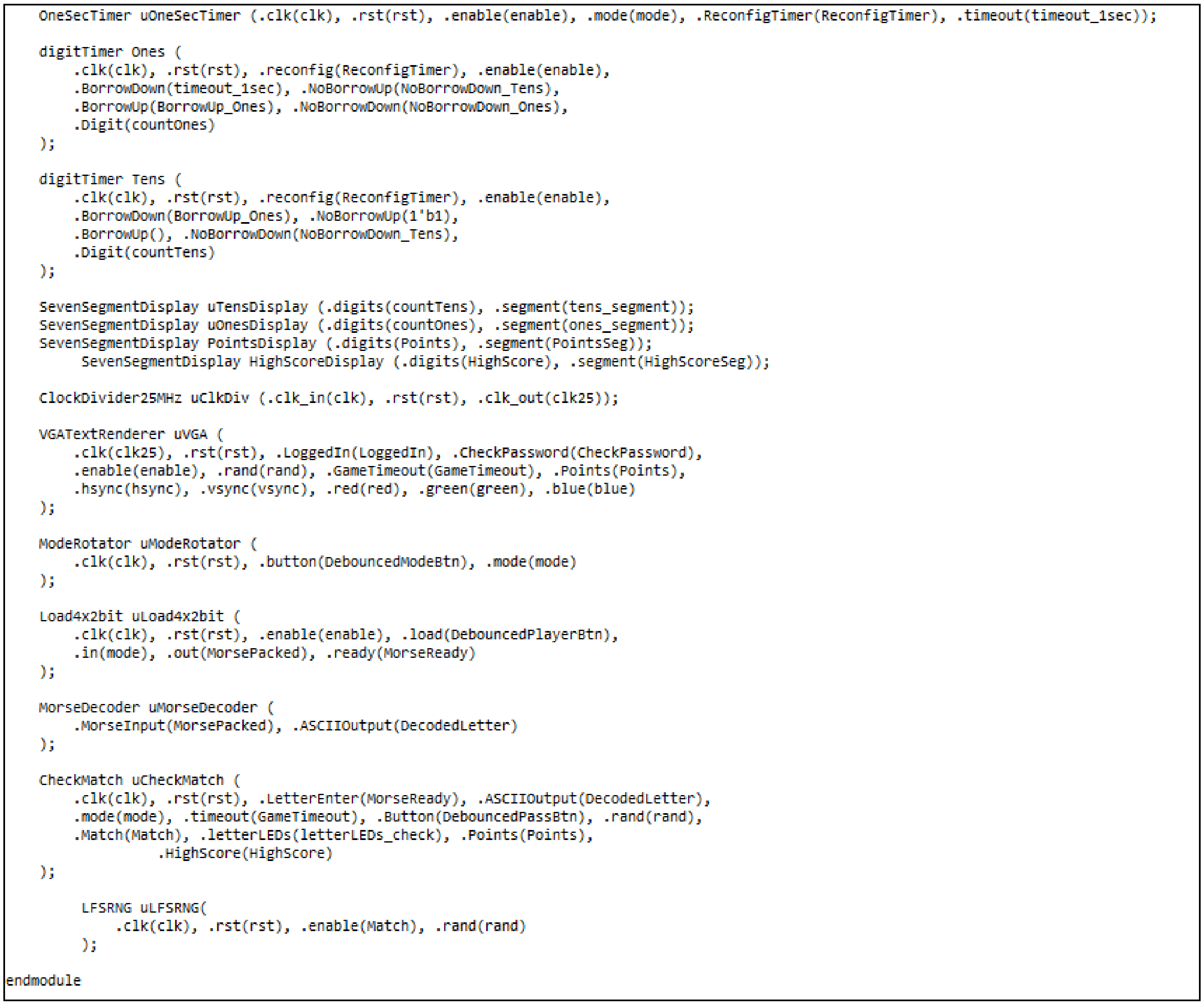
```
        end else if (enable) begin
            case (rand)
                4'd0: begin message[0]="H"; message[1]="E"; message[2]="L"; message[3]="L"; message[4]="O"; end
                4'd1: begin message[0]="W"; message[1]="O"; message[2]="R"; message[3]="L"; message[4]="D"; end
                4'd2: begin message[0]="D"; message[1]="E"; message[2]="B"; message[3]="U"; message[4]="G"; end
                4'd3: begin message[0]="S"; message[1]="H"; message[2]="I"; message[3]="F"; message[4]="T"; end
                4'd4: begin message[0]="L"; message[1]="O"; message[2]="G"; message[3]="I"; message[4]="C"; end
                4'd5: begin message[0]="C"; message[1]="L"; message[2]="O"; message[3]="C"; message[4]="K"; end
                4'd6: begin message[0]="S"; message[1]="T"; message[2]="A"; message[3]="R"; message[4]="T"; end
                4'd7: begin message[0]="R"; message[1]="E"; message[2]="S"; message[3]="E"; message[4]="T"; end
                4'd8: begin message[0]="B"; message[1]="O"; message[2]="A"; message[3]="R"; message[4]="D"; end
                4'd9: begin message[0]="S"; message[1]="T"; message[2]="A"; message[3]="T"; message[4]="E"; end
                default: begin message[0]="E"; message[1]="R"; message[2]="R"; message[3]="4"; message[4]="!"; end
            endcase
            msg_len = 5;
            msg_row = 30;

        end else begin
            for (i = 0; i < 48; i = i + 1)
                message[i] = 8'd32;

            if (char_row == 28) begin
                message[0]  = "S"; message[1]  = "E"; message[2]  = "L"; message[3]  = "E";
                message[4]  = "C"; message[5]  = "T"; message[6]  = " "; message[7]  = "D";
                message[8]  = "I"; message[9]  = "F"; message[10] = "F"; message[11] = "I";
                message[12] = "C"; message[13] = "U"; message[14] = "L"; message[15] = "T";
                message[16] = "Y";
                msg_len = 17;
                msg_row = 28;
            end else if (char_row == 30) begin
                message[0] = "1"; message[1] = " "; message[2] = "2"; message[3] = " "; message[4] = "3";
                msg_len = 5;
                msg_row = 30;
            end else begin
                msg_len = 0;
                msg_row = 0;
            end
        end
    end

    wire [6:0] start_col = (80 - msg_len) >> 1;
    wire [6:0] char_index = char_col - start_col;

    reg [7:0] char_code;
    always @(*) begin
        if (GameTimeout) begin
            if (char_row == 28 && char_index < 20)
                char_code = message[char_index];
            else if (char_row == 30 && char_index < 18)
                char_code = message[char_index + 24];
            else
                char_code = 8'd32;
        end else if (char_row == msg_row && char_index < msg_len) begin
            char_code = message[char_index];
        end else begin
            char_code = 8'd32;
        end
    end

    wire [7:0] font_row;
    FontROM font (
        .char_code(char_code),
        .row(pixel_y),
        .pixels(font_row)
    );

    wire pixel_on = visible && font_row[7 - pixel_x];
    assign red   = pixel_on ? 4'hF : 4'h0;
    assign green = pixel_on ? 4'hF : 4'h0;
    assign blue  = pixel_on ? 4'hF : 4'h0;

endmodule
```

**Figure 25:** Verilog Code for VGATextRenderer[2].



```verilog
// TopModule: Full system integration for a password-protected Morse code word game.

module TopModule(
    input wire clk,
    input wire rst,

    input wire [3:0] PassSwitches,
    input wire PassBtn,
    input wire PlayerBtn,
    input wire ModeBtn,

    output wire [6:0] PointsSeg,
         output wire [6:0] HighScoreSeg,
    output wire [6:0] tens_segment,
    output wire [6:0] ones_segment,

    output wire InLED,
    output wire OutLED,

    output wire LED0,
    output wire LED1,

    output wire hsync,
    output wire vsync,
    output wire [3:0] red,
    output wire [3:0] green,
    output wire [3:0] blue,

    output wire [4:0] LetterLEDs
);

    wire DebouncedPassBtn, DebouncedPlayerBtn, DebouncedModeBtn;
    wire LoggedIn, ReconfigTimer, enable, timeout_1sec;
    wire BorrowUp_Ones, NoBorrowDown_Ones, NoBorrowDown_Tens;
    wire [3:0] countTens, countOnes;
    wire CheckPassword, clk25, GameTimeout;
    wire [2:0] MatchedID;
    wire [1:0] mode;
    wire [3:0] Level, Points, HighScore;
    wire [7:0] MorsePacked, DecodedLetter;
    wire MorseReady;
    wire [4:0] letterLEDs_id, letterLEDs_pw, letterLEDs_check;
         wire [4:0] rand;
         wire Match;

    assign GameTimeout = ~NoBorrowDown_Tens && ~NoBorrowDown_Ones;
    assign InLED = LoggedIn;
    assign OutLED = ~LoggedIn;
    assign LED0 = mode[0];
    assign LED1 = mode[1];
    assign LetterLEDs = (LoggedIn) ? letterLEDs_check : (CheckPassword ? letterLEDs_pw : letterLEDs_id);

    ButtonShaper PassLoadBtn (.B_in(PassBtn), .B_out(DebouncedPassBtn), .clk(clk), .rst(rst));
    ButtonShaper PlayerLoadBtn (.B_in(PlayerBtn), .B_out(DebouncedPlayerBtn), .clk(clk), .rst(rst));
    ButtonShaper ModeLoadBtn (.B_in(ModeBtn), .B_out(DebouncedModeBtn), .clk(clk), .rst(rst));

    Identification uID (
        .clk(clk), .rst(rst), .PassBtn(DebouncedPassBtn), .InputID(PassSwitches),
        .mode(mode), .timeout(GameTimeout), .CheckPassword(CheckPassword),
        .MatchedID(MatchedID), .letterLEDs(letterLEDs_id)
    );

    Password uPassword (
        .clk(clk), .rst(rst), .PassBtn(DebouncedPassBtn), .InputPassword(PassSwitches),
        .MatchedID(MatchedID), .CheckPassword(CheckPassword), .mode(mode),
        .timeout(GameTimeout), .LoggedIn(LoggedIn), .letterLEDs(letterLEDs_pw)
    );

    GameController uGameCtrl (
        .clk(clk), .rst(rst), .PassEnter(DebouncedPassBtn), .LoggedIn(LoggedIn),
        .Timeout(GameTimeout), .mode(mode), .ReconfigTimer(ReconfigTimer), .enable(enable)
    );
```

**Figure 26:** Verilog Code for TopModule[1].



```
    OneSecTimer uOneSecTimer (.clk(clk), .rst(rst), .enable(enable), .mode(mode), .ReconfigTimer(ReconfigTimer), .timeout(timeout_1sec));

    digitTimer Ones (
        .clk(clk), .rst(rst), .reconfig(ReconfigTimer), .enable(enable),
        .BorrowDown(timeout_1sec), .NoBorrowUp(NoBorrowDown_Tens),
        .BorrowUp(BorrowUp_Ones), .NoBorrowDown(NoBorrowDown_Ones),
        .Digit(countOnes)
    );

    digitTimer Tens (
        .clk(clk), .rst(rst), .reconfig(ReconfigTimer), .enable(enable),
        .BorrowDown(BorrowUp_Ones), .NoBorrowUp(1'b1),
        .BorrowUp(), .NoBorrowDown(NoBorrowDown_Tens),
        .Digit(countTens)
    );

    SevenSegmentDisplay uTensDisplay (.digits(countTens), .segment(tens_segment));
    SevenSegmentDisplay uOnesDisplay (.digits(countOnes), .segment(ones_segment));
    SevenSegmentDisplay PointsDisplay (.digits(Points), .segment(PointsSeg));
         SevenSegmentDisplay HighScoreDisplay (.digits(HighScore), .segment(HighScoreSeg));

    ClockDivider25MHz uClkDiv (.clk_in(clk), .rst(rst), .clk_out(clk25));

    VGATextRenderer uVGA (
        .clk(clk25), .rst(rst), .LoggedIn(LoggedIn), .CheckPassword(CheckPassword),
        .enable(enable), .rand(rand), .GameTimeout(GameTimeout), .Points(Points),
        .hsync(hsync), .vsync(vsync), .red(red), .green(green), .blue(blue)
    );

    ModeRotator uModeRotator (
        .clk(clk), .rst(rst), .button(DebouncedModeBtn), .mode(mode)
    );

    Load4x2bit uLoad4x2bit (
        .clk(clk), .rst(rst), .enable(enable), .load(DebouncedPlayerBtn),
        .in(mode), .out(MorsePacked), .ready(MorseReady)
    );

    MorseDecoder uMorseDecoder (
        .MorseInput(MorsePacked), .ASCIIOutput(DecodedLetter)
    );

    CheckMatch uCheckMatch (
        .clk(clk), .rst(rst), .LetterEnter(MorseReady), .ASCIIOutput(DecodedLetter),
        .mode(mode), .timeout(GameTimeout), .Button(DebouncedPassBtn), .rand(rand),
        .Match(Match), .letterLEDs(letterLEDs_check), .Points(Points),
                  .HighScore(HighScore)
    );

         LFSRNG uLFSRNG(
             .clk(clk), .rst(rst), .enable(Match), .rand(rand)
         );

endmodule
```

**Figure 27:** Verilog Code for TopModule[2].