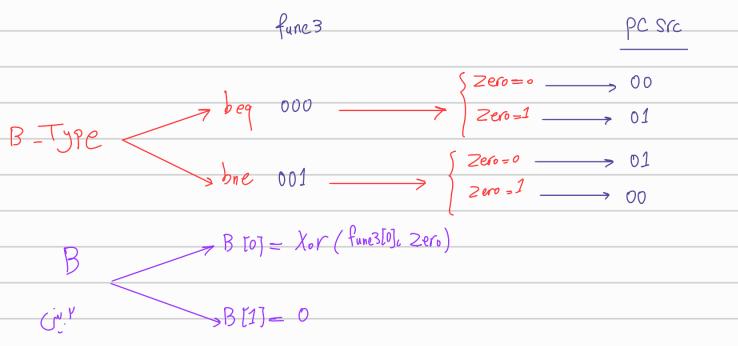


Type		OP(Reg Write	Inm Sic	ALV Src	Mem Write	Result Src	ALV	PC Src	
Type 000011 2 000 1 0 01 00 00	RType (add sub and or set)		0011			. 0	O	00	10	00	
Type 1100111 1 000 1 0 10 00 10	I Type (addi ori selli)	e 0010011		1	000	1	0	00	10	00	
STPE 0100011 0 001 1 1 29 00 00 BTgpe 1100011 0 010 0 0 99 01 B (beg chee) UType 0110111 1 100 9 0 11 29 00 JType 1101111 1 011 9 0 10 99 01 (Jah) Alv opc fr fv Alv Gatroll 00	I Type (lw)	0000011		1	000	1	0	01	00	00	
STIPE 0100011 0 001 1 1 92 00 00 BType 1100011 0 010 0 0 92 01 B (beg chae) UType 0110111 1 100 2 0 11 29 00 [Jul] Alv OPC fr fv Alv Gutril 00 X X 000 (+) 01 X X 001 (-) 10 000 \$\neq 0100000 \text{ out } 001 (-) 111 010 000 \$\neq 0100000 \text{ out } 010 (8)	I Type (Jalr)	1100111		1	000	1	0	10	00	10	
(beginne) UType 0110111 1 100 9 0 11 94 00 JType 1101111 1 011 9 0 10 92 01 (Jal) ALV OPC Pr Pv ALV Gentrall 00 X X 000 (+) 01 X X 001 (-) 10 000 \$\neq 01000 00 \\ 000 01000 00 \\ 010 (8)	STIPE	0100	0011	0	001	1	1	RH	00	00	
Type 1101111				0	010	0	0	ЯЯ	01	В	
(Jal) ALV OPC Pr Pv ALV Controll 00	, · · · · · · · · · · · · · · · · · · ·			1	100	R	0	11	RH	00	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$				1	011	9L	0	10	92	01	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	ALV OPC fr			fv		ALV C	entroll				
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	00		Χ χ			000) (+)				
000 0100600 001 (-1	01		X	χ χ		001	(-)				
111 010 (8)	10		D	00 ≠ 01000 ov			000	(+)			
010 (8)							001 (-1				
110								(8)			
010 010 (set)							011 101	(1) (slt)			



	32-bit Instruction Formats														
_	31	27	26	25	24	20	19	15	14	12	11	7	6	0	
R		funct7			rs	rs2		rs1		funct3		rd		opcode	
I		j		rs1		fun	ct3	rd		opcode					
S		imm[11:5]			rs2		rs1		funct3		imm[4:0]		opcode		
В	j	imm[12 10:5] rs2			rs1		fun	ct3	imm[4:1 11]		opcode				
U	imm[31:12]											rd	opo	code	
-	imm[20 10:1 11 19:12]										rd opcode			code	
J															

	Register	ABI Name
	x0	zero
Jal ra. 8	x1	ra
	x2	sp
Sw Soi84 (Zvo)	x3	gp
3. 15 (3.1)	×4 ×5-7	tp —
	x8	s0/fp
add So, Zero, Zero	x9	s1
So ← max	x10-11	a0-1
add Si, Zero, Zero	x12-17	a2-7 —
Ser _ index of mex	x18-27	s2-11
Ol Circumstance of the state of	x28-31	t3-t6
add Sr, Zoro, Zero Sr +i		
old Sti Zelo, Zelo	008000	∂ef
Loop: Seti ti, Si, 20	048028	a23
	000004	433
beg tic zero, End Luop	000004	4b3
LW St. O(St)	000009	933
slt tr. Sr. So	00000	a33
•	0144a 3	313
bne tr. Zeroc End14	020302	263
add S., Zero, Sp	000a29	983
add Sr. Zero. Si	0089a	3 b 3
	000396	563
EndIf: addi Se. Sr. +4	013004	133
add Sic Sic +1	009009	933
τ_{i} , τ_{i}	001484	193
Jol Zero, Loop	004a0a	a13
End Loop:	fddff0	96f
Jalr Zero, ra, O	000086	267
(LEO! ESTO		

