University of Tehran
College of Engineering
School of Electrical & Computer Engineering

Experiment 1
Sessions 1, 2

Clock and Periodic Signal Generation

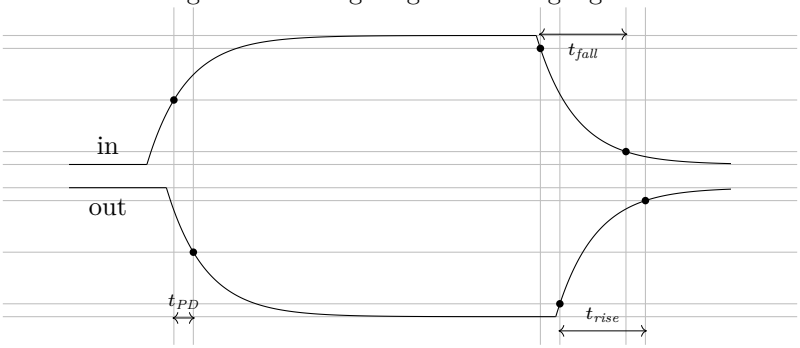
Digital Logic Laboratory
ECE 045, ECE 895
Laboratory Manual

Spring 1404

Contents

Prepared and developed by Katayoon Basharkhah under supervision of Professor Z. Navabi

Figure 1: Timing diagram of a logic gate



Introduction

The goal of this experiment is to introduce the concepts of static characteristics of digital logic gates, delay times, clock frequency generation and digital system using schematic diagram and *Verilog* HDL.

By the end of this experiment, you should have learned:

- Power supply, Function Generator, and Oscilloscope
- 74 Series Basic Logic Gates
- Different oscillator circuits (a LM555 timer IC, Schmitt trigger Oscillator)
- Sequential circuits using clocks and counters

1 Clock Generation using ICs and Analog components

In this part, you will understand different methods of clock generation in digital systems. You will use 74 Series discrete logic devices for implementing the circuits of this section.

1.1 Ring Oscillator

In a physical device, no gate can switch instantaneously; in a device fabricated with MOSFETs, for example, the gate capacitance must be charged before current can flow between the source and the drain. Thus, the output of every gate changes a finite amount of time after the input has changed. Therefore, one of the most important parameters in digital logic gates is the propagation delay, that is defined as the time from the 50% point of input to the 50% point of output. There are also two more parameters named t_{fall} and t_{rise} that are measured as the time between 10% and 90% point of the signal and vice versa.

The delay of logic gates is very small and this imposes a large bandwidth. So, measuring this delay directly using a relatively low-cost oscilloscope may be difficult. An alternative method for measuring this parameter is using a *ring oscillator* as shown in figure 2. A ring oscillator is composed of a chain of odd number of inverters, in which the output of the last inverter is connected to the

Figure 2: Ring oscillator

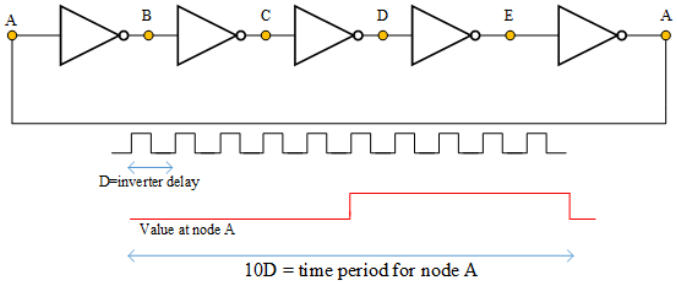
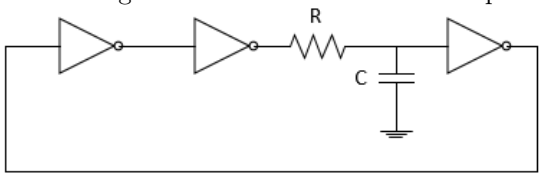


Figure 3: Ring oscillator with resistor and capacitor



input of the first one. It can be easily seen that adding more inverters to the chain increases the total gate delay. The time at which a value feeds back to the same node is the time period of the ring oscillator which equals $2N * Delay_{inv}$, where N is the odd number and $Delay_{inv}$ is the delay of each inverter gate. The delay of each single inverter can be determined by measuring the total delay.

Construct the circuit shown in figure 2 with as little wire as possible. 74HCT04 is the inverter gate of 74 series devices that include six inverters. You should wire up five inverters to a chain.

1. Measure the propagation delay of the chain by measuring the period time of the output.
2. Calculate the delay of a single inverter and report this time.
3. Change the circuit to figure 3 and use the resistor with 1 kΩ or 100 Ω depending on your IC, and a capacitor with 470 pF, then measure the frequency.

1.2 LM555 timer

LM555 is among the devices can be used for generating clock signal or time delays. The pin layout of this IC can be seen in figure 4.

This IC operates in three modes: Monostable, Bistable and Astable. The astable mode that we use in this experiment allows the timer to operate as an oscillator that outputs a continuous rectangular pulse of a required frequency. For astable operation, we need two resistors and one capacitor to design a circuit that operates at the frequency required. The timing during which the output is either high or low is determined by these externally connected resistors and capacitors. Note that the durations of the low and high states may be different. Figure 5 illustrates an LM555 configuration for astable mode operation.

Figure 4: LM555 timer pin-out

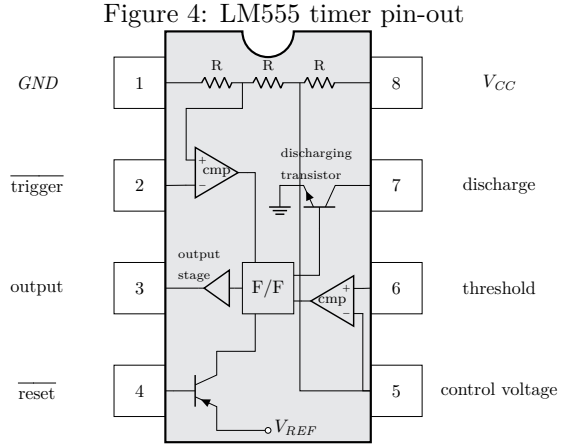


Figure 5: LM555 in astable mode

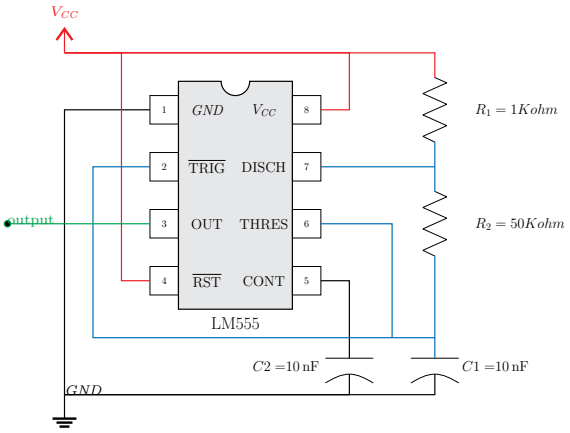
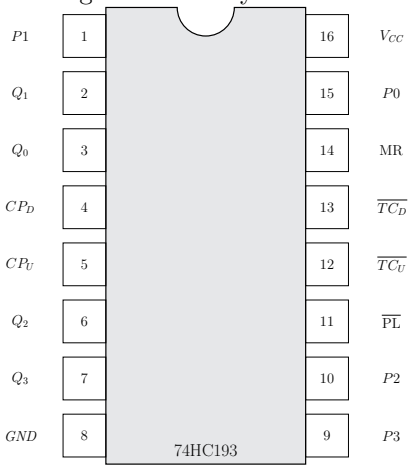


Figure 6: Pin layout of 74193



The external capacitor $C1$ charges through $R_1 + R_2$ and discharges through R_2. Thus, the duty cycle and frequency may be precisely set by selecting the right combination of resistances and capacitance. According to figure 4 and figure 5, the charge time (output high) is given by $T_1 = 0.693 * (R_1 + R_2) * C$ and the discharge time (output low) by $T_2 = 0.693 * R_2 * C$. Thus, the total time period of the square wave is $T = T_1 + T_2 = 0.693 * (R_1 + 2R_2) * C$. Consequently, the frequency of oscillation is $\frac{1}{T}$. The duty cycle also can be computed by $\frac{R_1+R_2}{R_1+2R_2}$.

These equations describe how we can choose these three values to decide on the frequency and the high and low duration of our signal. With the LM555 timer, the default value of R_1 in this configuration is 1 kΩ and this means that we cannot get a perfect 50% duty cycle. (If we make $R_2 \gg R_1$ then we can get close.)

Do the following work. Your report must include the procedure you followed, as well as any observations and results.

1. Implement the LM555 in astable mode using the wiring diagram from figure 5 and observe the output. Report the clock frequency and the duty cycle and include the waveform of the output in your report.

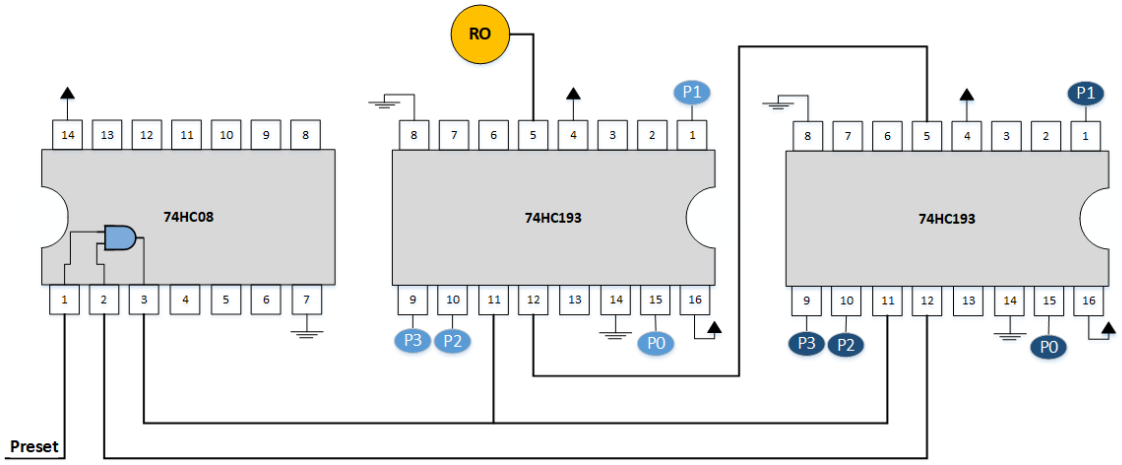
2. Change the value of R_2 resistors to produce different clock frequencies. To do so, R_2 should be 1 kΩ, 10 kΩ and 100 kΩ. Calculate the frequency and duty cycle using above equations and compare them to the clock signal you see on the output.

1.3 Synchronous Counter as a Frequency Divider

Different clock signals can be produced by the aforementioned methods, but not all of them are suitable for all applications. Consider a 1 Hz clock signal which can be easily produced by an LM555 timer. The timing error of this signal can be 1-2%, which is too much for a low frequency like this, while this error range is acceptable for higher frequencies. So, a higher frequency can be chosen and then a frequency divider can reduce the frequency to the desired one.

Counters can be used as a frequency divider. 74HC193 is a synchronous 4-bit up/down counter. As figure 6 shows, it has 4 inputs $P3$-$P0$(most to least), 4 outputs $Q3$-$Q0$ (most to least), and a

Figure 7: Frequency divider using 74193



parallel load, which allows for presetting an initial value for the counter. With this pin layout, two counters can be cascaded when the modulus is more than 4 bits.

When up counting is desired the initial value is obtained by:

$$\textit{Initial value} = \textit{Maximum value} - \textit{Modulus}$$

Construct a divide by 200 synchronous up-counter as shown in figure 7. You should:

1. Use the ring oscillator of part 1 to generate a clock signal. This will be the clock input of the LSB counter.
2. A Presetting mechanism is necessary for the initial loading of the counters of figure 7. The mechanism as you have learned in the logic design course can include an AND gate for anding a preset input signal with the load inputs of the counter. Perform this presetting by using 7408 AND gate as shown in figure 7.
3. Record the results of carry out of the MSB counter and measure its frequency, compare the results with the frequency of the input clock.

1.4 T Flip-Flop

You should use a T flip-Flop after the counter to produce a 50 percent duty cycle signal. For this purpose use a D Flip-Flop, 74HC74 IC, and convert it to a T Flip-Flop as the pin layout shown in figure 8.

Acknowledgment

This lab manual was prepared and developed by Katayoon Basharkhah, Ph.D. student of Digital Systems at the University of Tehran, under the supervision of Professor Zain Navabi.

This manual has been revised and edited by Zahra Jahanpeima, PHD student of Digital Systems at University of Tehran.

Figure 8: D Flip-Flop connection