

Digital Electronics and Computer Organization Lab (ENCS 221)

Experiment No. 5

-Sequential Logic Circuits

Student’s Name: Mohammad Salem

Student’s No: 1200651

Partners: Nafe Abubaker

Instructor’s Name: Dr. Khader Mohammad

Teaching Assistant’s Name: Haleema Hmedan

Sections: 3

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# Abstract

In this report, I will introduce the various types of sequential logic circuits that are commonly used in building digital systems. These include the flip-flop, register, counters, and latches. Sequential logic circuits are essentially combinational circuit with feedback.

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# Theory

## Sequential circuits in General:

Any digital circuit classified as either a combinational or a sequential circuit. As known before, combinational logic circuits implement Boolean functions, which mappings of inputs to outputs, and the output of these circuits are functions of input only. The Sequential circuits as shown in figure 1 are combinational circuit which connected to storage elements to form a feedback path.

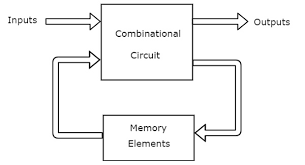
The outputs of the sequential circuit are a function not only of the inputs, but also of the present state of the memory elements. The next state of the storage elements is also a function of external inputs and the present state. Thus, a sequential circuit is specified by a time sequence of inputs, outputs, and internal states. Also, has memory so output can vary based on input. This type of circuits uses previous input, output, clock and a memory element.

Figure - sequential circuit

## Latches:

Latches are basic storage elements that operate with signal levels, latches are level-sensitive devices useful for the design of the asynchronous sequential circuit.

There are many types of Latches, such as RS-Latch, D-Latch as shown below.

1) SR-Latch

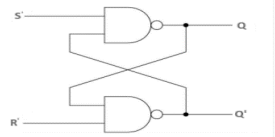
The SR latch is a circuit with two cross-coupled NAND gates, and two inputs, S for set and R for reset, as shown the figure 2. SR-latch has two useful states, when output Q = 1 and Q’ = 0, the latch is said to be in the set state, and when Q = 0 and Q’ = 1, it is in the reset state as shown in the table below.

Figure - SR-Latch

Table - SR-Latch

|  |  |  |
| --- | --- | --- |
| Q | Q’ | State |
| 1 | 0 | set |
| 0 | 1 | reset |

2) D-Latch

D-latch is similar to the SR latch with some modifications made; the inputs are the complements of each other. The design of D-latch with Enable signal, and the truth table are shown below in figure 3.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Enable | D | Q(t) | Q(t+1) | state |
| 1 | 0 | X | 0 | reset |
| 1 | 1 | X | 1 | set |
| 0 | x | X | Q(t) | no change  Figure - D-Latch |

Table - D-Latch

## Flip Flops:

Flip-flops are like latches, they also used for storing binary information, but the difference in flip flops is the output. The output changes in the flip-flop occurs only at the clock edge while in the latch it occurs at the clock level.

There are many types of Flip flops, such as D flip-flop, JK flip-flop, and T flip-flop.

1) D Flip Flop

D flip-flop has just one input in addition to the clock input. This input is called the DATA input. When the clock is triggered (become 1), the Q output matches to the DATA input, and if the DATA input is HIGH (=1), the Q output goes HIGH, and if the DATA input is LOW, the Q output goes LOW.

|  |  |  |  |
| --- | --- | --- | --- |
| CLK | D | Q | Q’  Figure - D Flip Flop |
| 0 | 0 | Q | Q’ |
| 0 | 1 | Q | Q’ |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Table - D Flip Flop

2) JK Flip Flop

The JK Flip Flop is the most widely used flip flop. It is considered to be a universal flip-flop circuit. The sequential operation of the JK Flip Flop is the same as for the RS flip-flop with the same SET and RESET input.

The J and K inputs of the JK flip-flop are respectively connected to the SET and RESET inputs of the SR flip-flop. The difference between the two is that while the J and K inputs of the SR flip-flop are set to 1, the J and K inputs of the JK flip-flop are not. When the two inputs of the SR flip-flop are set to 1, the circuit produces invalid states, but in the case of the JK flip-flop, the invalid states are not.

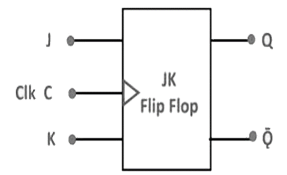


Table - JK Flip Flop

Figure - JK Flip Flop circuit

3) T Flip Flop

The T (Toggle) flip-flop is simply a JK flip-flop whose output alternates between HIGH and LOW with each clock pulse. Toggles are widely used in logic circuits because they can be combined to form counting circuits that count the number of clock pulses received. [1]

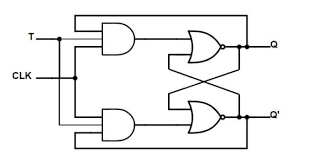


Figure - T Flip Flop

|  |  |  |
| --- | --- | --- |
| T | Q | Q’ |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

Table - T Flip Flop

## Registers:

Registers are groups of flip‐flops, each one shares a common clock and is capable of storing one bit of information. An n‐bit register consists of n flip‐flops capable of storing n bits of binary information. In addition to the flip‐flops, a register may have combinational gates that perform certain data‐processing tasks. As a general Definition, registers consist of a group of flip‐flops together with gates that affect their operation. The flip‐flops hold the binary information, and the gates determine how the information is transferred into the register.

1) Shift Registers

Shift registers basically consist of several single bit D flip-flop, one for each data bit, connected together in a serial type chain arrangement, so that the output from one D flip-flop becomes the input of the next flip-flop and so on.

As an example of shift registers, the following figure 7 represents 4-bit shift registers.

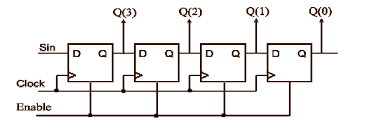


Figure - 4 bit shift register

2) 4-Bit Shift Register with serial-in and parallel-out load

In Serial-in Parallel-out shift registers, the data is stored into the register serially while it is retrieved from it in parallel-fashion.

Here in figure 8, the data which stored (Data in) is fed serially at the input of the first flip flop. It is also seen that the inputs of all other flip-flops (except the first flip-flop) are driven by the previous flip-flops outputs. In this kind of shift register, the data stored in the register is considered as a parallel-output data (Data out) at the outputs of the flip-flops (Q1 to Q4).

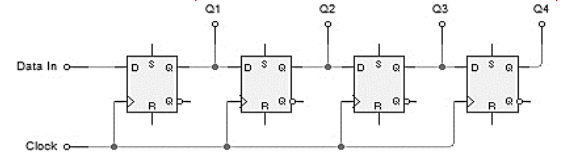


Figure - 4 bit shift register with serial-in and parallel-out load

## Counters:

Counters are special-purpose register; it is a register that goes through a prescribed sequence of states. Counters are classified into two categories: Ripple and Synchronous counters.

1) Synchronous Counters

Synchronous counters are different from ripple counters in that clock pulses are applied to the inputs of all flip‐flops.

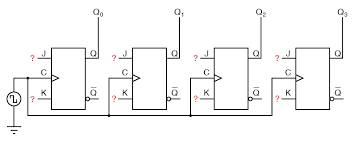


Figure - Synchronous Counters

2) Ripple Counters

In a ripple counter, a flip‐flop output transition serves as a source for triggering other flip‐flops. In other words, the CLK inputs of flip‐flops are triggered not by the common clock pulses, but by the transition that occurs in other flip‐flop outputs. A 3- bit Ripple Counter is shown in the figure 10 below.

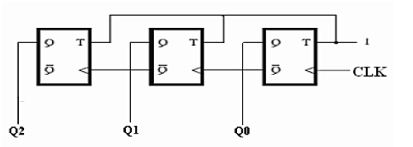


Figure - Ripple Counter

# Procedure & Discussion

## 1. Constructing RS Latch with Basic Logic Gates

We used IT-3008 module to construct the RS Latch circuit. First, we connected the inputs to Pulser Switches SWA and SWB and outputs to logic Indicactors and we got the following results:

|  |  |  |  |
| --- | --- | --- | --- |
| A3 | A4 | F6 | F7 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 |

Table - Truth Table for RS Latch

As known before, if A3 equals to 1 (set case), the output F6 will be 1, but in the table 6, it is the opposite; it was noticed that the inputs are in active low state and the outputs are in the active high state. For example, if A3 equals to zero, then it is activated and the output F6 is equals to one, so it is activated, and so on.

If both inputs were set to 1, the output will not change and will remain the same as before.

## 2. Constructing RS Latch with control input

We used IT-3008 module to construct the RS Latch with control input. First, we connected the inputs to Pulser Switches SWA and SWB and the output to logic Indicators then we got the following results as shown as in the table 7.

|  |  |  |  |
| --- | --- | --- | --- |
| A1 | A5 | F6 | F7 |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 |

Table - Truth Table for RS Latch with control input

When A1 = 0 and A5 = 1, then output Q will equal 0 and Q' will equal 1. If we change A5 to zero, the outputs won't change, and we noticed that the case when both inputs = 1 is an invalid case since both Q and its complement = 1.

## 3. Constructing D latch with RS latch

We connected A1 to SW1 and CK2 to SWA and F6 to L1 and we got the following results:

|  |  |  |
| --- | --- | --- |
| CK2 | A1 | F6 |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| ⎍ | 0 | 0 |
| ⎍ | 1 | 1 |

Table - Truth Table for D Latch

When we set the clock to zero, there will be no output regardless of what the input is, but after changing the clock to 1 and setting the input to 0, the output will equal zero, and after setting the input to 1, the output will equal one, in either case, if we changed the clock back to zero, the output will keep the result it previously had.

## 4. Constructing JK latch with RS latch

After connecting CK2 to SWB, A1 to SW0, A5 to SW1 and the output to the logic Indicators then we got:

|  |  |  |  |
| --- | --- | --- | --- |
| CK | A1 (J) | A5 (K) | F6 (Output) |
| ⎍ | 0 | 0 | 0 |
| ⎍ | 0 | 1 | 0 |
| ⎍ | 1 | 0 | 1 |
| ⎍ | 1 | 1 | 1 |

Table - Truth Table for JK latch

If both inputs (A1 & A5) are set to logic 0 (J = K = 0), regardless of the clock state, the flip-flop will keep any data it has (as a memory), but when both inputs are set to 1 (J = K = 1), the flip-flop will switch and turn to its complement state. For example, if J = 1 and K = 0, the output state will be set to 0, so when changing the K value to 1 the output will be the complement of the previous input.

## 5. Constructing JK Flip Flop with master – slave RS latch

We used IT-3008 module to construct the JK flip flop circuit. First, we connect CK2 to Pulser switch and CK1 to SWA, K to SW0, J to SW1 and the outputs to the logic Indicators.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| CK | K | J | F1 | F2 | F6 | F7 |
| ⎍ | 0 | 0 | 1 | 0 | 1 | 0 |
| ⎍ | 0 | 1 | 1 | 0 | 1 | 0 |
| ⎍ | 1 | 0 | 0 | 1 | 0 | 1 |
| ⎍ | 1 | 1 | 1 | 0 | 1 | 0 |
| ⎍ | 1 | 1 | 0 | 1 | 0 | 1 |

Table - Truth table for JK flip flop

As written in table (4.5) above, it is obvious that when J=0 and K=0, there is no change in the state of the circuit, but when J=0, k=1, F6 will reset to zero, also, when J=1, K=0, F6 will set to one, and when J=1, K=1, the outputs F1, F2, F6, F7 will toggle (keep turning between 0 and 1 every clock cycle).

## 6. Constructing Shift Register with D Flip Flops

Three D flip-flops were connected, and connect a clock in each CLK input of all flip flops. The input A is connected to a Logic State into the input D of the first flip-flop. The input B is connected to a Logic State into all the flip-flops’ reset inputs.

1) At A=1, send in a CK signal from SWA the output is1000

2) At A=0, send in a CK signal from SWA the output is 0100

3) At A=0, send in a CK signal from SWA the output is 0010

4) At A=1, send in a CK signal from SWA the output is 1001

## 7. 4-Bit Shift Register with serial and parallel load

When we connected CK to the clock generator TTL level out at 1 Hz and change data at B1 with DIP2 the results we got are:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A1 | C1 | L3 | L2 | L1 | L0 |
| 0 | ⎍ | 0 | 0 | 0 | 1 |
| 0 | ⎍ | 0 | 0 | 1 | 1 |
| 0 | ⎍ | 0 | 1 | 1 | 1 |
| 1 | ⎍ | 0 | 1 | 1 | 1 |

Table - Truth Table for shift register

When we connected LOAD to the clock generator TTL level at 1 Hz and set A1 to 1 the results we got are:

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| D1 | D | C | B | A | L3 | L2 | L1 | L0 |
| ⎍ | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| ⎍ | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| ⎍ | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| ⎍ | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| ⎍ | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |

When the mode input (A1) =0, the circuit works as a parallel register, and when A1=1, the circuit works as a serial register.

When A1=1 the shift stops.

## 8. 2-bit Synchronous Counter

|  |  |  |
| --- | --- | --- |
| CLK | Q1 | Q0 |
| ⎍ | 0 | 0 |
| ⎍ | 0 | 1 |
| ⎍ | 1 | 0 |
| ⎍ | 1 | 1 |
| ⎍ | 0 | 0 |
| ⎍ | 0 | 1 |
| ⎍ | 1 | 0 |
| ⎍ | 1 | 1 |

Table - Truth Table for Synchronous Counter

After the fifth clock edge, Q0 will change to 0 and Q1 will change to 0 too, now they are back to the reset state.

## 9. 3-bit Ripple Counter

Divide by 8 counter is 3-bit counter that count from 0 to 7.

|  |  |  |  |
| --- | --- | --- | --- |
| CLK | Q2 | Q1 | Q0 |
| ⎍ | 0 | 0 | 0 |
| ⎍ | 0 | 0 | 1 |
| ⎍ | 0 | 1 | 0 |
| ⎍ | 0 | 1 | 1 |
| ⎍ | 1 | 0 | 0 |
| ⎍ | 1 | 0 | 1 |
| ⎍ | 1 | 1 | 0 |
| ⎍ | 1 | 1 | 1 |

Table - Truth Table for 3 bit Ripple Counter

## 10. BCD Counter

We used IC 7490 on IT-3008 module to construct the BCD counter by connecting C3, C4 to SW0 and D1, D2 to SW2 and F1~F4 to L1~L4 to SWA.

When the input =0, the counter will count upward from 0 to 9 and back to zero and so on. But when the input =1, it will reset the counter to 9 because it was indicated in R9 to be reset to 9.

## Discussion

**Although latches are useful for storing binary information, they are rarely used in sequential circuit design, why?**

Certainly, latches are faster than flip-flops because they contain several latches, but they create glitches that are not appreciated when designing, and also latches are level-triggered as previously mentioned while flip-flops are edge-triggered, so the change in the flip-flop occurs only at its triggering edge.

**What is the disadvantage of the RS flip flops?**

When both inputs are 1 (S=R=1), the output and its complement will also be 1, which is not allowed.

**What is the difference between “synchronous” and “ripple” counters?**

In ripple-counters, each flip-flop is triggered by its own clock, whereas in synchronous counters, all flip-flops are triggered with the same clock, so synchronous counters should be faster.

# Conclusion

In this experiment, I first describe the theoretical foundations I gained from this experiment about sequential circuits and their applications. I also designed a lot of sequential circuits, such as latches, flip-flops, registers, and counters. As a result, I determined the outputs of each circuit and wrote them down in truth tables. As a result of this experiment, I developed skills in understanding the sequential circuits and how to implement them in logic diagrams. I also gained a greater understanding of how the circuits work.

# References

<https://www.tutorialspoint.com/digital_circuits/digital_circuits_sequential_circuits.htm>

Accessed on 29-04-2022 at 5:00 PM

<https://www.bt-webworld.com/t-flip-flop-circuit-diagrams>

Accessed on 29-04-2022 at 5:30 PM

<https://www.javatpoint.com/>[2]

Accessed on 29-04-2022 at 3:22 PM