

Digital Electronics and Computer Organization Lab (ENCS 221)

Experiment No. 7

-Constructing Memory Circuits Using Flip-Flops

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Date: 10 JAN 2022

# Abstract

This experiment begins by introducing the theoretical foundations of the most essential element of a computing system, which is memory, by talking about random access memories (RAMs) in general, and different types of RAM structures.

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# Theory

## 1) Memory in general

A memory circuit stores the voltage signal representation on an input signal whenever it is triggered by a control signal, and it holds that voltage until it is triggered again. During assertion of the control signal, the input signal is ignored, and the output voltage is driven to the most recently stored voltage. Because a memory circuit stores the input signal level at each assertion of the control input, the output will change immediately (if the input value is opposite what is stored), or it will remain constant. Memory occurs between control signal assertions, because the output remains constant at the last stored value, regardless of input signal changes. The figure below shows the basic Diagram of the memory.

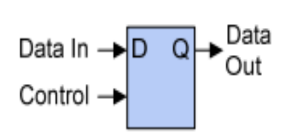


Figure - basic memory device [1]

Memory circuits, as shown in the above diagram, require at least two inputs: a data signal to be memorized, and a timing control signal that indicates when the data signal should be memorized.

Computer’s memory has two basic types: Primary memory (RAM and ROM), and Secondary memory (hard drive, CD, etc.). Random Access Memory (RAM) is primary-volatile memory, and Read Only Memory (ROM) is primary-non-volatile memory.[2]

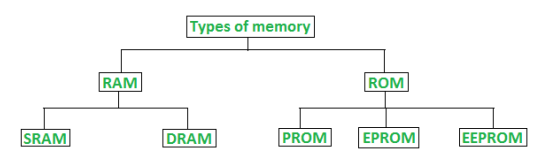


Figure - : Classifications of Computer’s Memory. [3]

## 2) Random Access Memory (RAM)

In general, Random Access Memory can be defined by the following four points.

* It is called also the read write memory or the main memory or the primary memory.
* This is the storage for data the CPU needs to execute a program.
* It is a volatile memory: data disappears when the power is turned off.
* SRAM (Static Random Access Memory) and DRAM (Dynamic Random Access Memory) are two types of RAM.

Here are five types of basic RAM structures:

### 1) 1-bit RAM

In the figure below, the input and output are not separated. Two control terminals are available: the R/W terminal (R for READ, W for WRITE) and the ENABLE terminal (CS for ENABLE). Also included are a D flip-flop and two tri-state buffers.

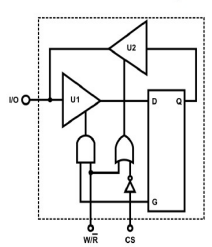


Figure - 1bit memory

The tri-state buffers U1 and U2 do not operate when CS=0, so data input is not possible. The Dflip-flop's output Q is not sent to the I/O port when CS=0.

When CS=1, W/R controls the D flip-flop in negative state. It means that when W/R' =1 (the write case), U2 opens but U1 does not, so the I/O will accept data input through U1. If W/R'=0 (the read case), so U1 opens and U2 does not, so the output Q of the D flip-flop will return to the I/O input.

### 2) 4-bit RAM

RAM can also be connected to this connector to increase its capacity. According to figure below, a decoder was used to determine the address of the cells. RAM1 I/O1 and I/O2 are selected if the selection line of the decoder A = 0, and RAM1 I/O1 and I/O2 are selected if A = 1, then RAM1 I/O1 and I/O2 are selected.

Address line A is used to select between RAM1 and RAM2. Since there is only one address line, that can select from the 2 RAMs, and in each CS, it can only select a 2-bit RAM so the total capacity is 2×2 = 4 RAMs and each RAM store 1 bit as the previous figure.

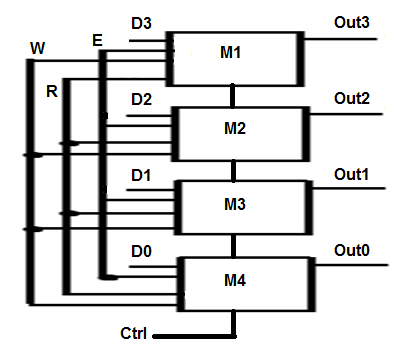


Figure - 4 bit RAM logic diagram [4]

### 3) 2-bit RAM

In the figure below, the 2-bit RAM circuit has independent input and output. At Address=0, input D1 is enabled and the content of D1 is shown at the output, and at Address=1, input D2 is enabled and the content of D2 is shown at the output. The ENABLE terminal must be triggered whenever inputs change.

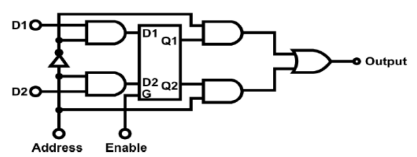


Figure - 2 bit RAM

### 4) 64-bit RAM

Locations are determined by the number of address lines in 64-bit RAM. A memory cell consists of 24=16 locations (address lines). The RAM's total capacity is 64 bits, so a 4-bit data can be stored at each location.

According to the figure below, the input and output terminals are separated, and the four addresses inputs (A0, A1, A2, A3) select one of the 16 words (cells) in the memory. There are two control inputs on the read/write control logic (ME', WE'), and both are in the low state. The input process begins when ME' = 0.

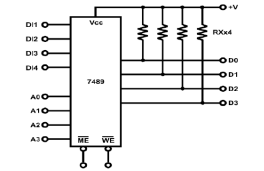


Figure - 64bit RAM

# Procedure & Discussion

## 1) Constructing 2-bit RAM circuit using D Flip-Flops:

A 2-bit RAM was constructed with two D flip-flops, AND gates, and NAND gates and each D flip-flop was connected to a clock, and an AND gate that contained the inputs and selection line of the circuit.

Table - first truth table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Input | | | | Output | | |
| CLK | S1 | D2 | D1 | F3 | F2 | F1 |
| ⎍ | 0 | 0 | 0 | 1 | 0 | 1 |
| ⎍ | 0 | 0 | 1 | 1 | 0 | 1 |
| ⎍ | 0 | 1 | 0 | 1 | 0 | 1 |
| ⎍ | 0 | 1 | 1 | 1 | 0 | 1 |
| ⎍ | 1 | 0 | 0 | 1 | 1 | 0 |
| ⎍ | 1 | 0 | 1 | 1 | 1 | 0 |
| ⎍ | 1 | 1 | 0 | 1 | 1 | 0 |
| ⎍ | 1 | 1 | 1 | 1 | 1 | 0 |
| ⎍ | 0 | 0 | 0 | 0 | 0 | 0 |
| ⎍ | 0 | 0 | 1 | 1 | 0 | 1 |
| ⎍ | 0 | 1 | 0 | 0 | 0 | 0 |
| ⎍ | 0 | 1 | 1 | 1 | 0 | 1 |
| ⎍ | 1 | 0 | 0 | 0 | 0 | 0 |
| ⎍ | 1 | 0 | 1 | 1 | 0 | 0 |
| ⎍ | 1 | 1 | 0 | 0 | 1 | 0 |
| ⎍ | 1 | 1 | 1 | 1 | 1 | 0 |

According to the table above, each time the clock triggers from zero to one, and the selection line (the address) is zero, the outputs F3, F1 follow the input D1, because D1 is enabled (D1). As long as (the address) S1=1, the outputs F2, F3 follow the input D2, because it is also a write operation, but it is on D2 (D2 is enabled).

## 2) Constructing 64-Bit RAM Circuit:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | 1 | 0 | 0 |  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 |  | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |  | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 |  | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table - second truth table

The address of any memory location (cell) must be applied at the address input terminals (A0, A3), and the input WE' (S2) must be set to zero, so the input data will be written into the chosen address (given to the memory).

For reading from any memory location, the address of the memory location was also required regardless of the input data values, and the input WE' setting must be set to one.

# Conclusion

In this experiment, I described the theoretical foundations that I acquired regarding Random Access Memory (RAM) and its types. I then designed some of the RAM circuits experimentally, then compiled the truth tables using the outputs of each circuit.

Through this experiment I learned how to implement the circuits in logic diagrams, and I also gained a better understanding of how circuits exactly work.

# References

<https://learn.digilentinc.com> [1]

<https://www.geeksforgeeks.org> [2]

<https://www.researchgate.net/figure/Fig-8-The-above-fig-shows-the-4-bit-R-W-Memory-circuit-comprising-of-four-1-bit-R-W_fig2_314898315> [3]