

**ENCS3330, DIGITAL INTEGRATED CIRCUITS.**

**Assignment #1**

**Student: Mohammad Salem – 1200651.**

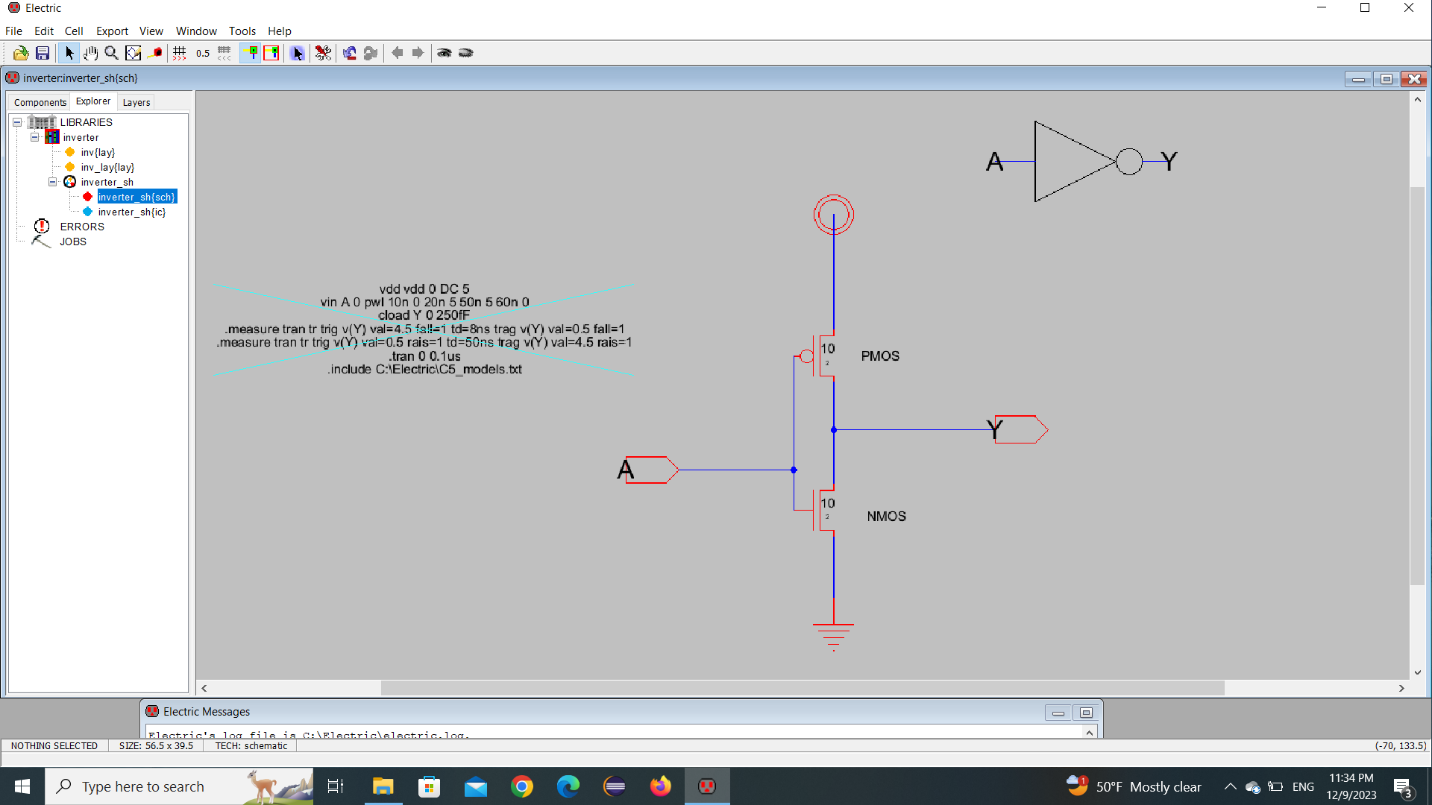
**Section 2.**

**Dr: Khader Mohammad**

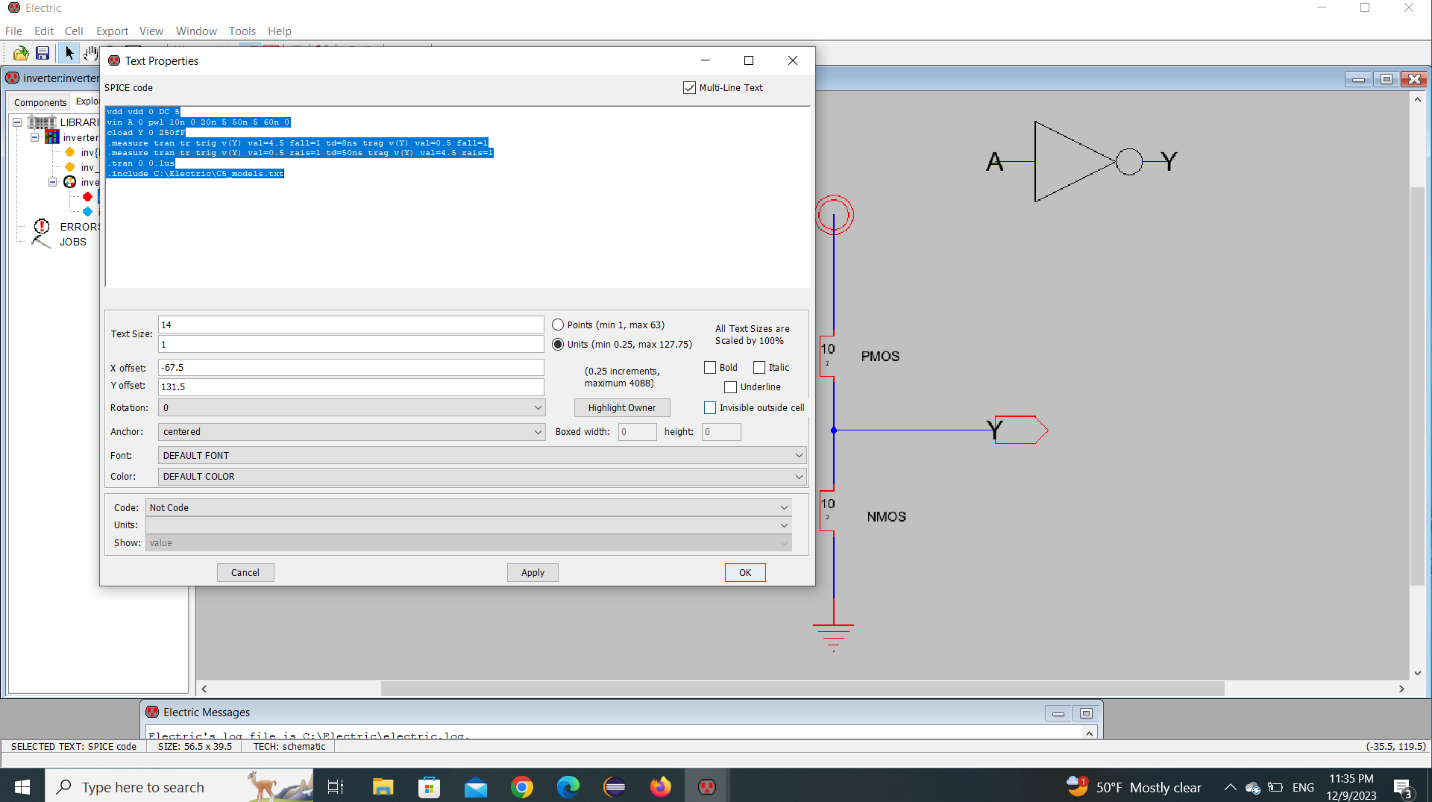
**Date: 11/12/2023.**

**1.CMOS Device (Inverter Gate)**

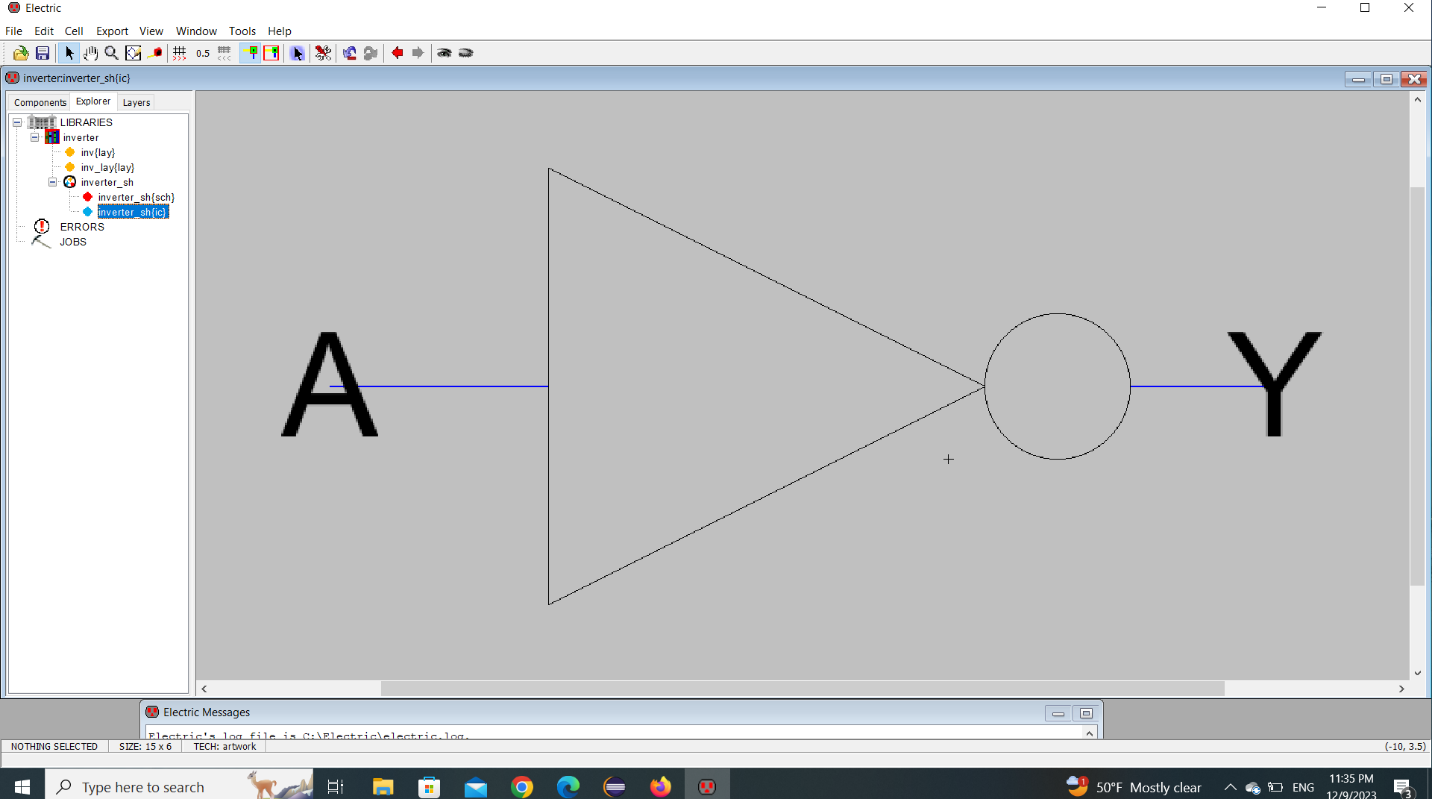
Inverter on schematic:

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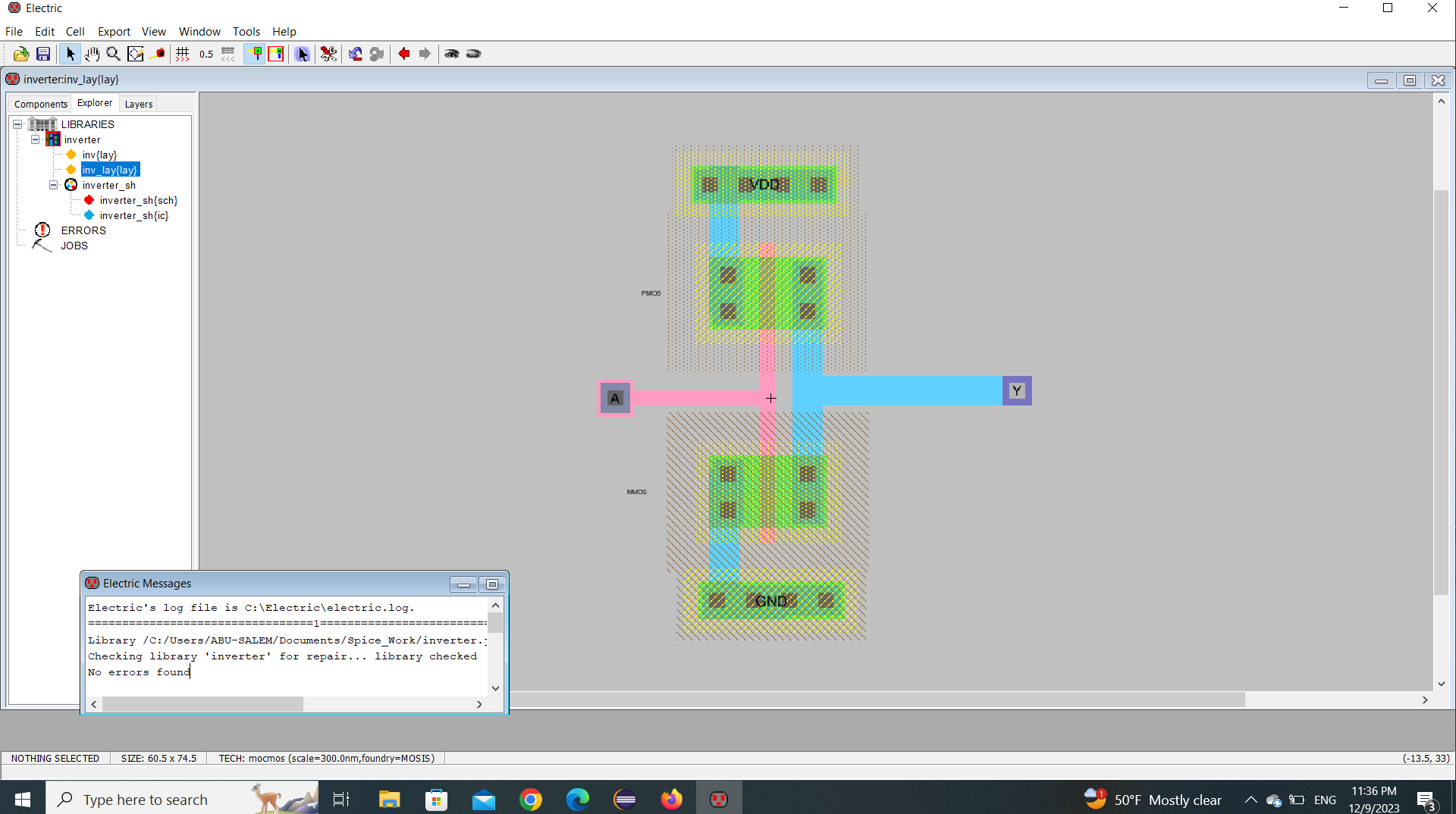
Inverter code:

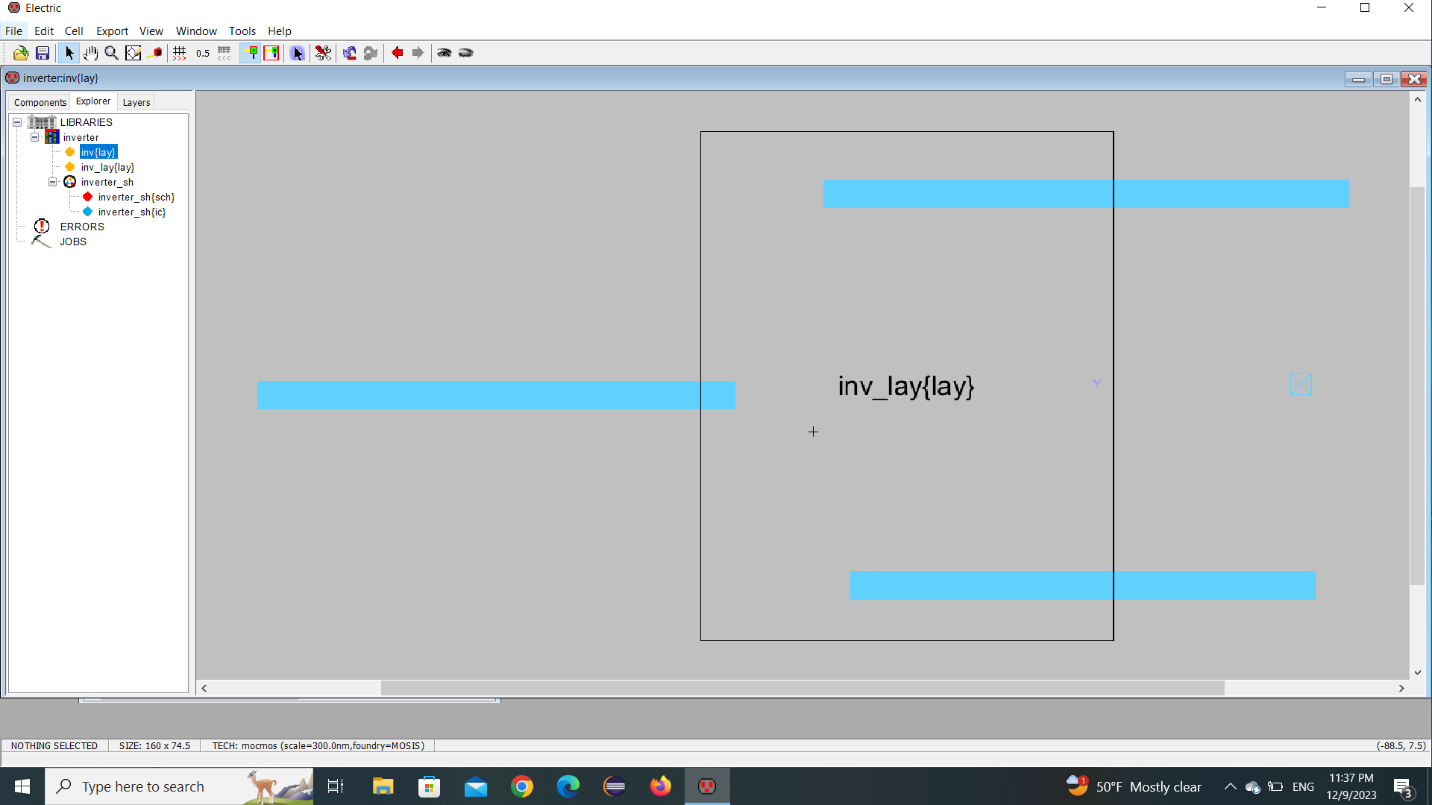


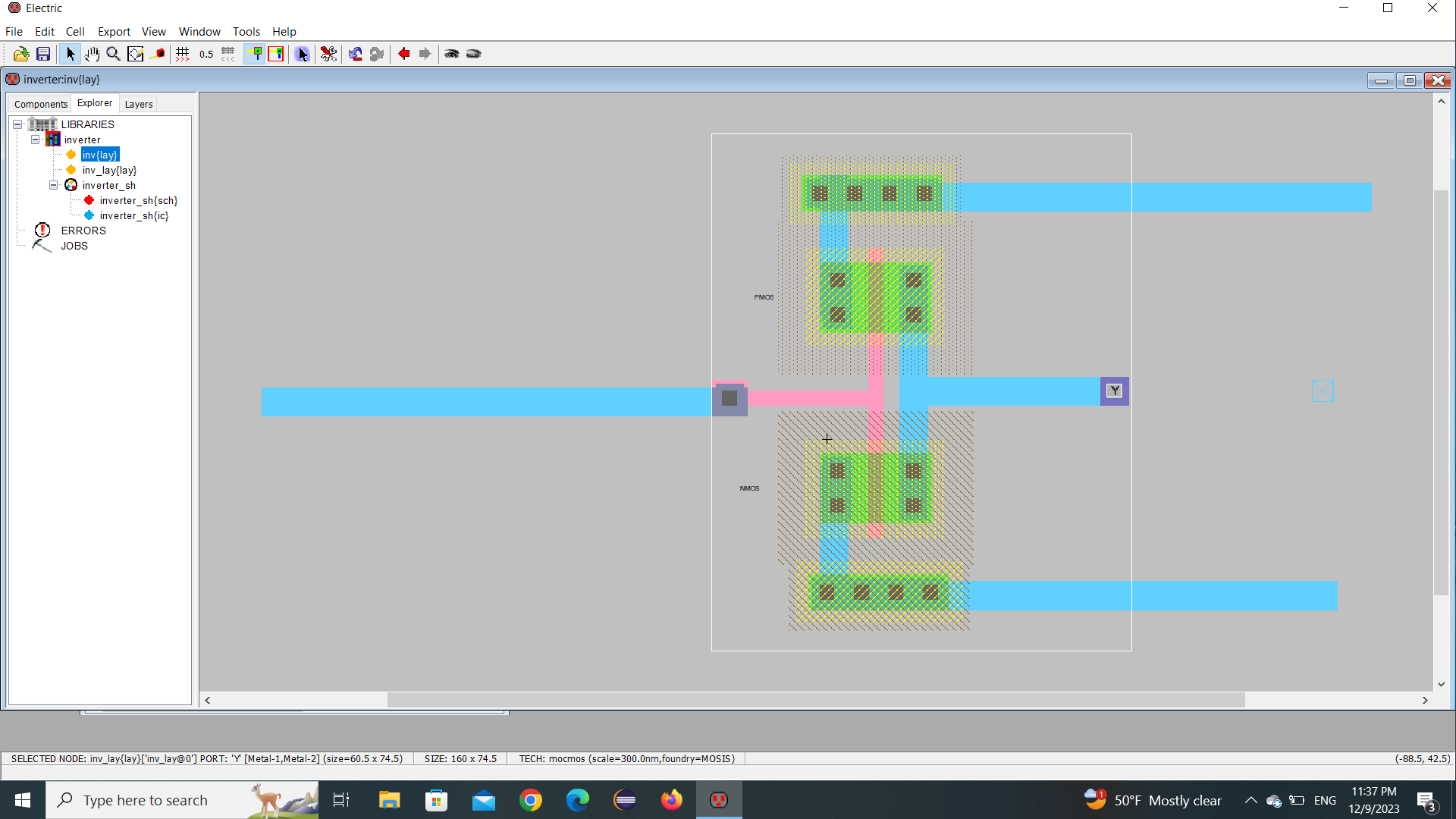
Inverter icon:



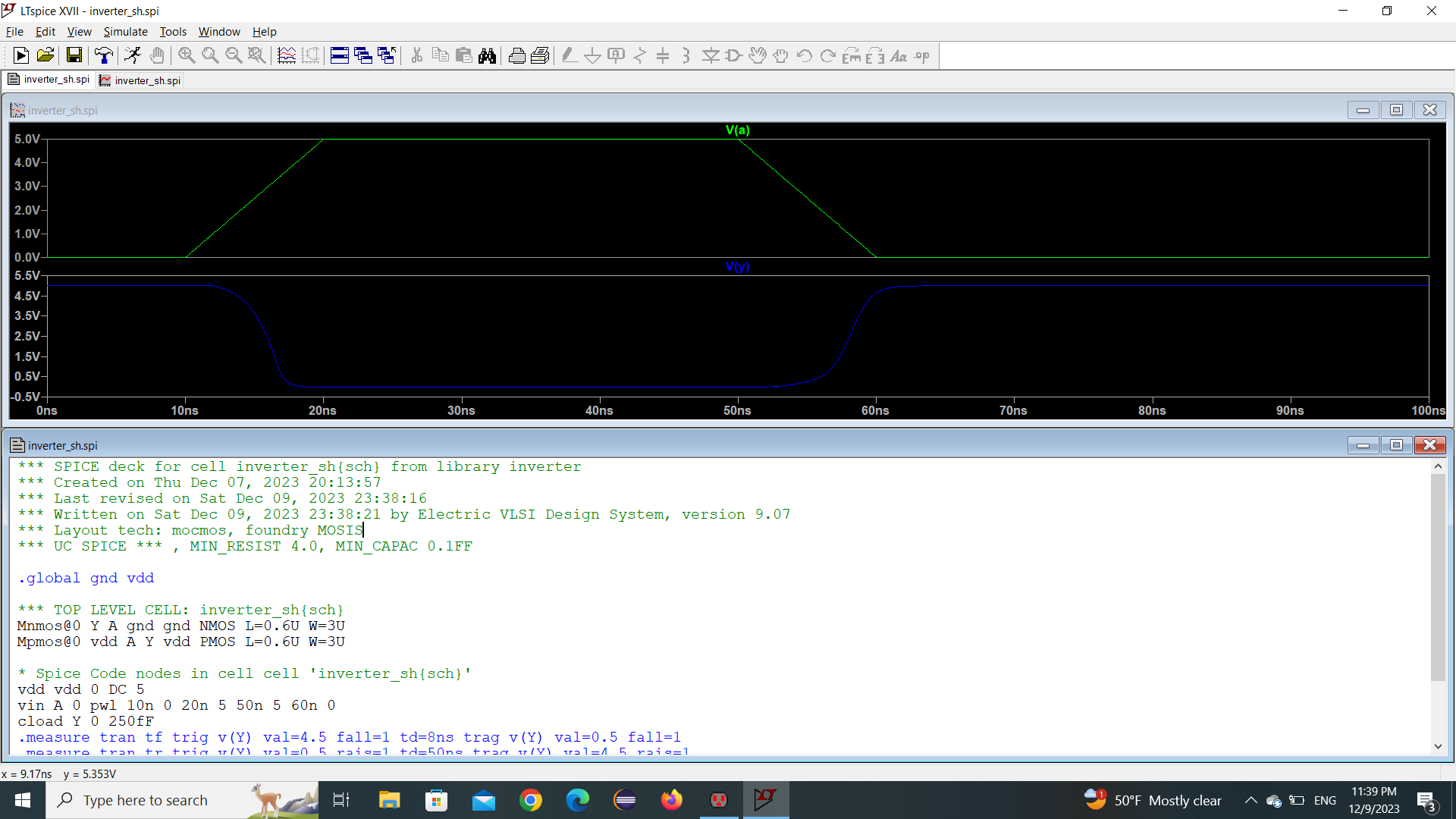
Inverter in layout



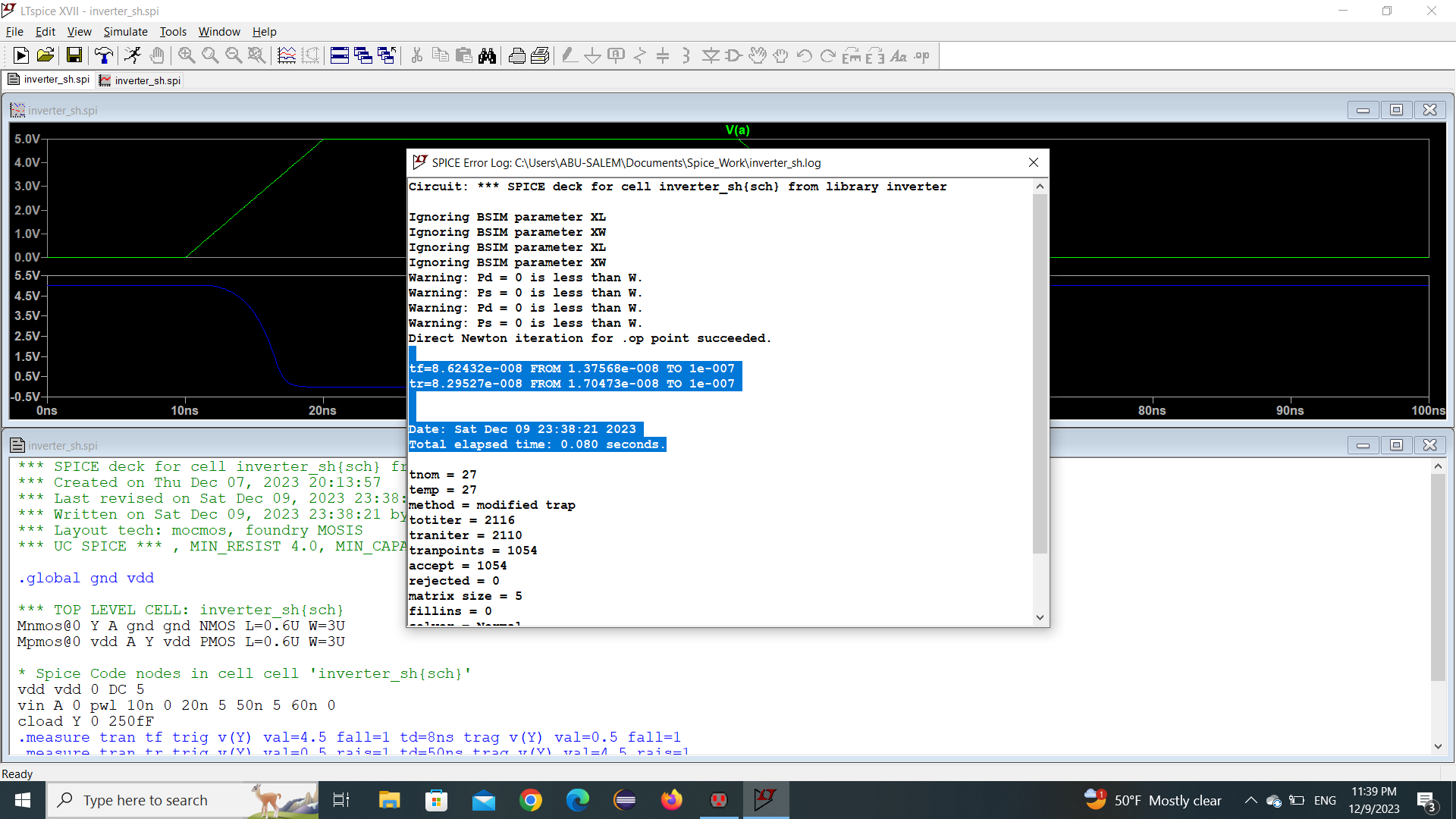




Elaborate results, and waveform:

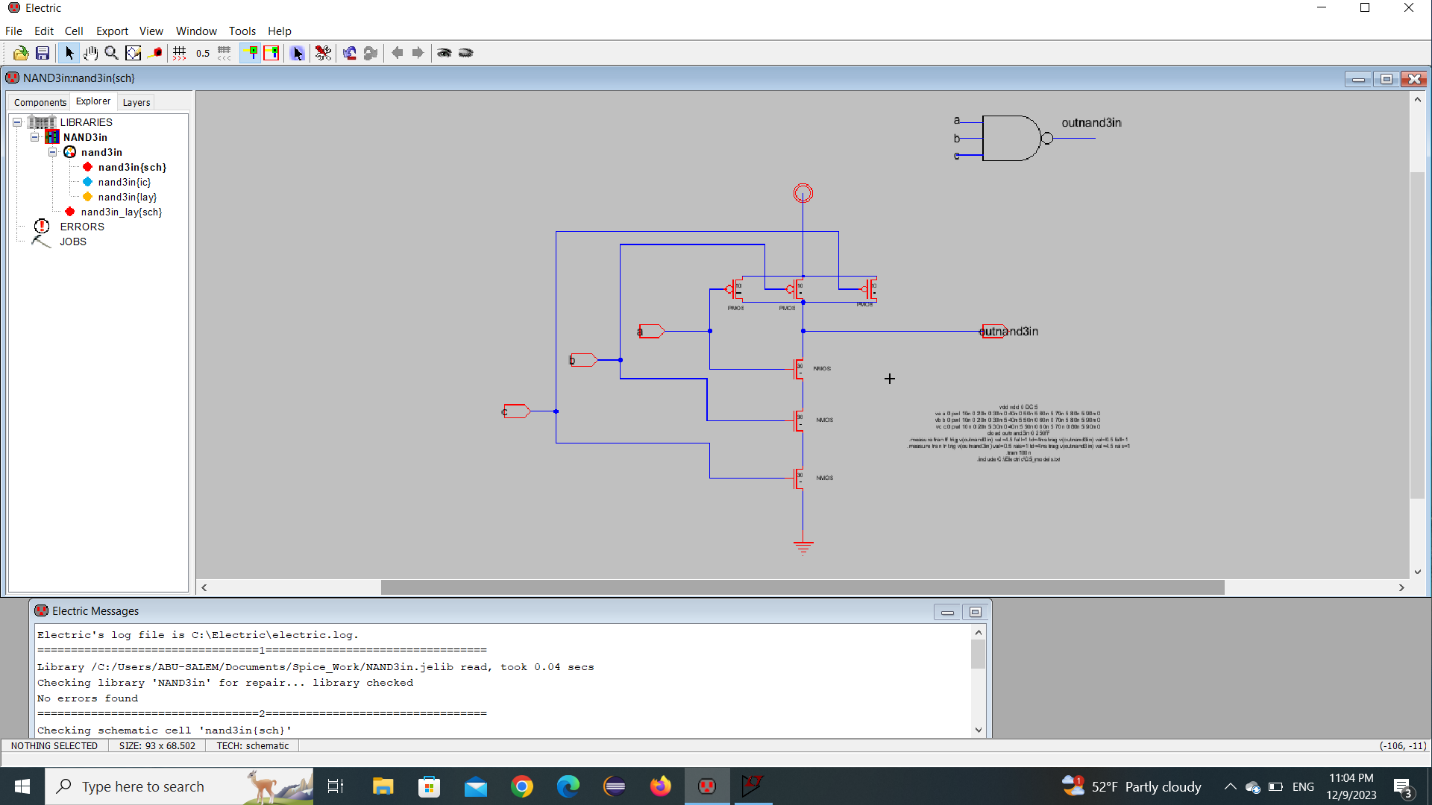


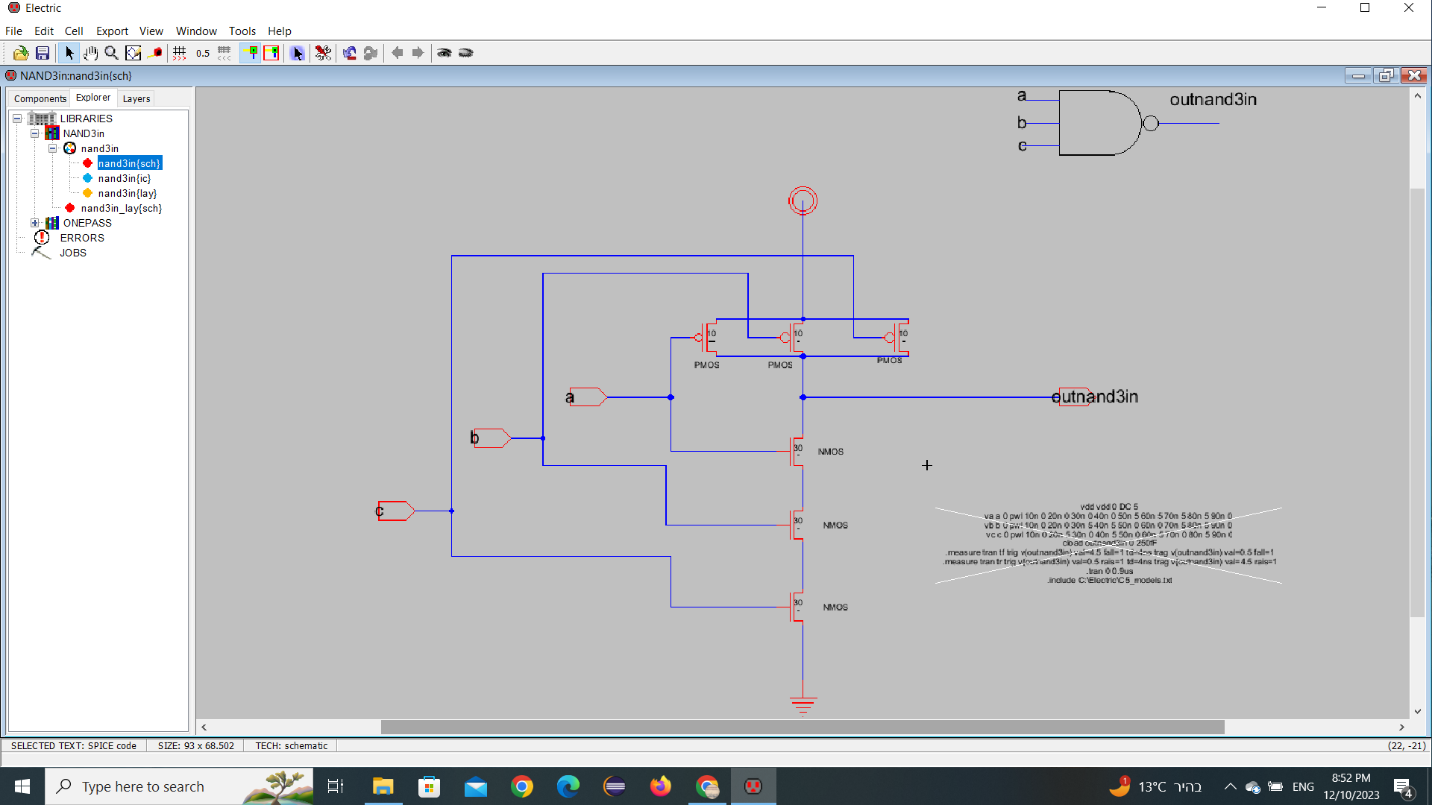
Final result with tr and tf :



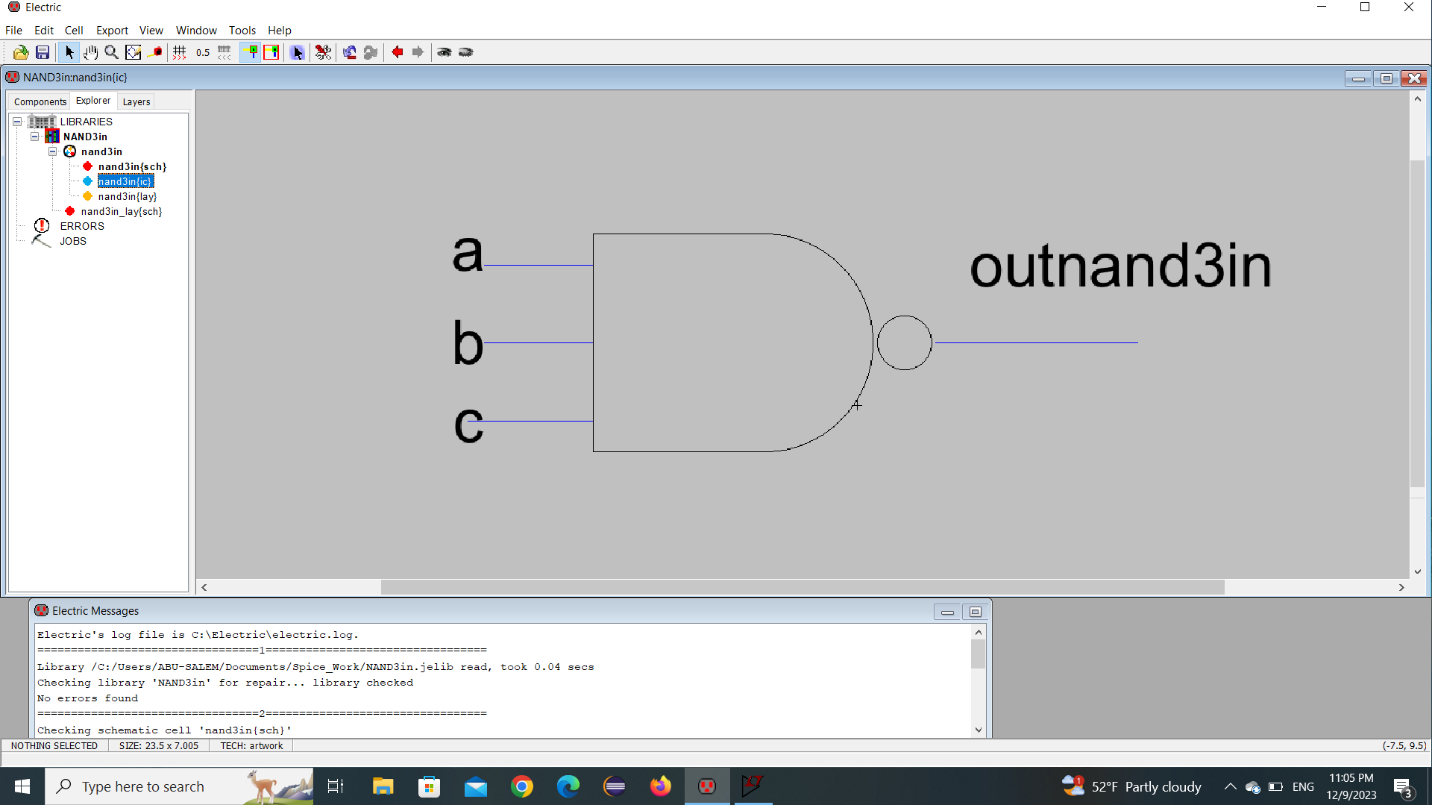
**2. three input NAND Gate**

Three input NAND gate on schematic:

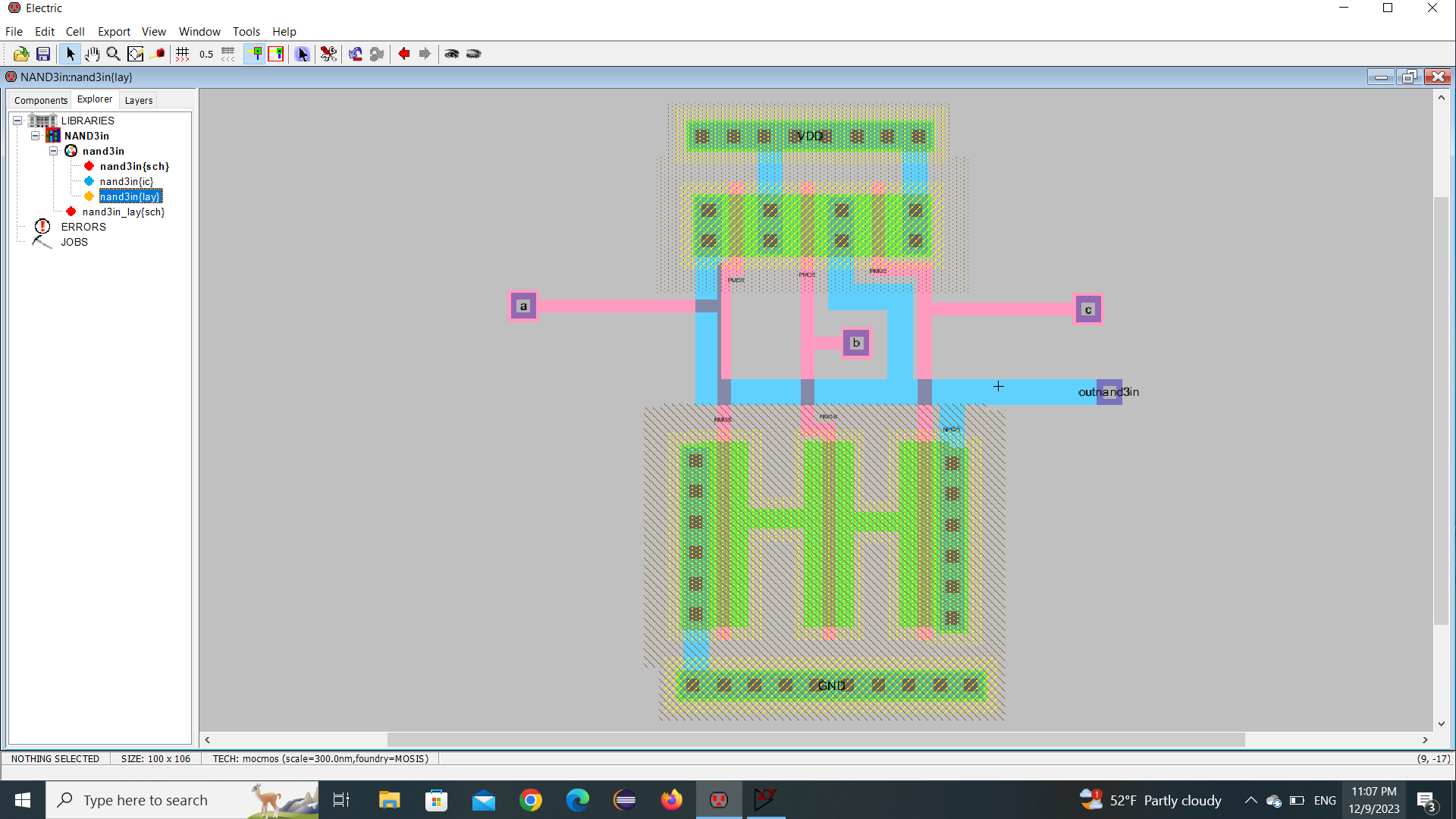
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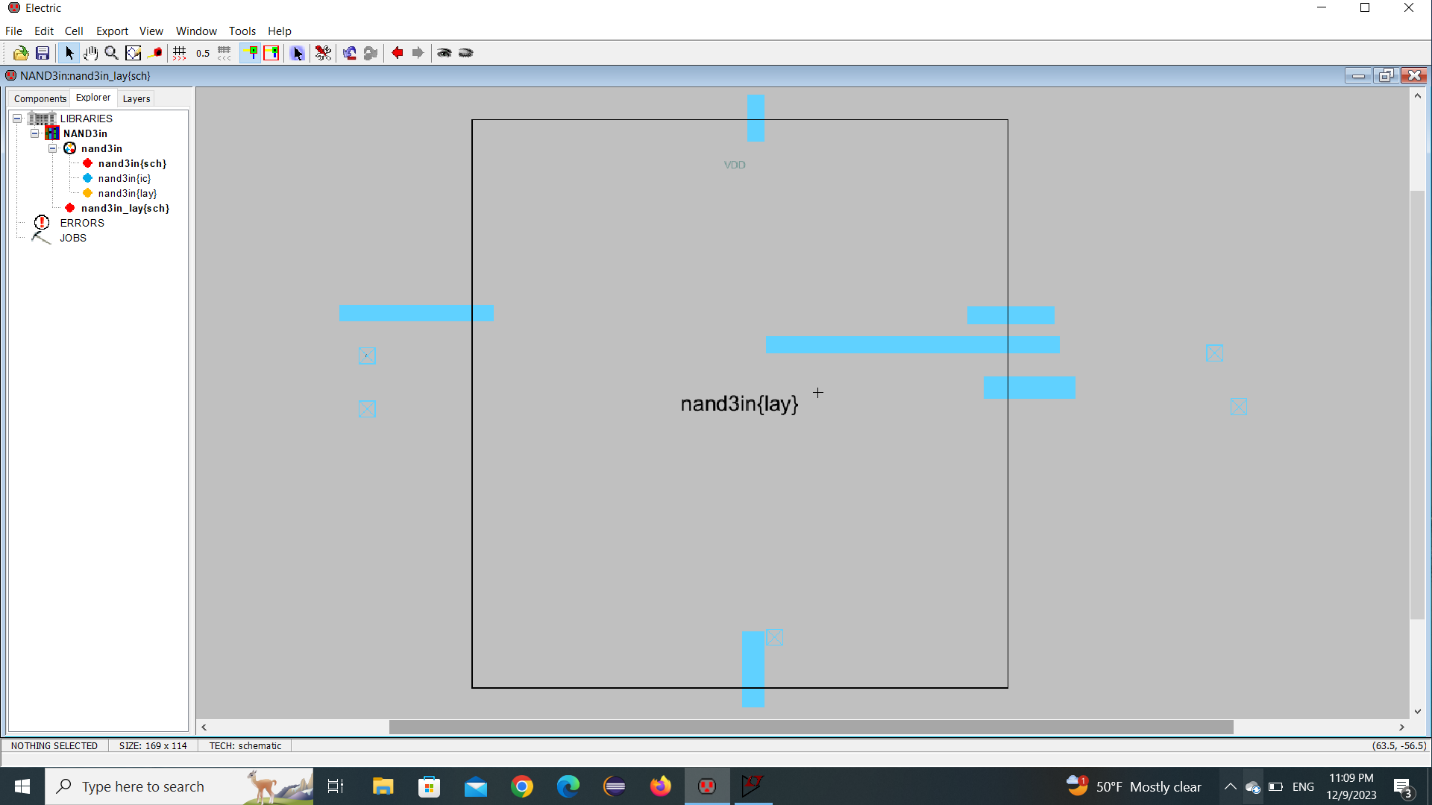


Nand icon:

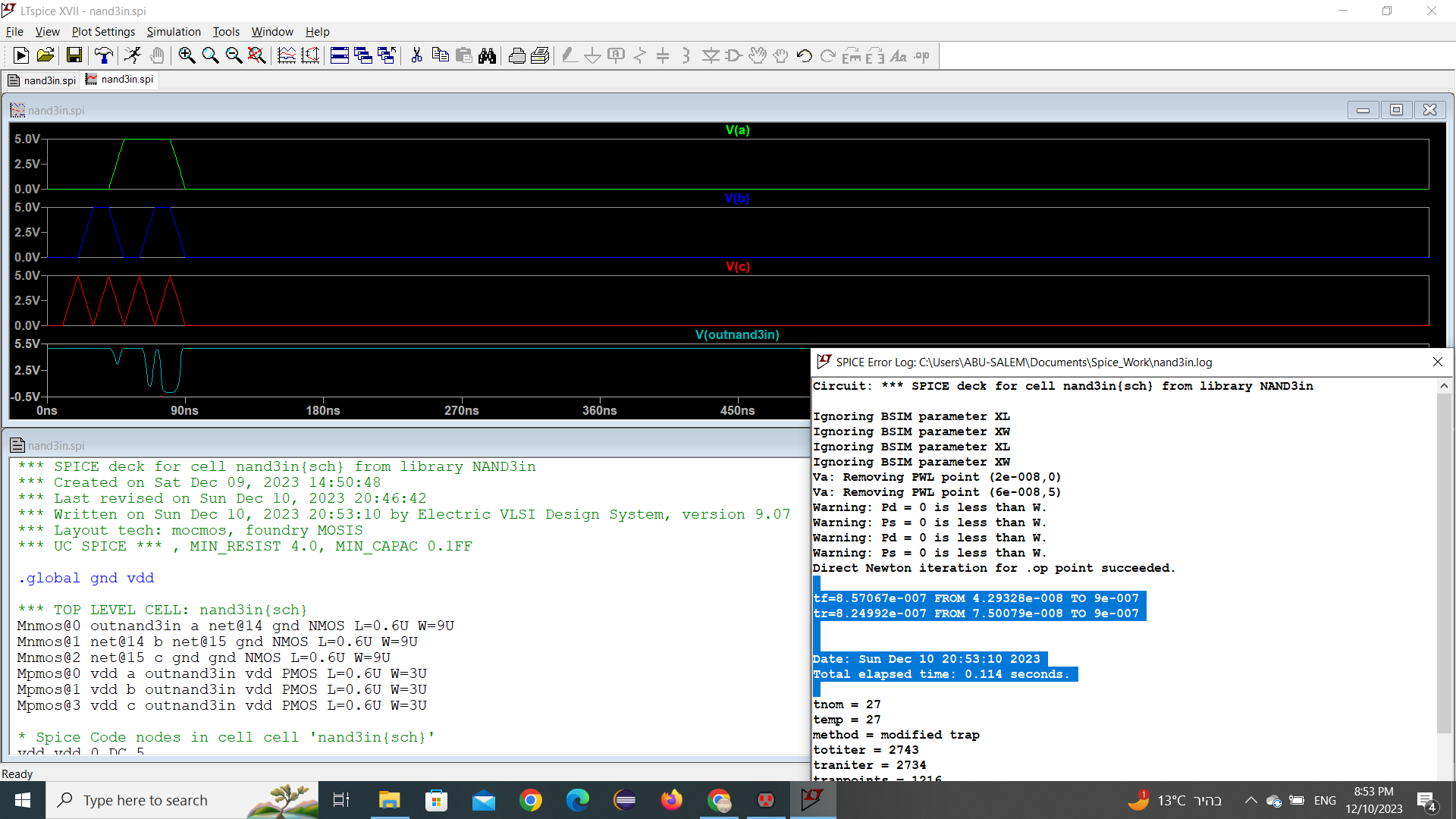


NAND Layout:



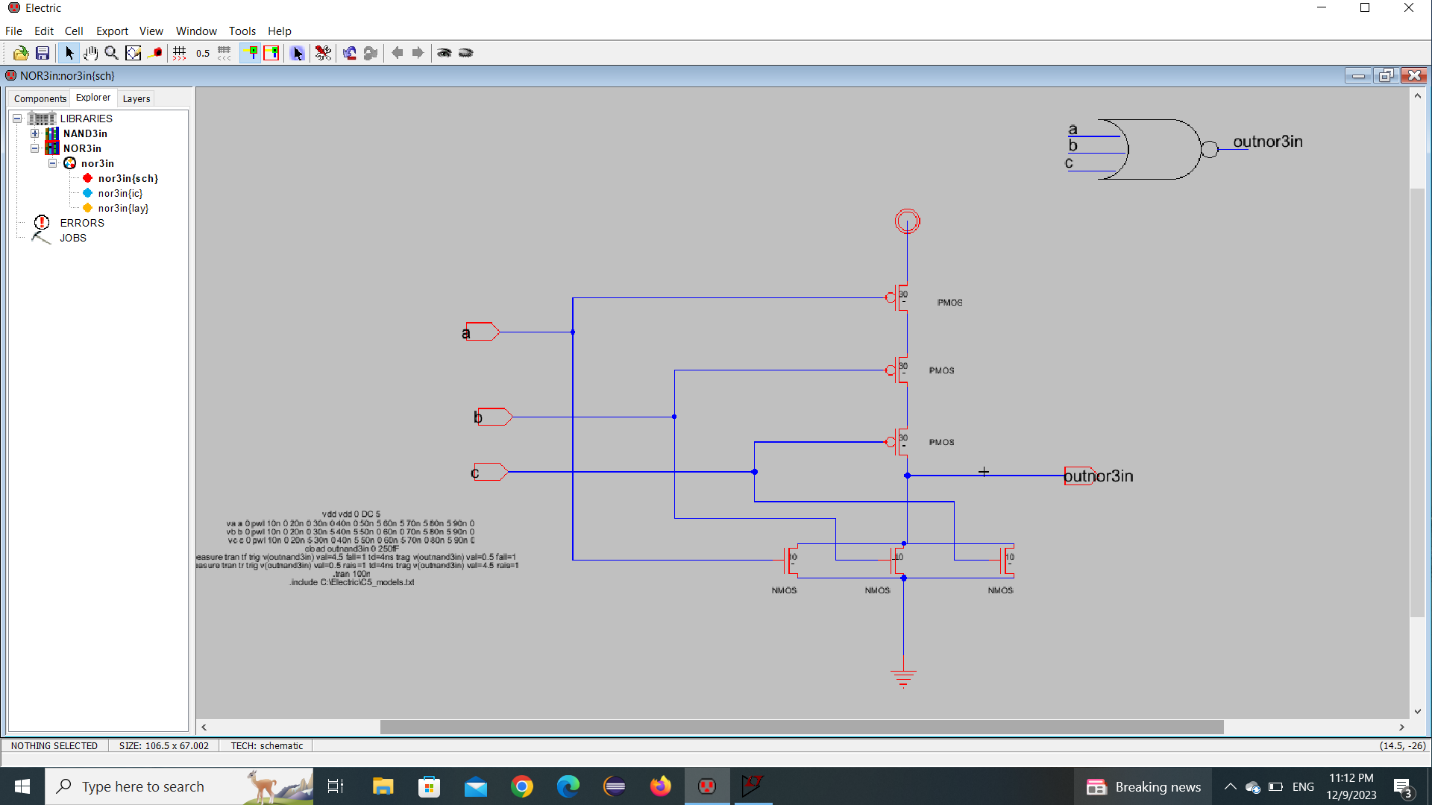


Final result with tr and tf :

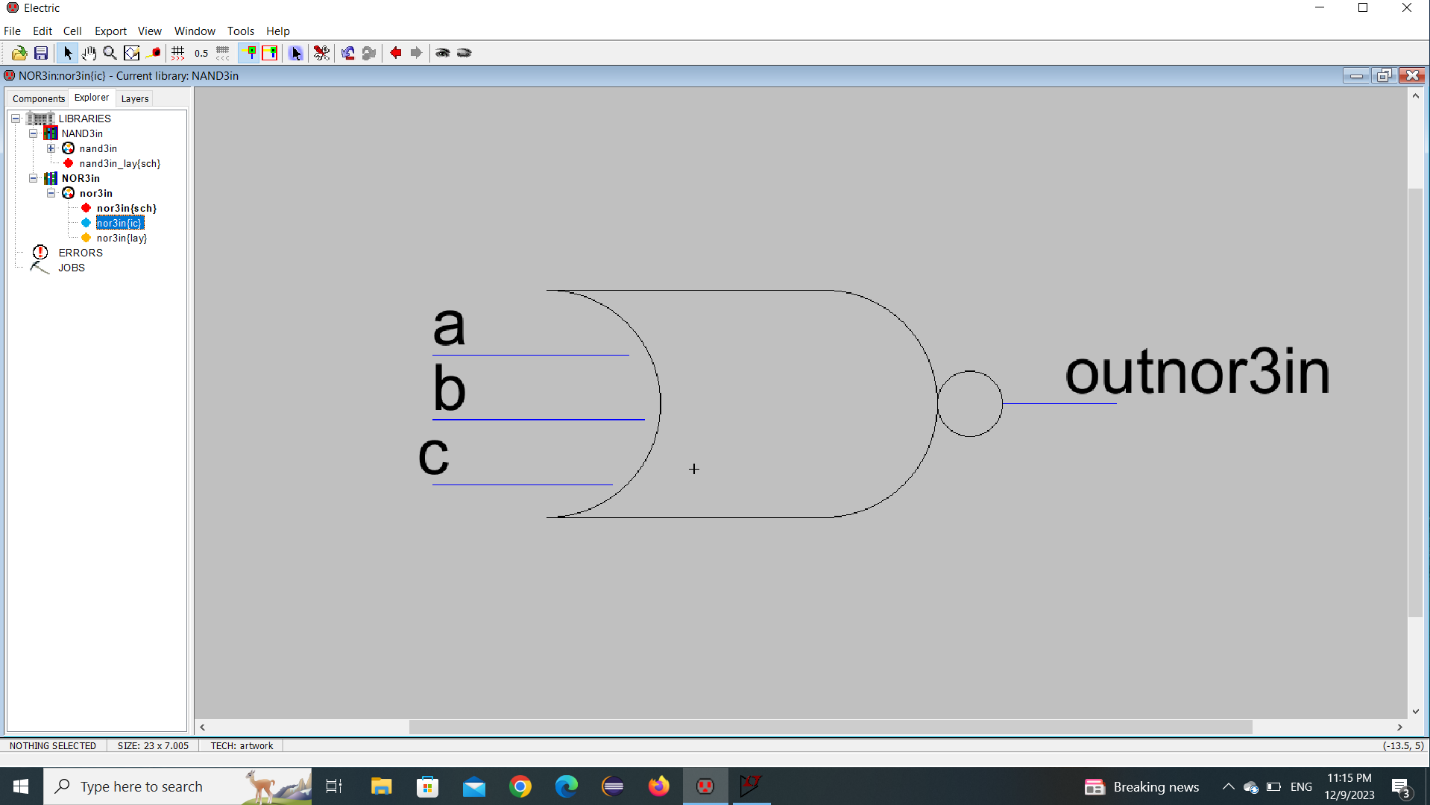


**3. three input NOR Gate**

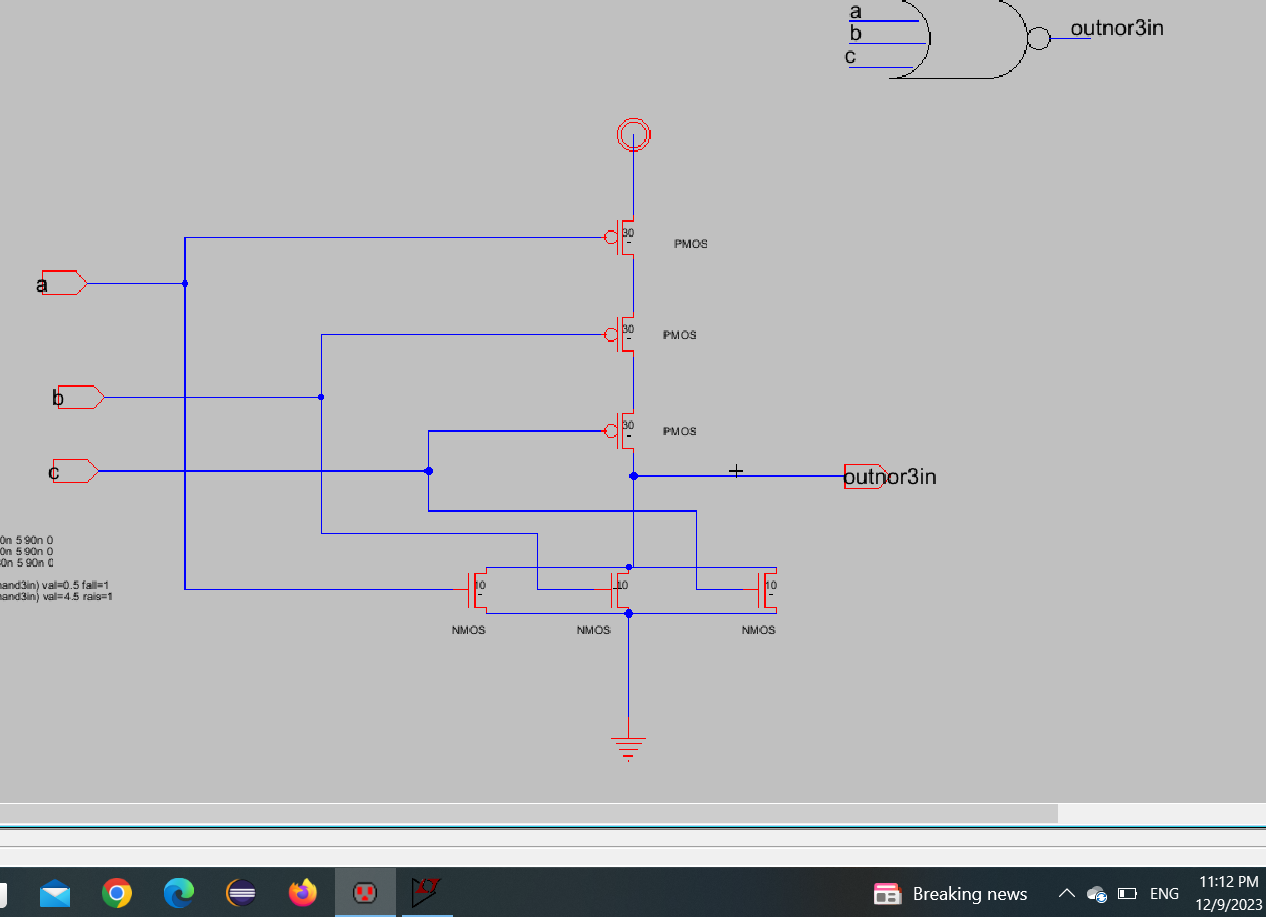
Three input NOR gate in schematic

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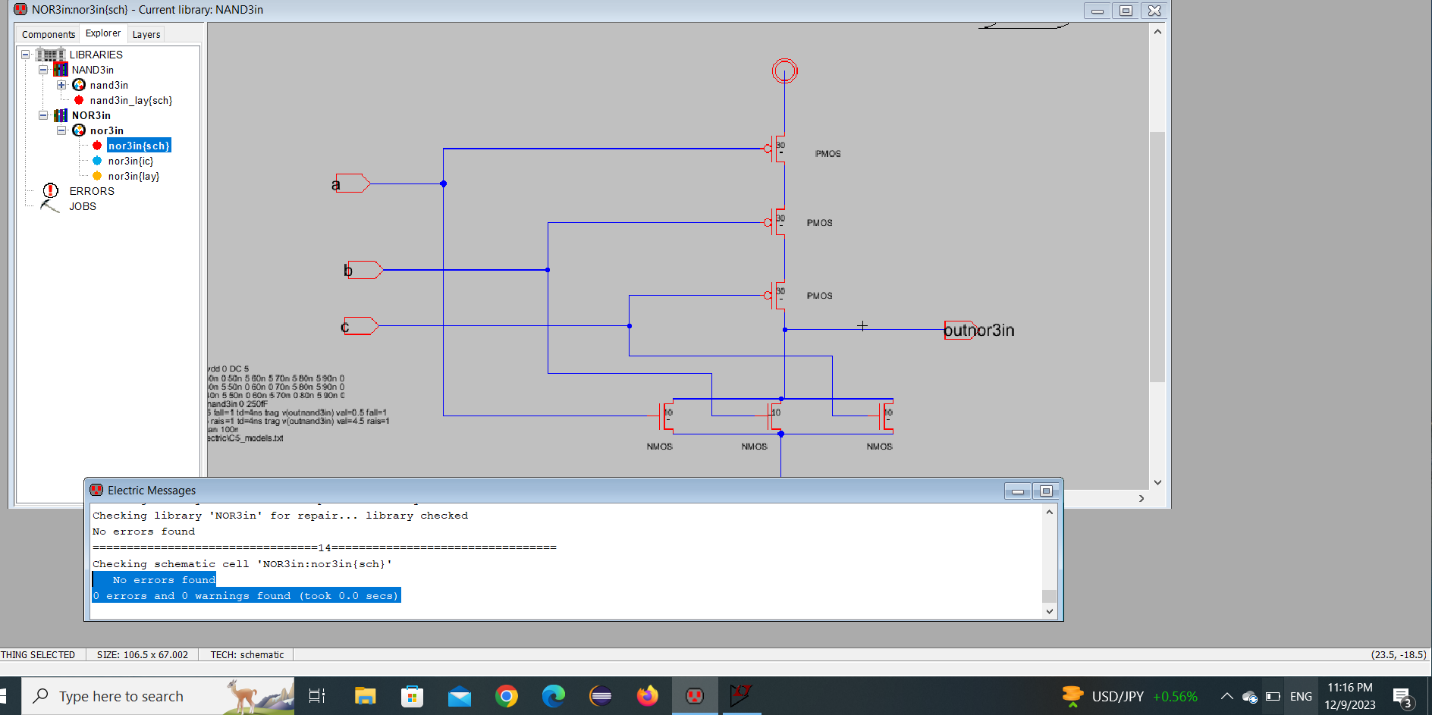
Nor icon:



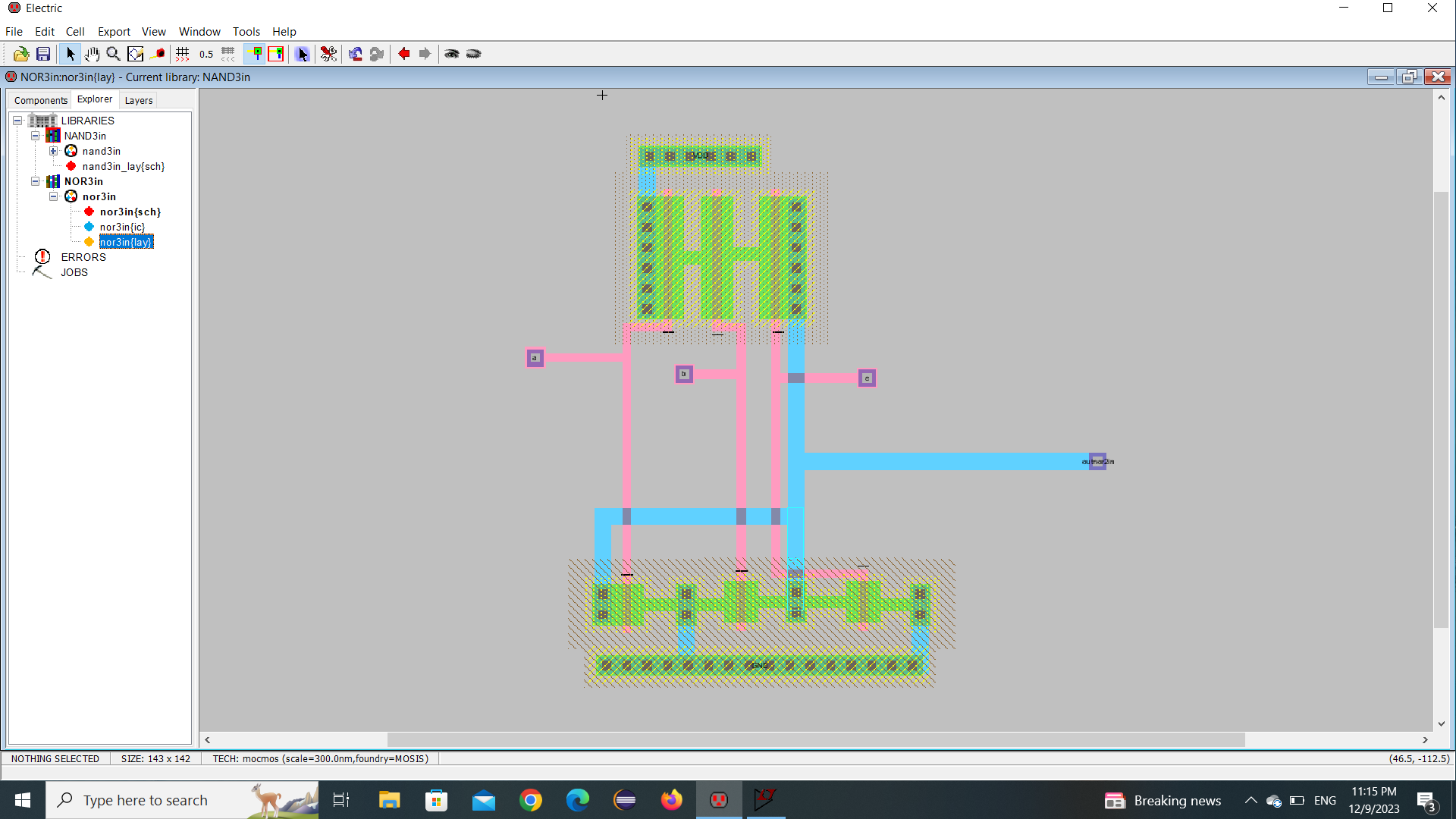
NOR Sizing:



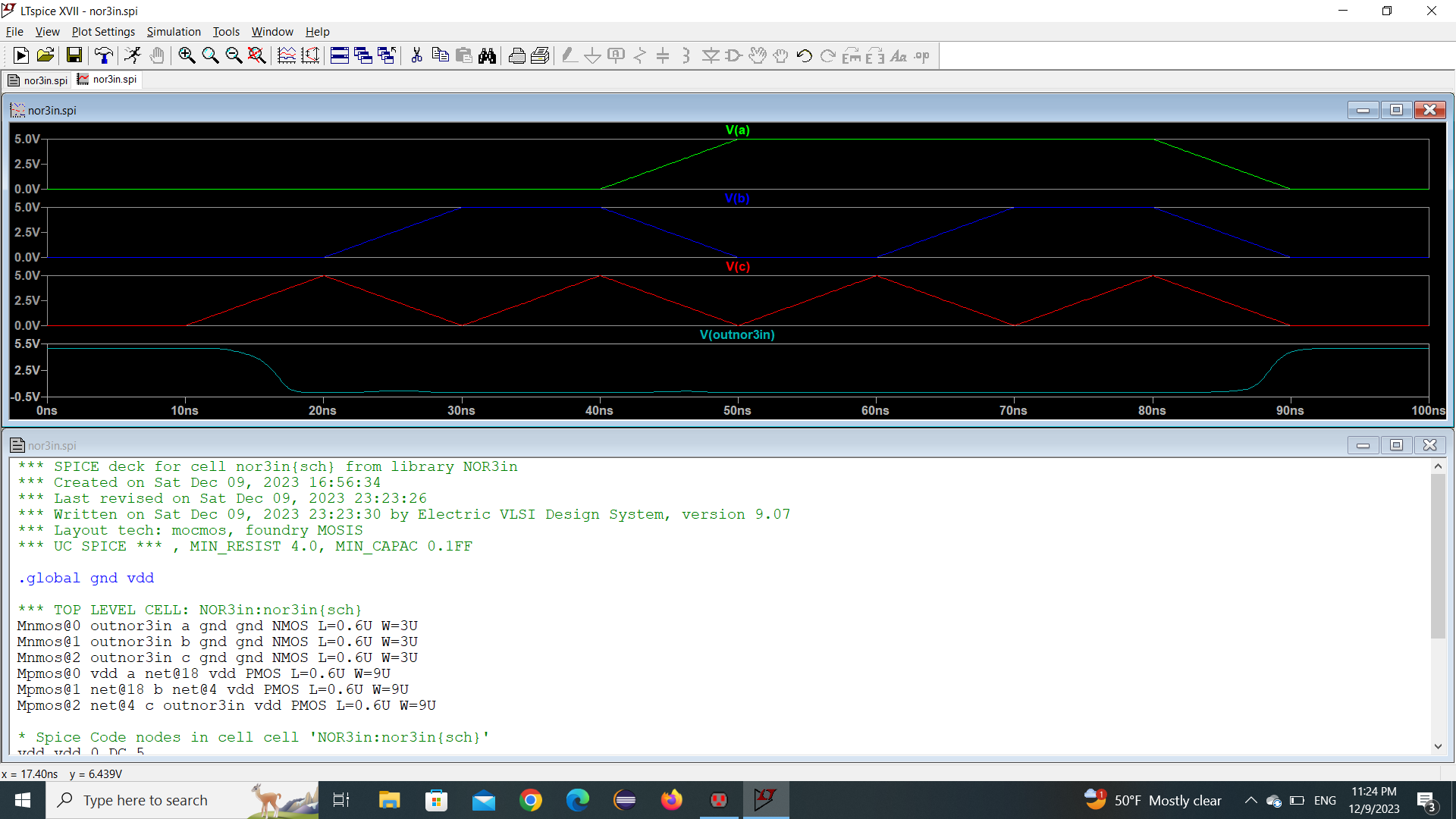
No error Befor run:



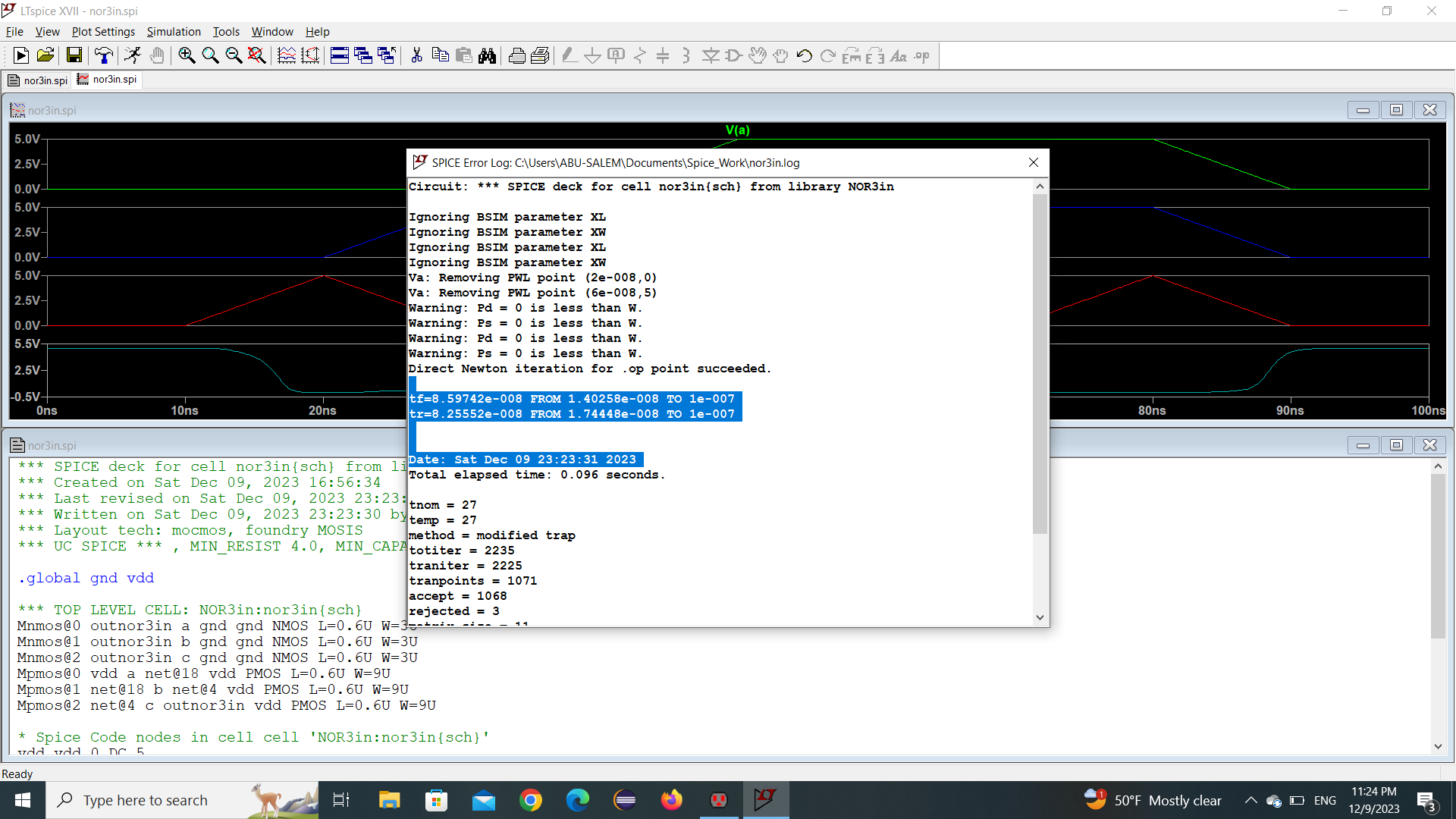
Nor Layout:



Nor elabrate with waveform:

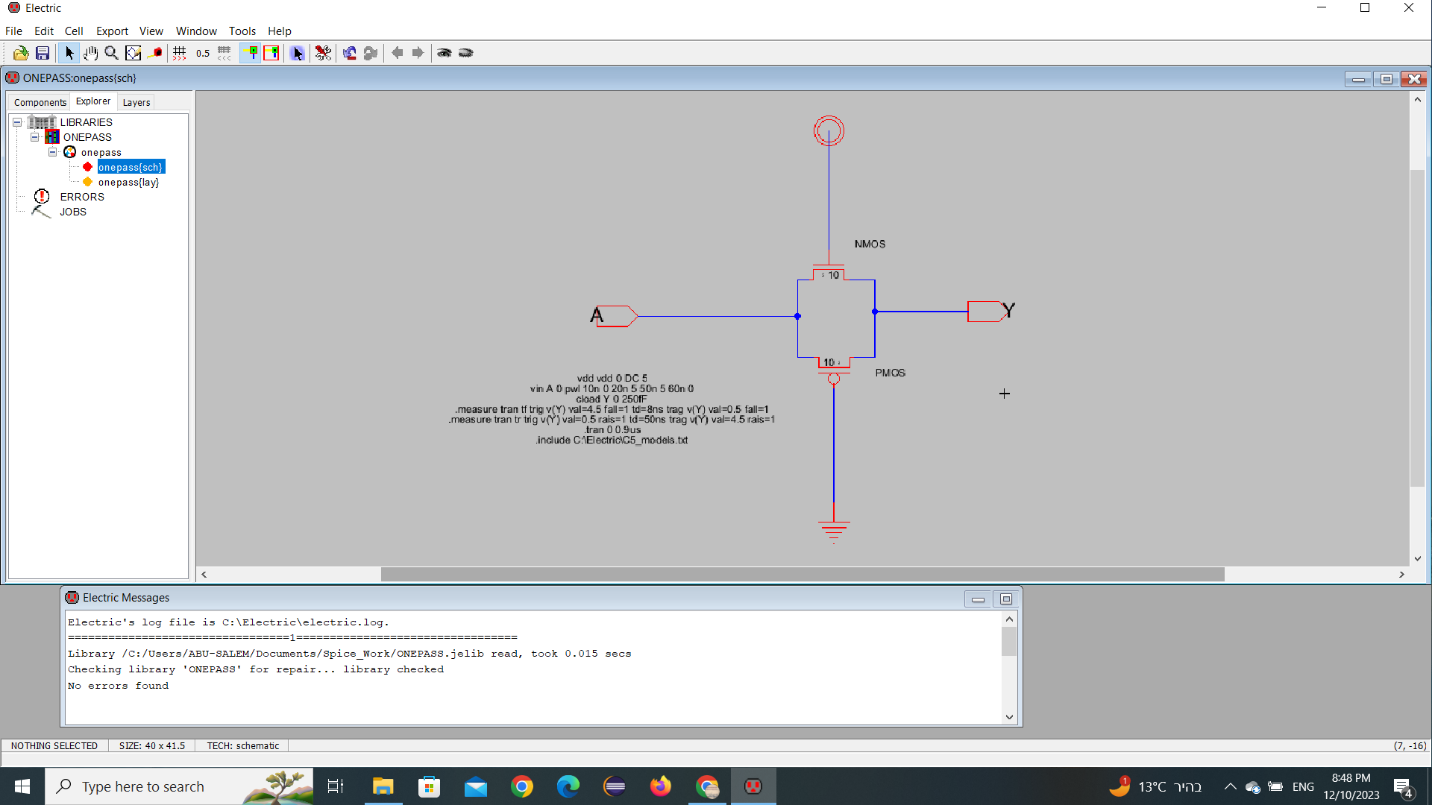


Final result with tr and tf :

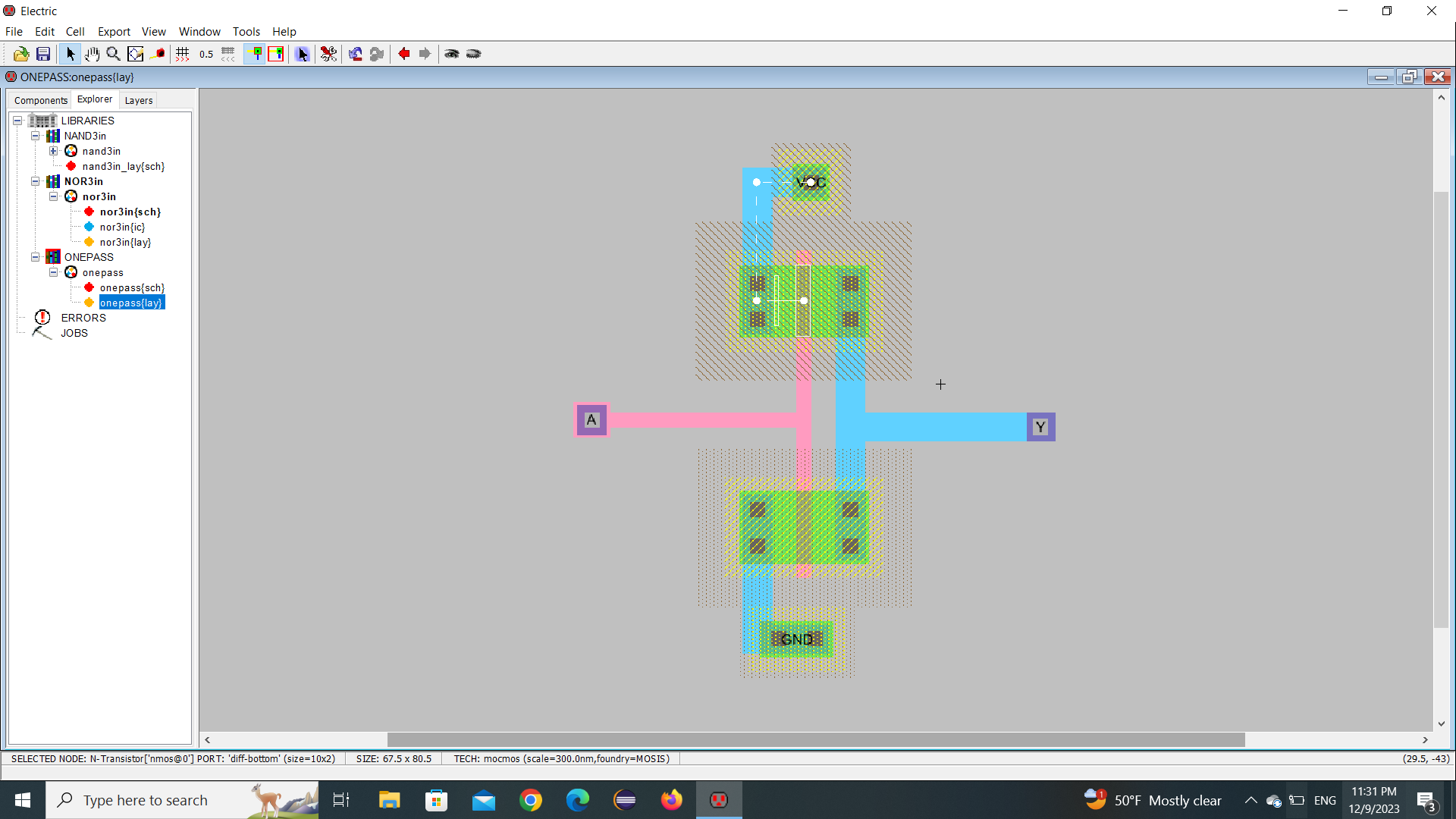


**4.One bit Pass Gate**

One bit pass gate in schematic

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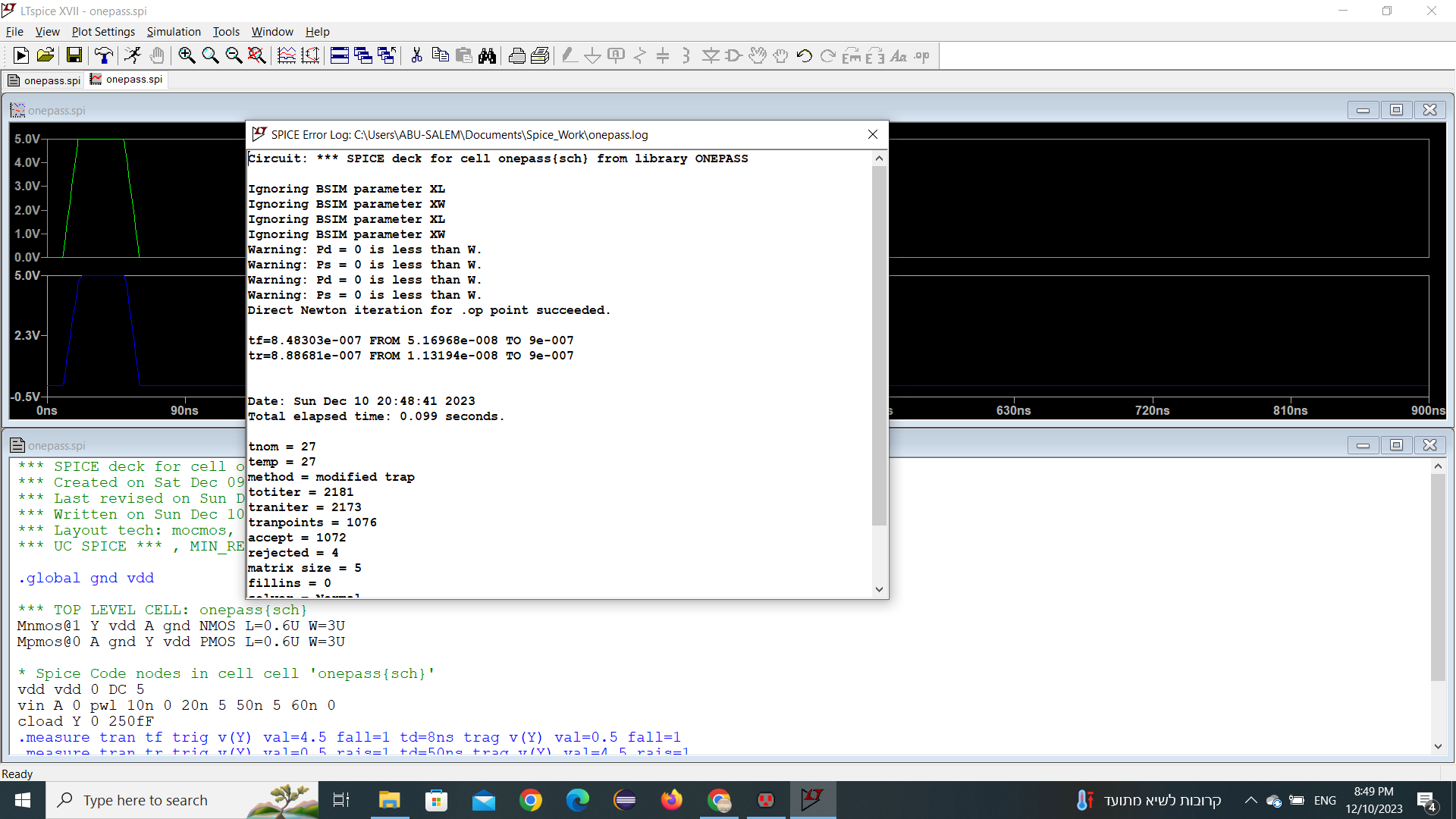
One bit pass gate Layout:



One bit pass gate elabrate with waveform:



Final result with tr and tf :



I put size of NMOS and PMOS are equals (Inverter)

Wn=10 , Wp=10

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Inverter | 3input NAND gate | 3input NOR gate | One bit pass gate |
| Size | Wn+Wp | 90Wn+30Wp | 30Wn+90Wp | Wn+Wp |

The tf and tr are equals at all signals in my designe.

Thancks for reading

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