

**ENCS3330, DIGITAL INTEGRATED CIRCUITS.**

**Assignment #2**

**Student: Mohammad Salem – 1200651.**

**Section 2.**

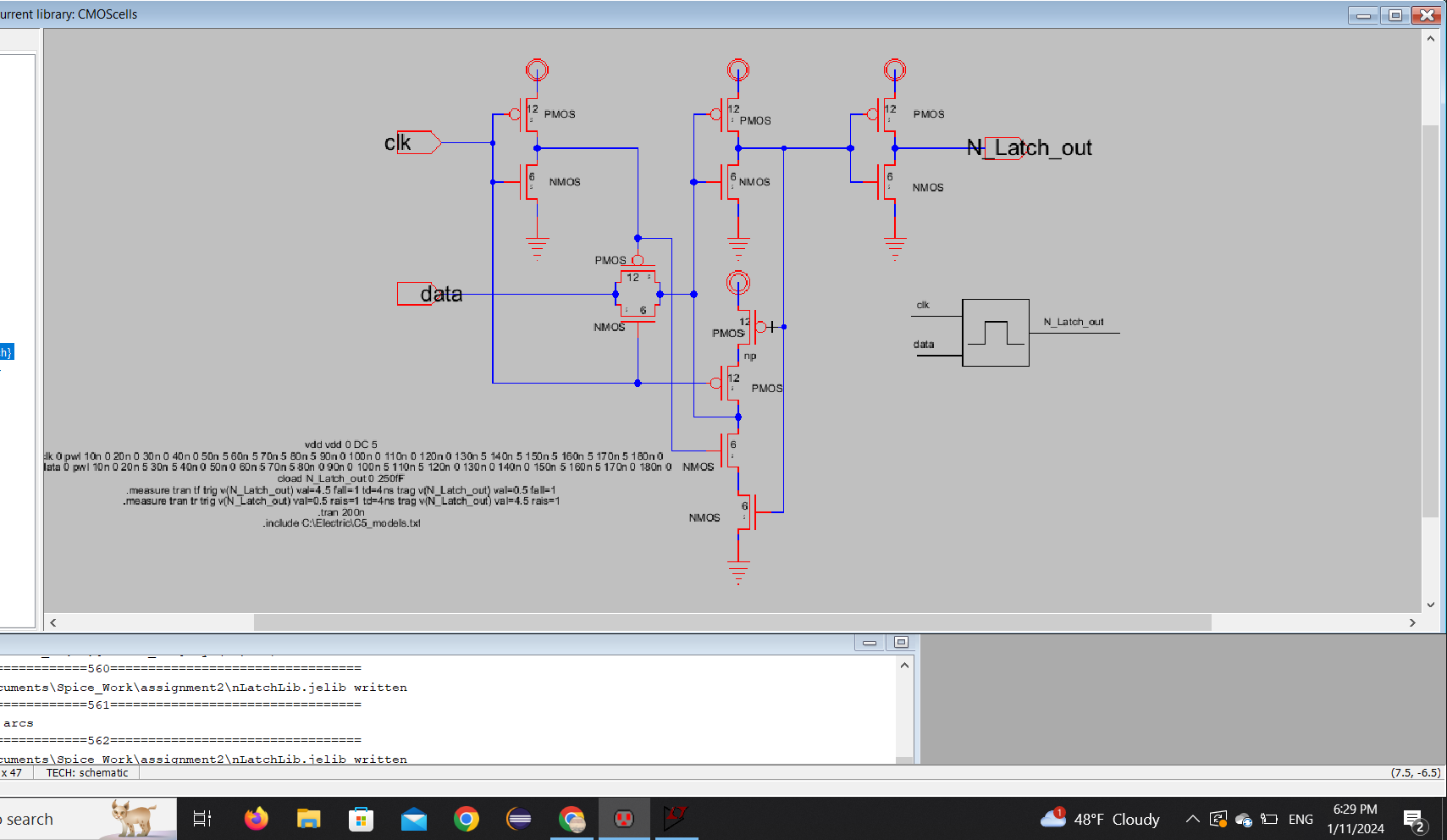
**Dr: Khader Mohammad**

**Date: 14/1/2024.**

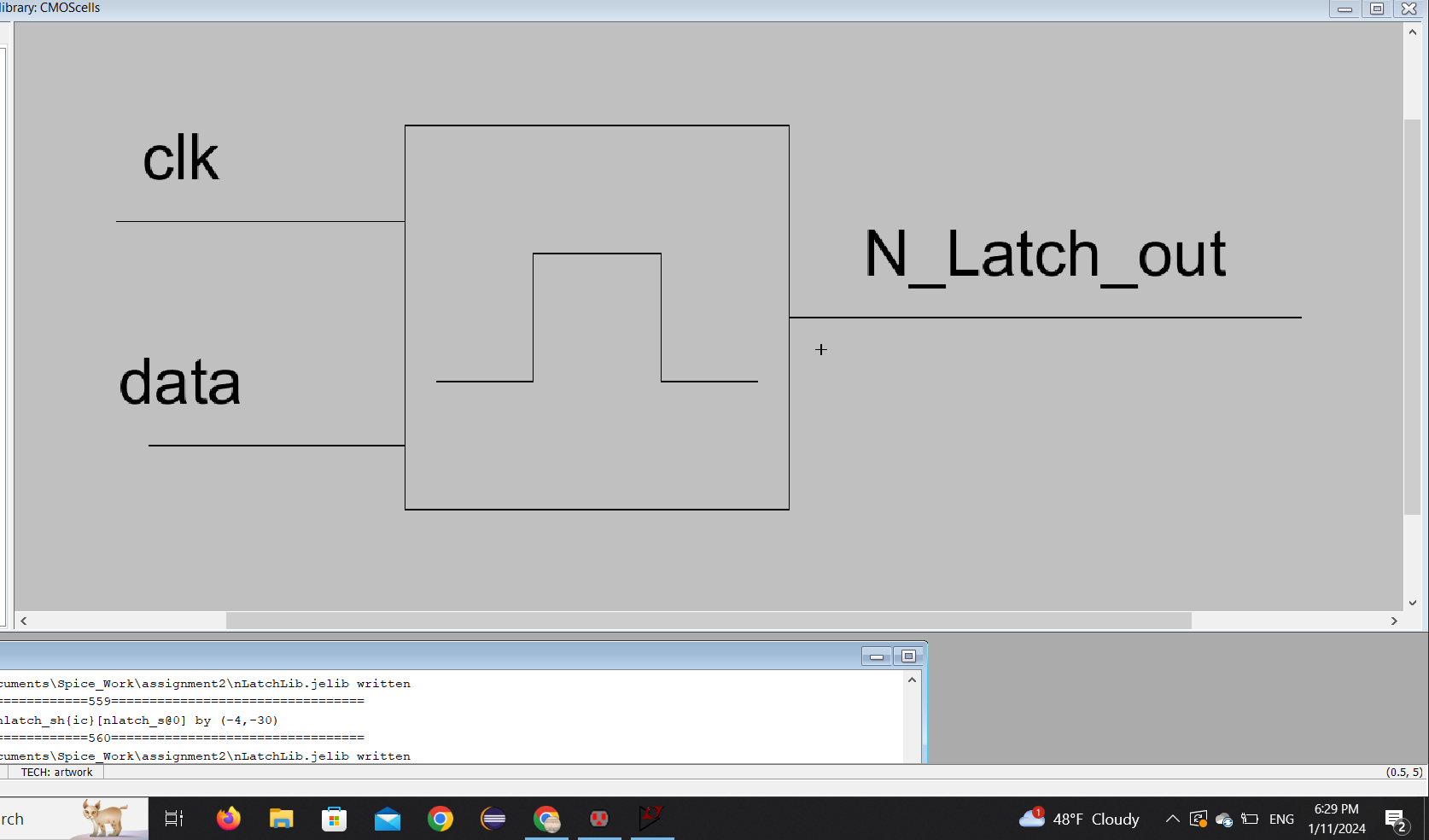
**Assignment #2**

**N-Latch**

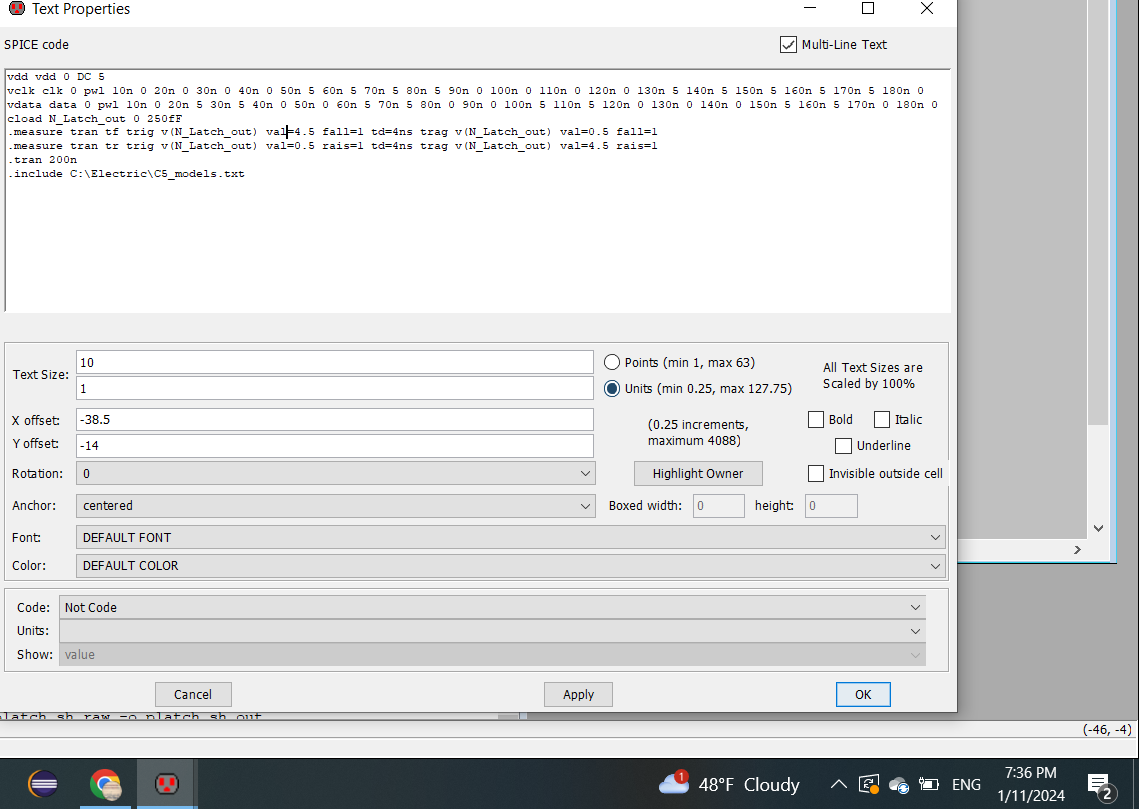
1. **Schematic view**

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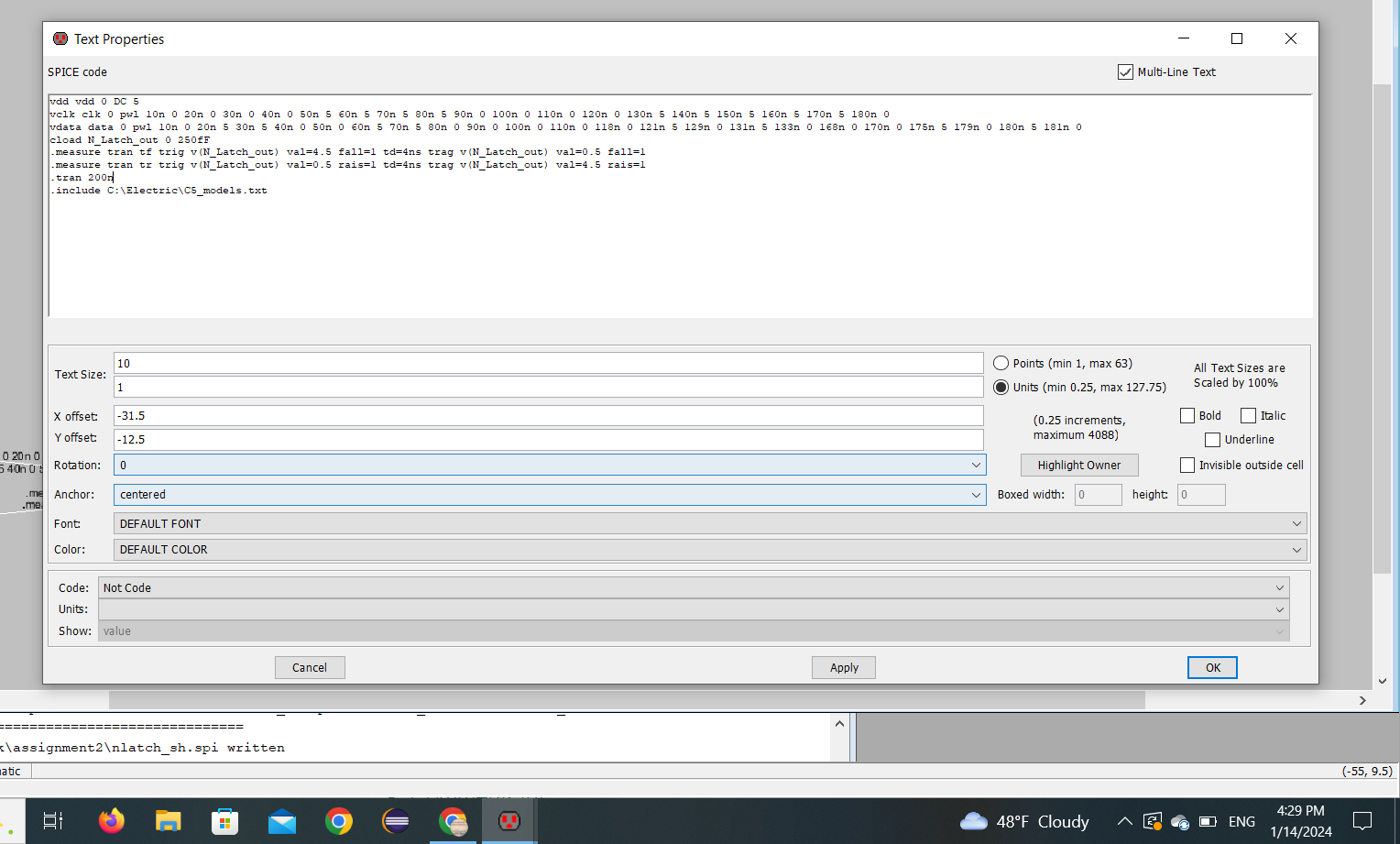
**2.Icon view**

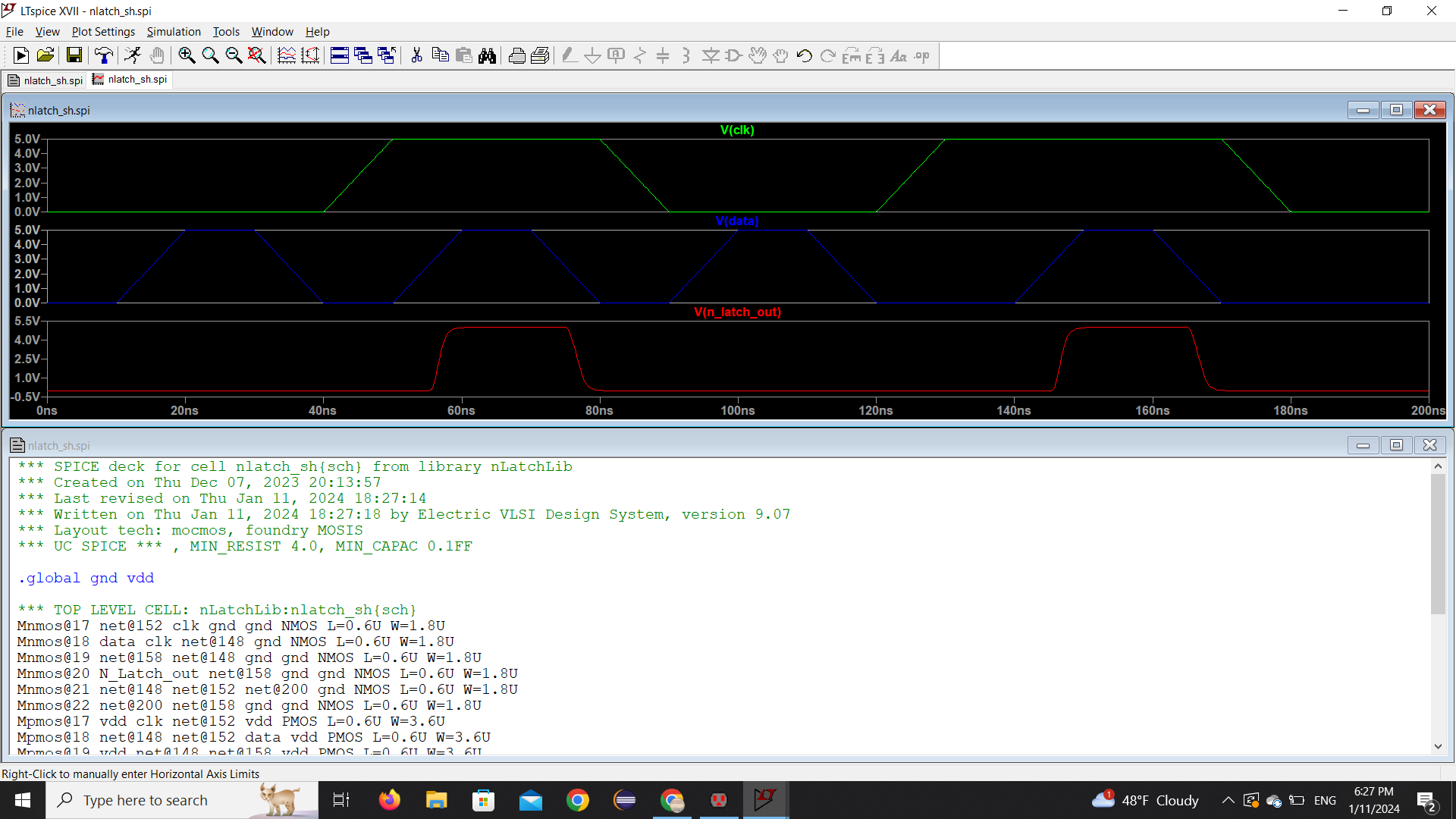
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**3.Code view**

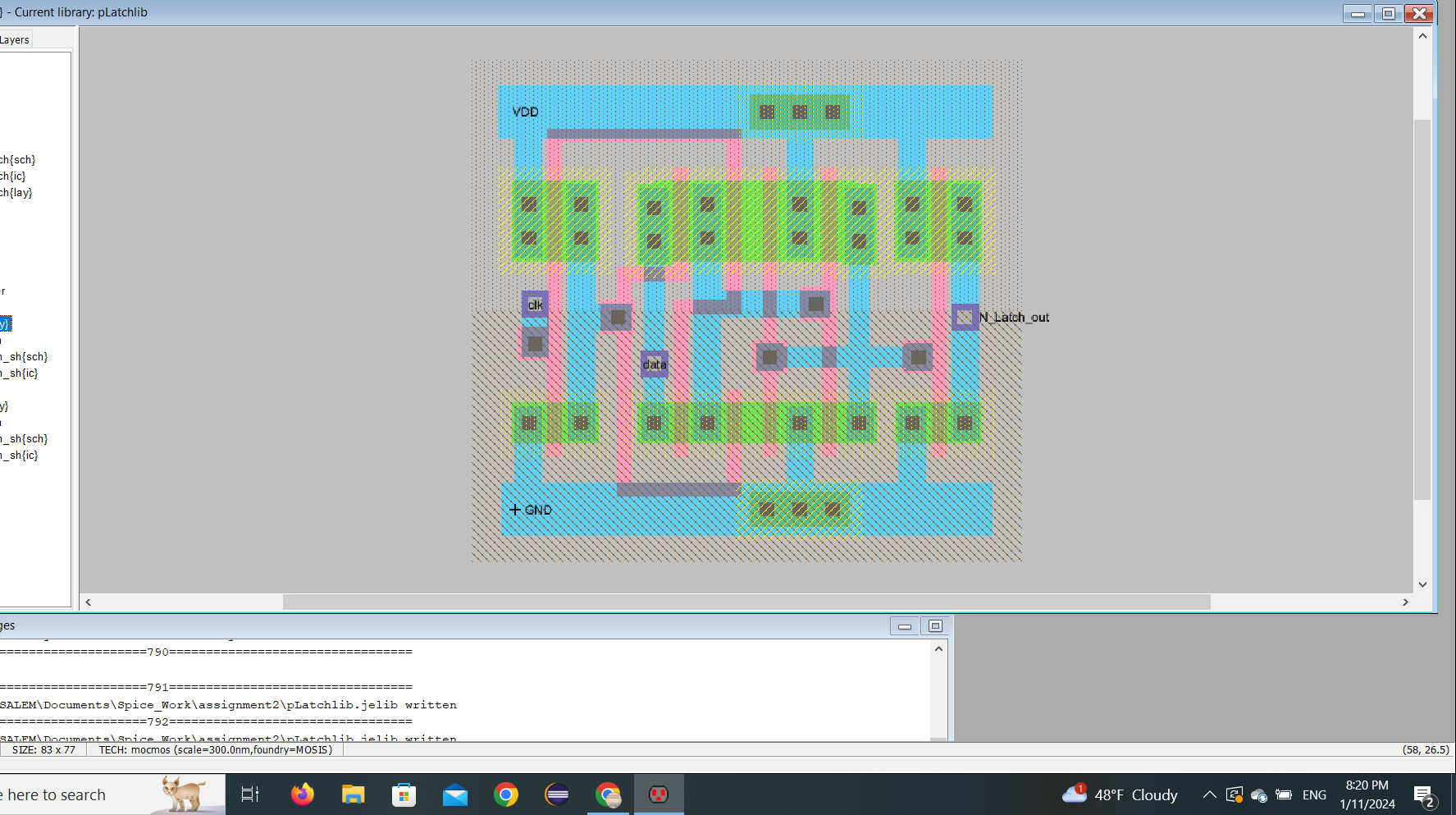
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**4.Delay to out and clk to out as appears in the following figure.**

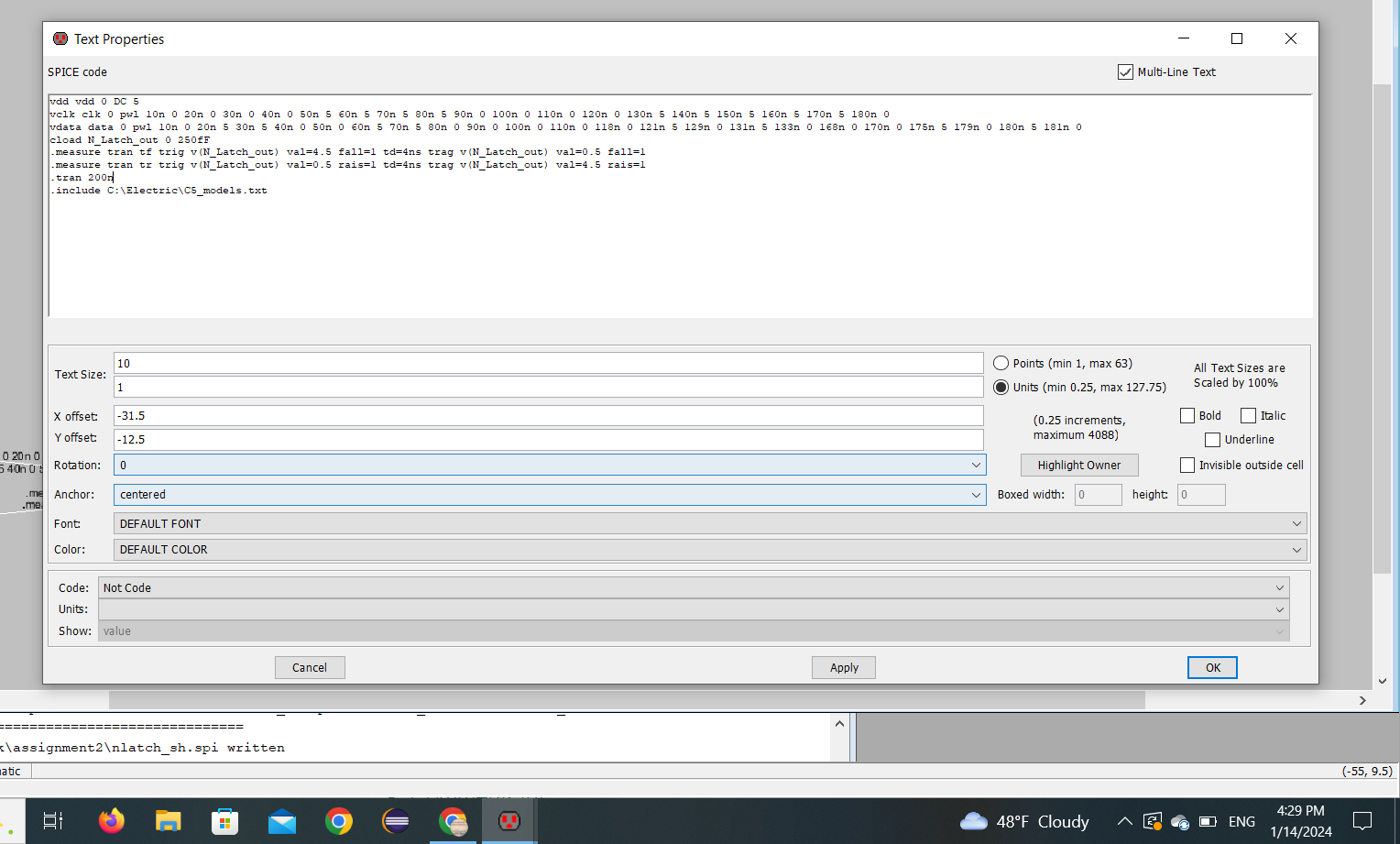
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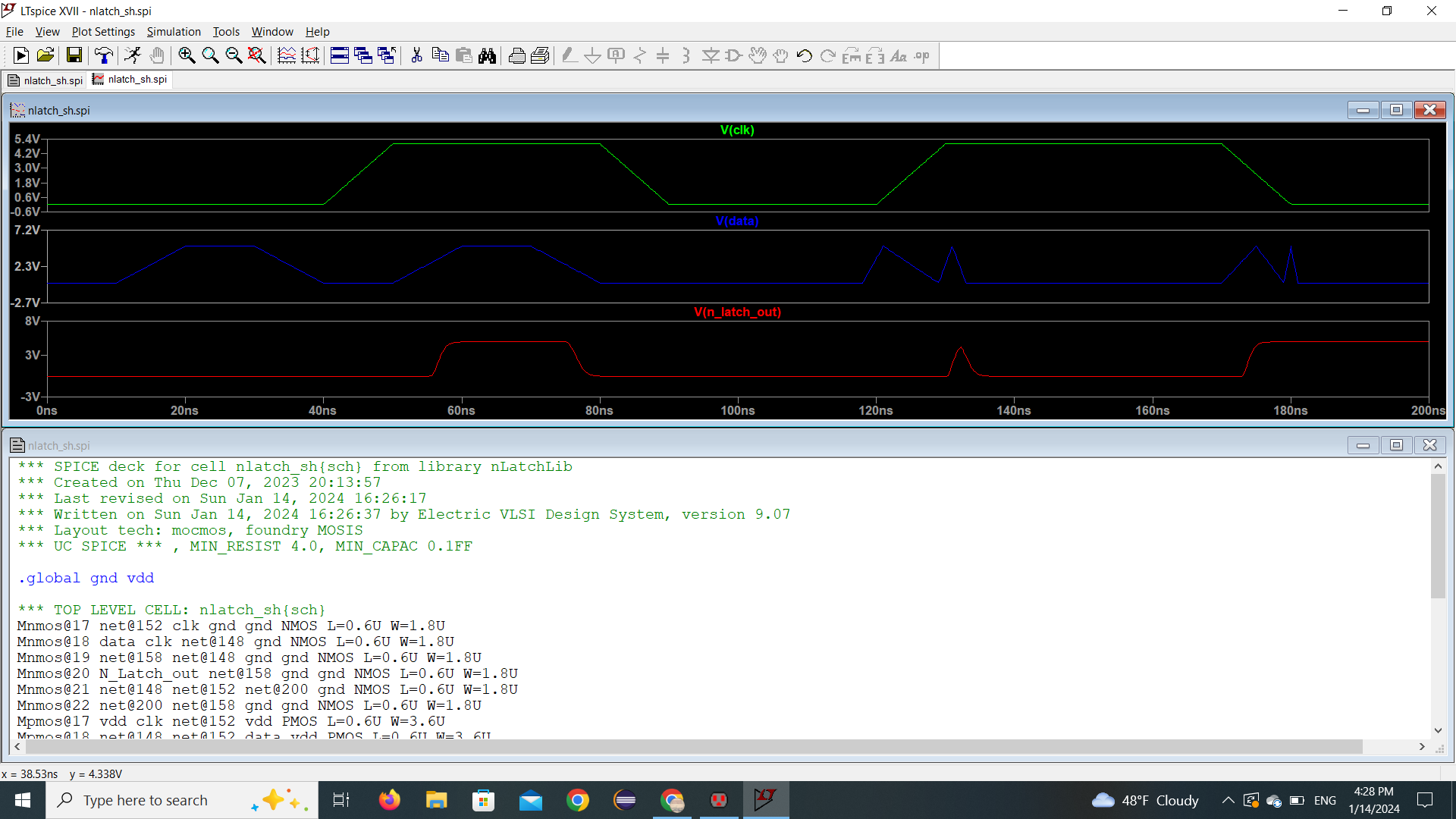
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**5.Layout**

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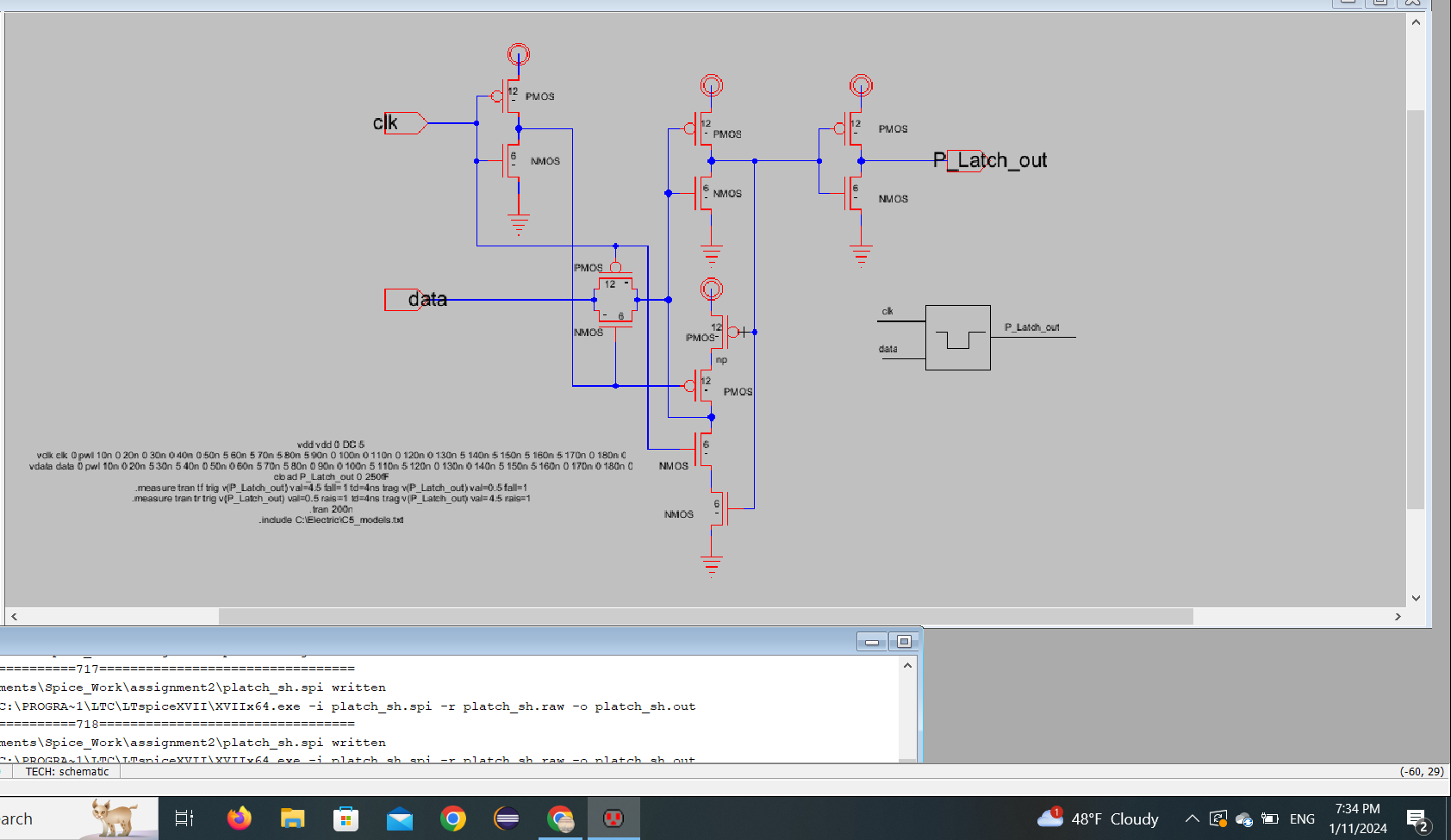
**Cases when simulation failed when missing setup/Hold windo**

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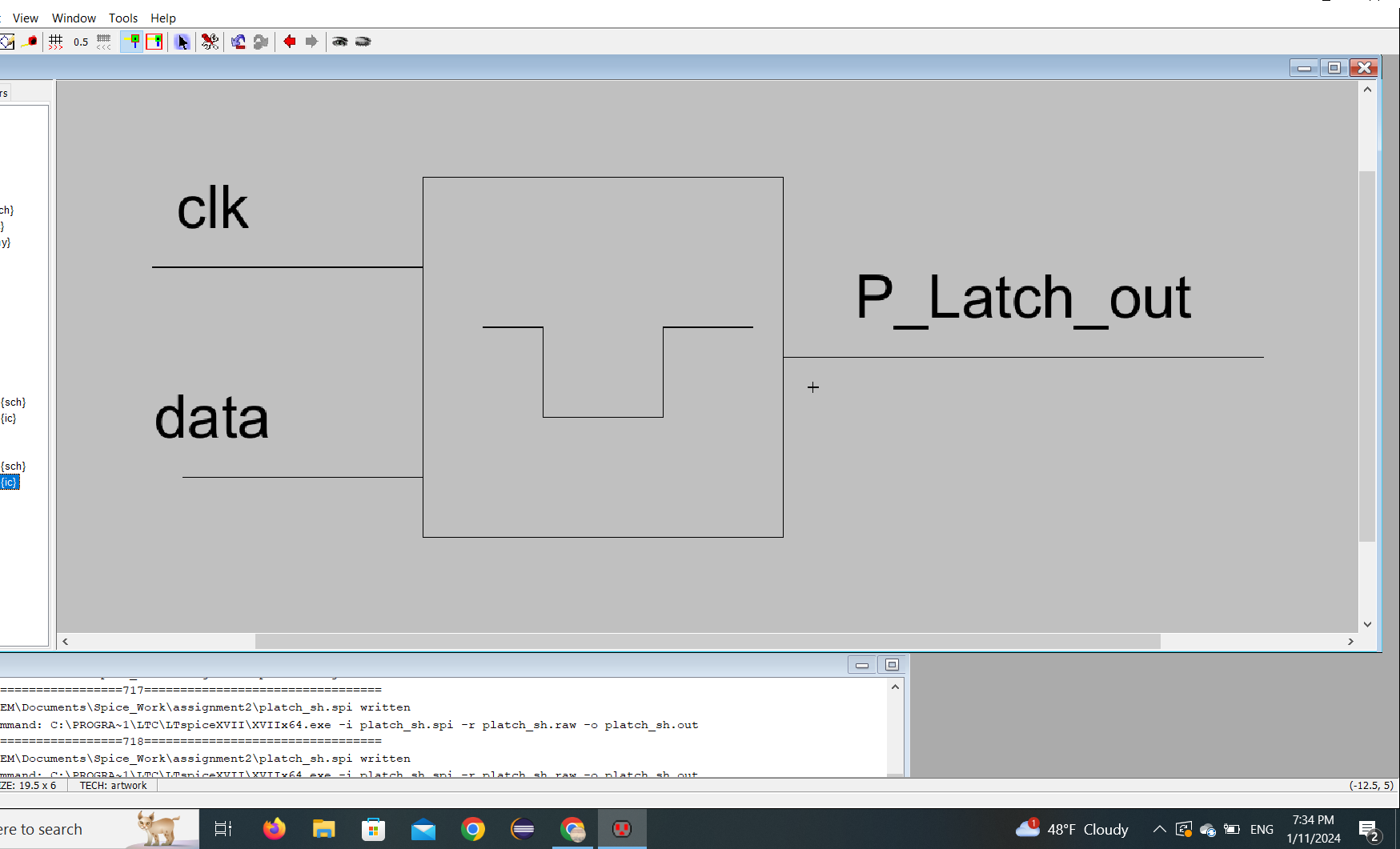
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**P-Latch**

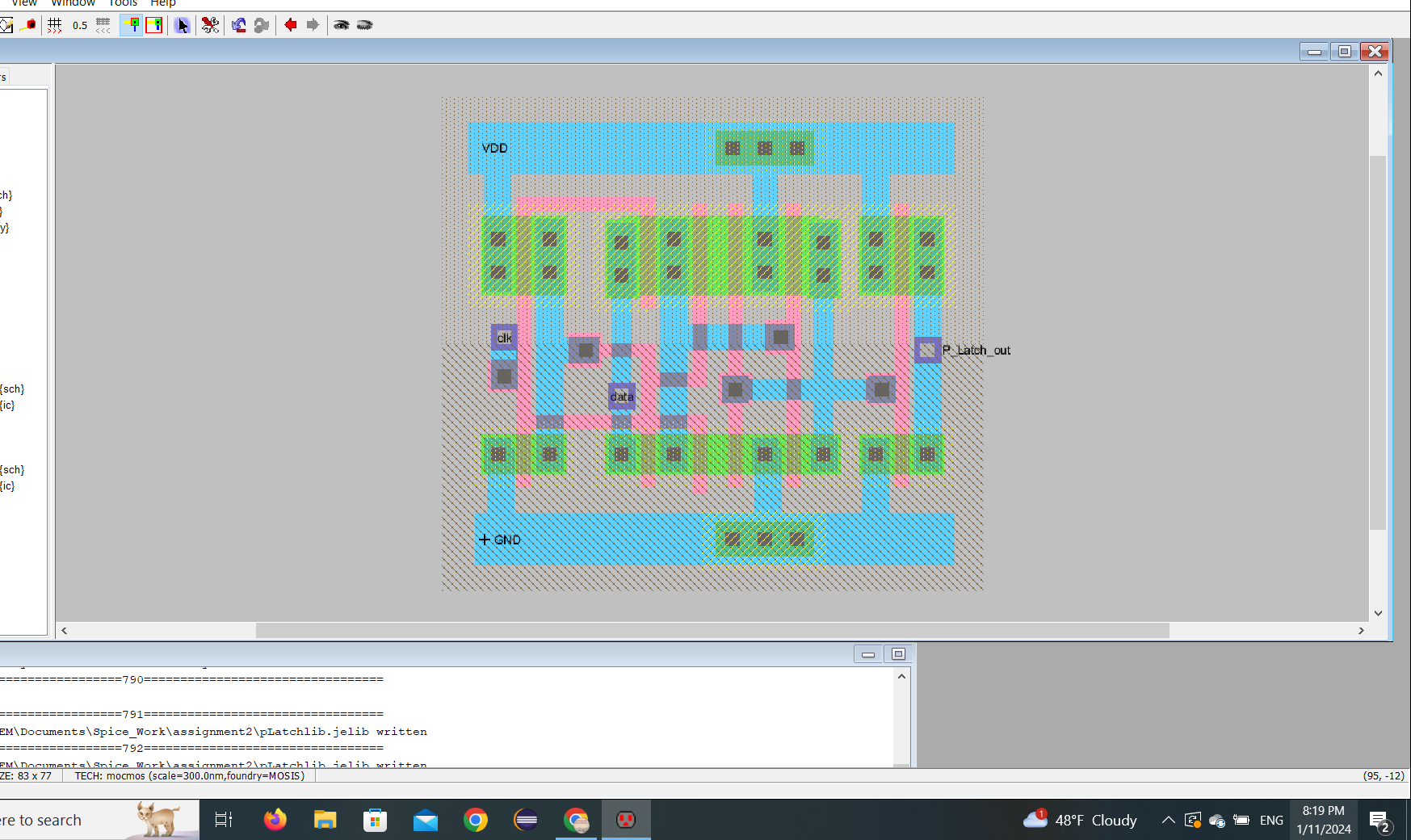
1. **Schematic view**

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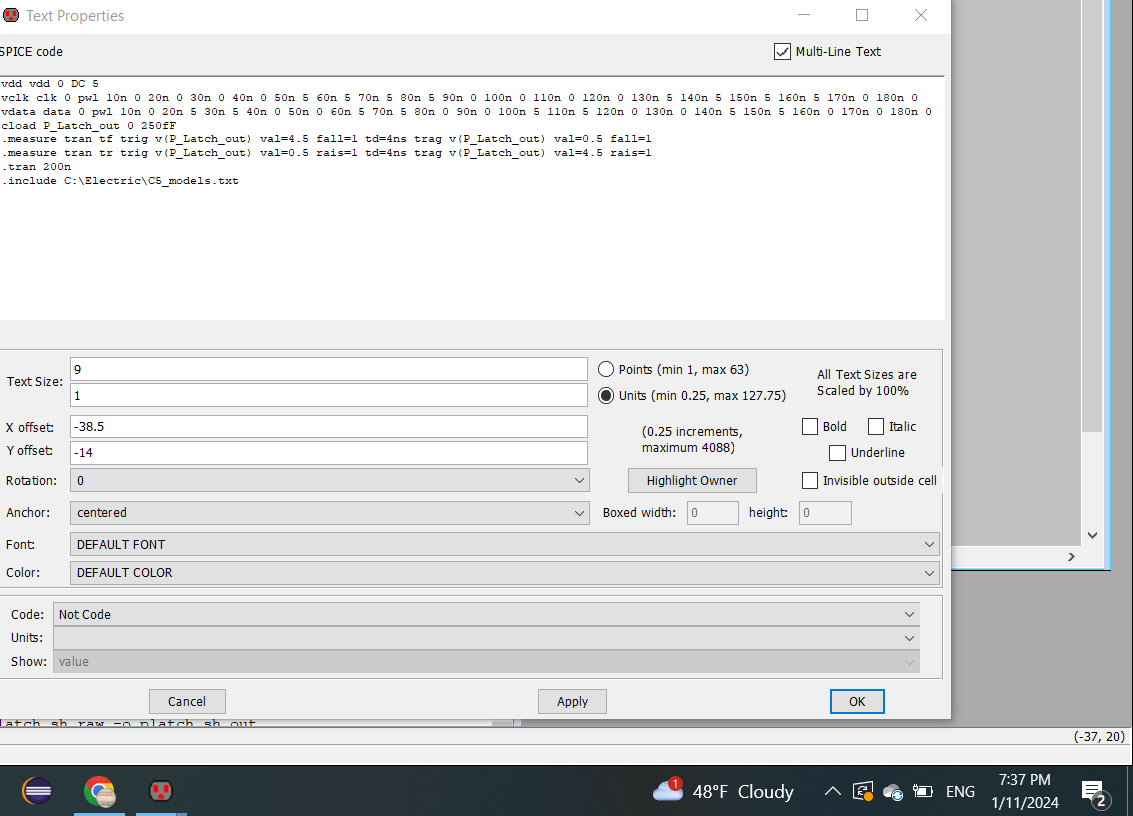
**2.Icon View**

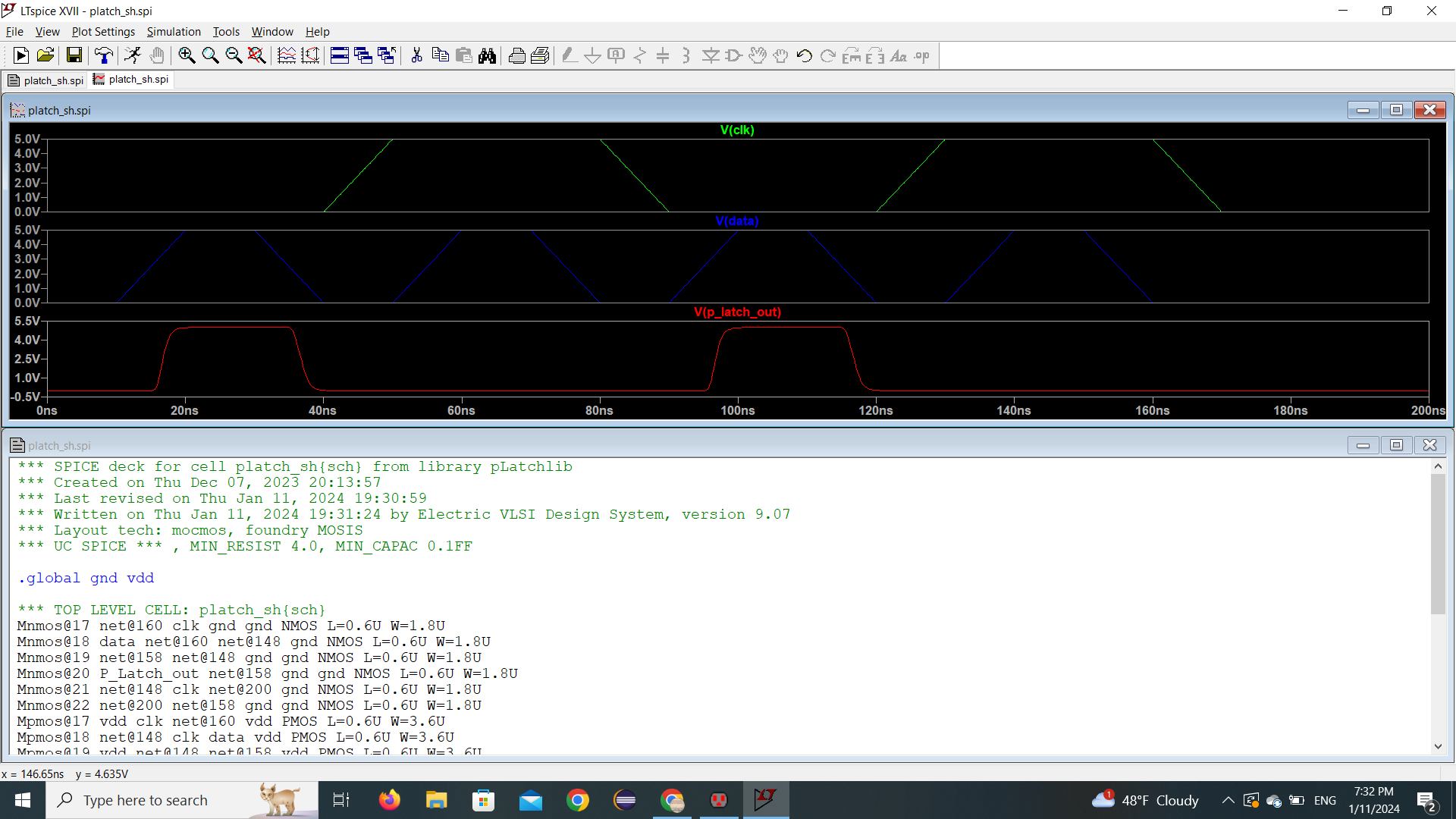
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**3.Layout view**

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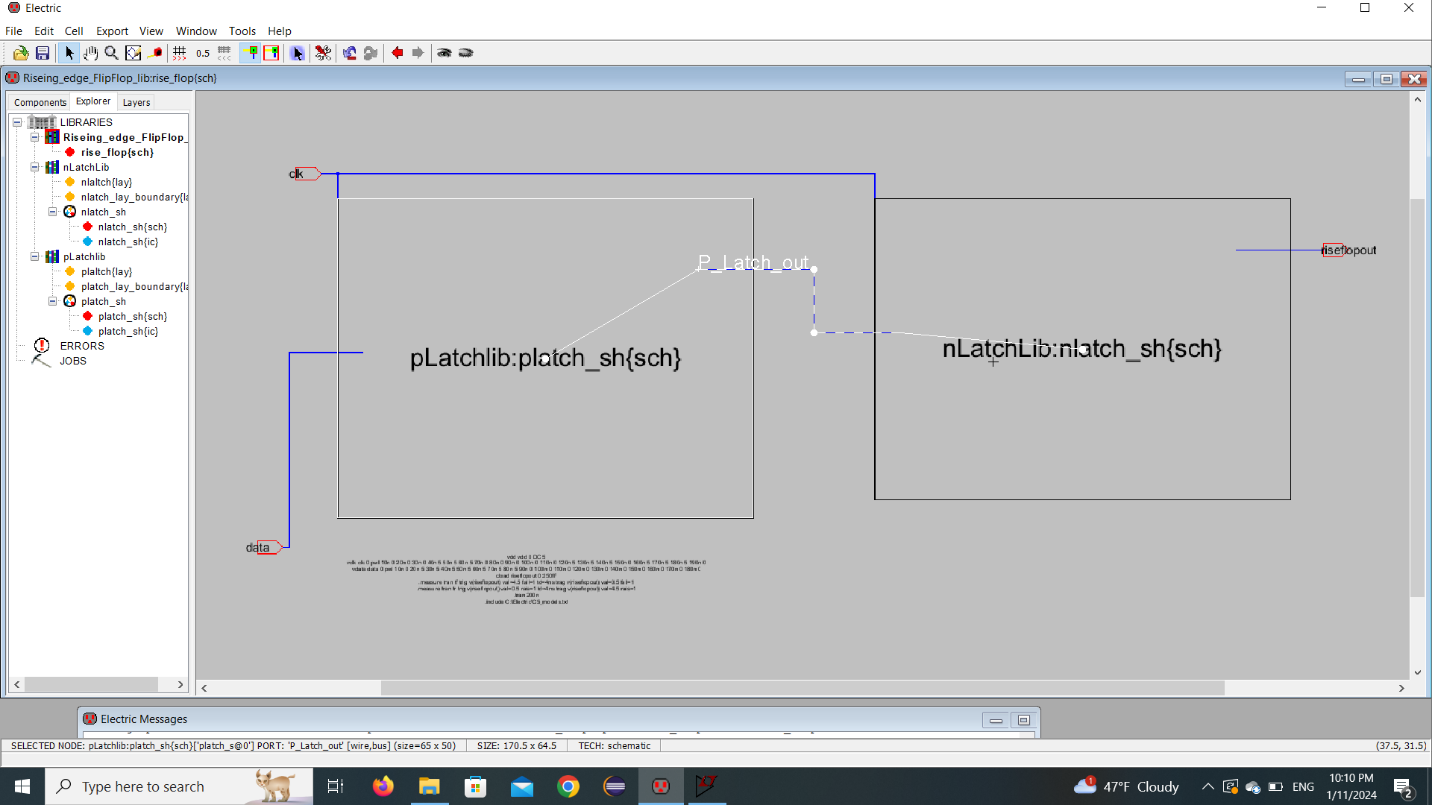
**4.Delay to out and clk to out as appears in the following figure.**

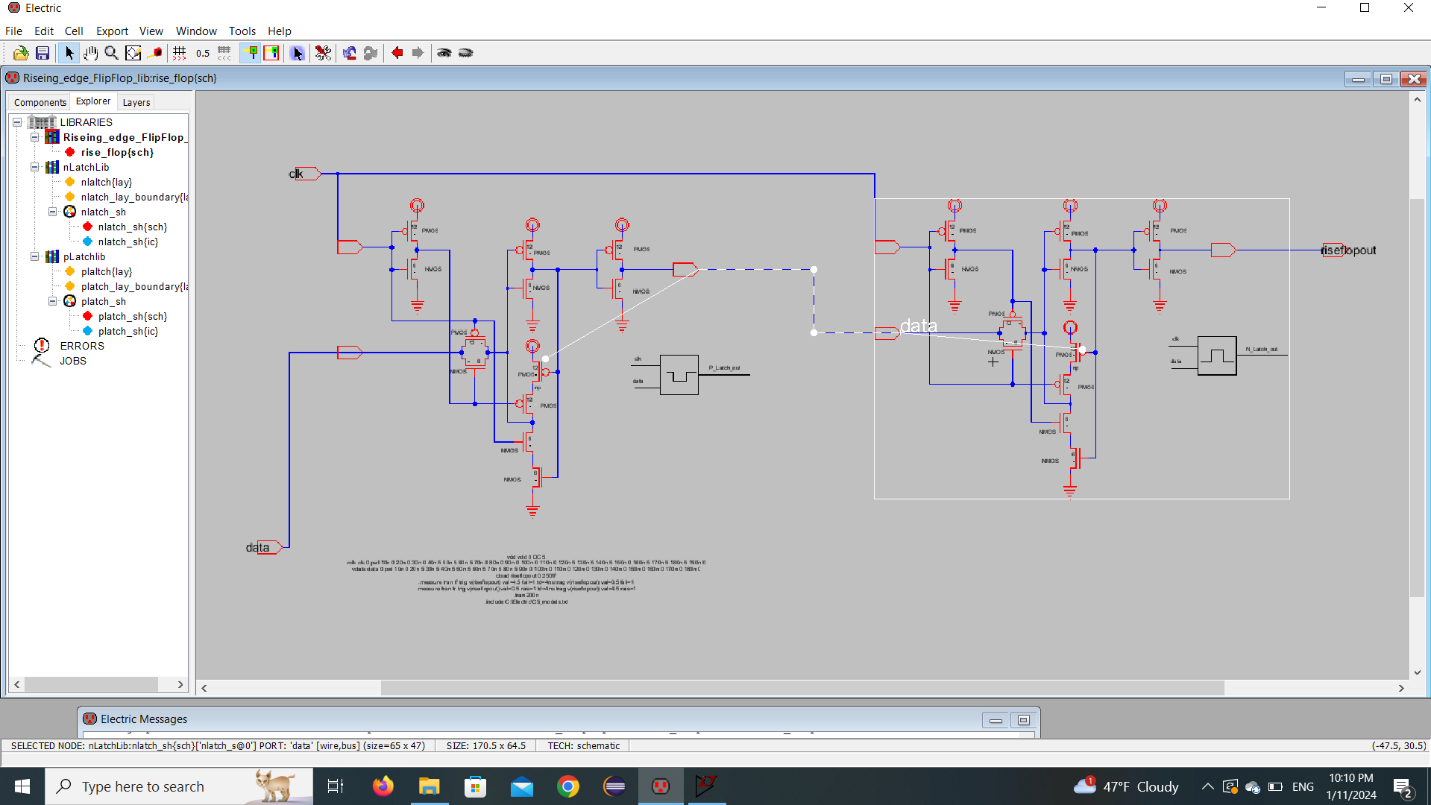
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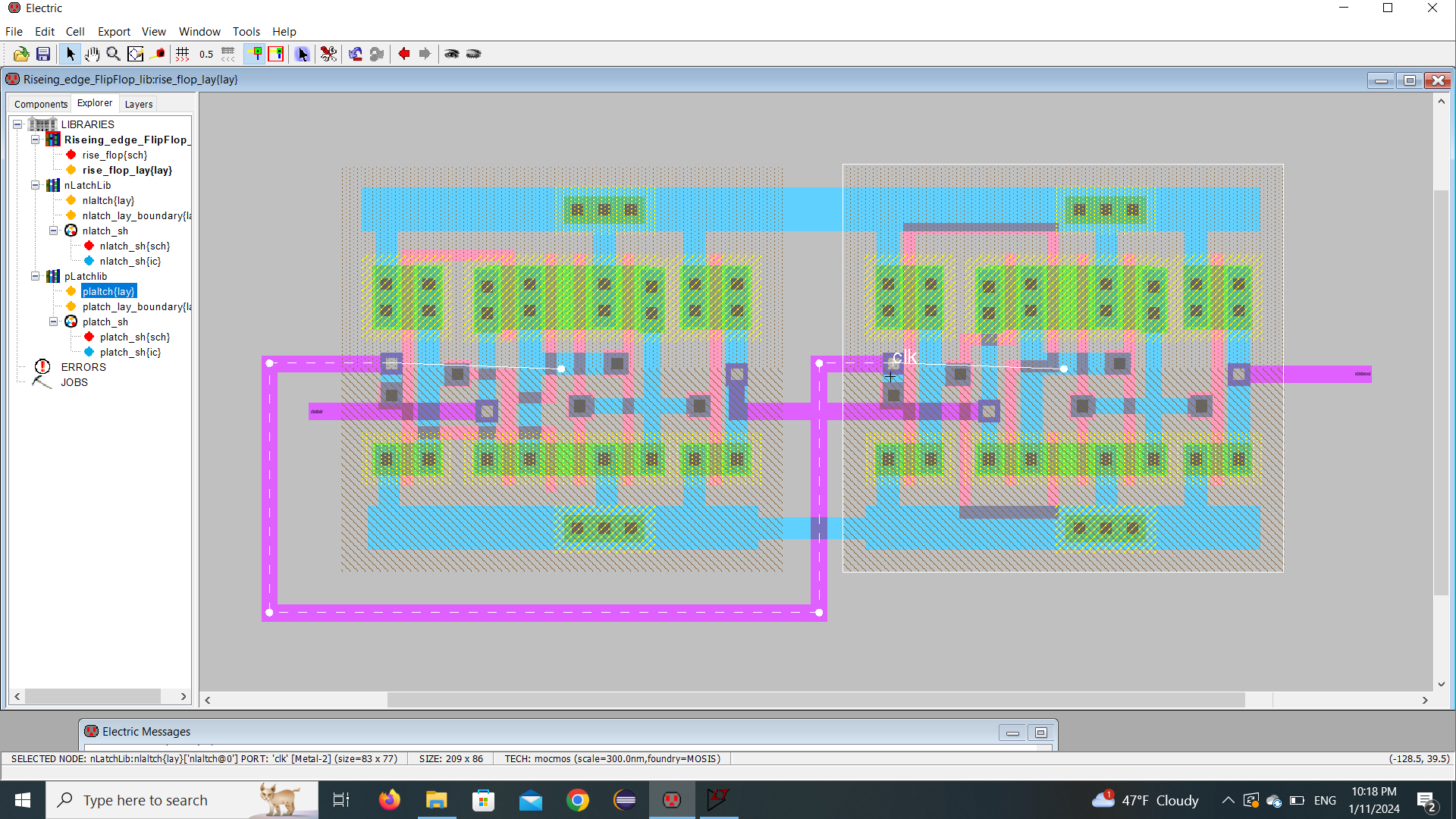
**Rising Edge\_FlipFlop**

1. **Schematic view**

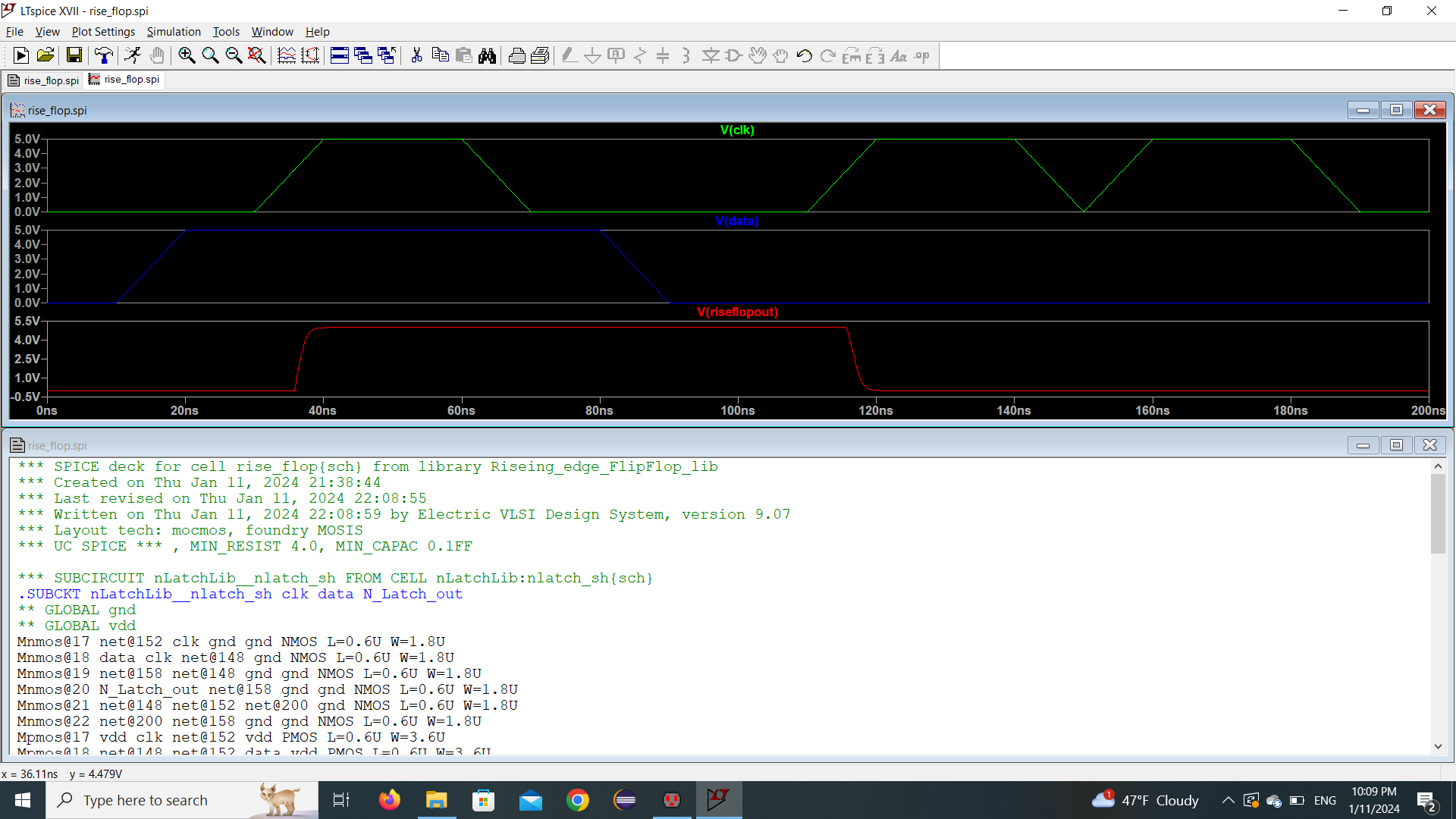
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**2.Layout**

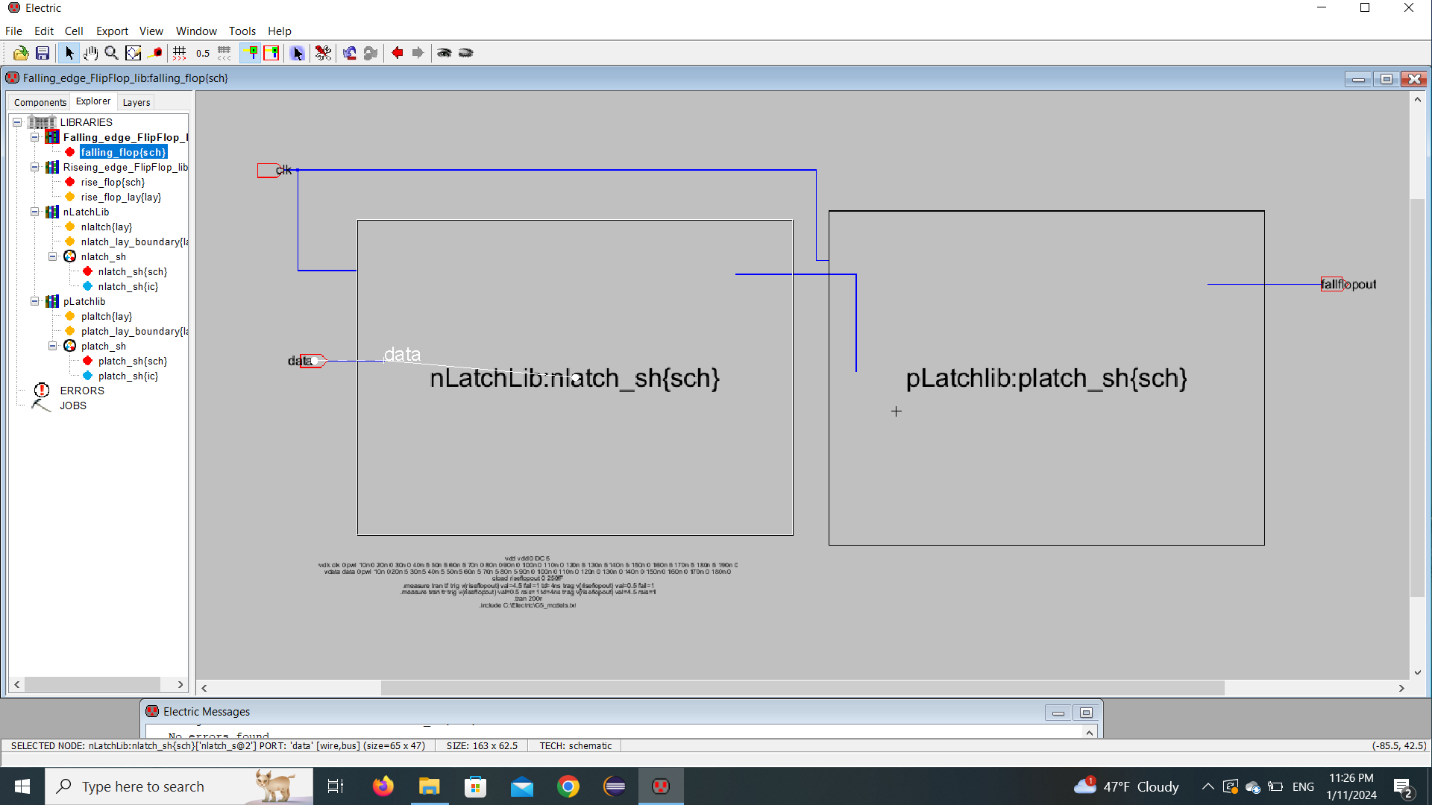
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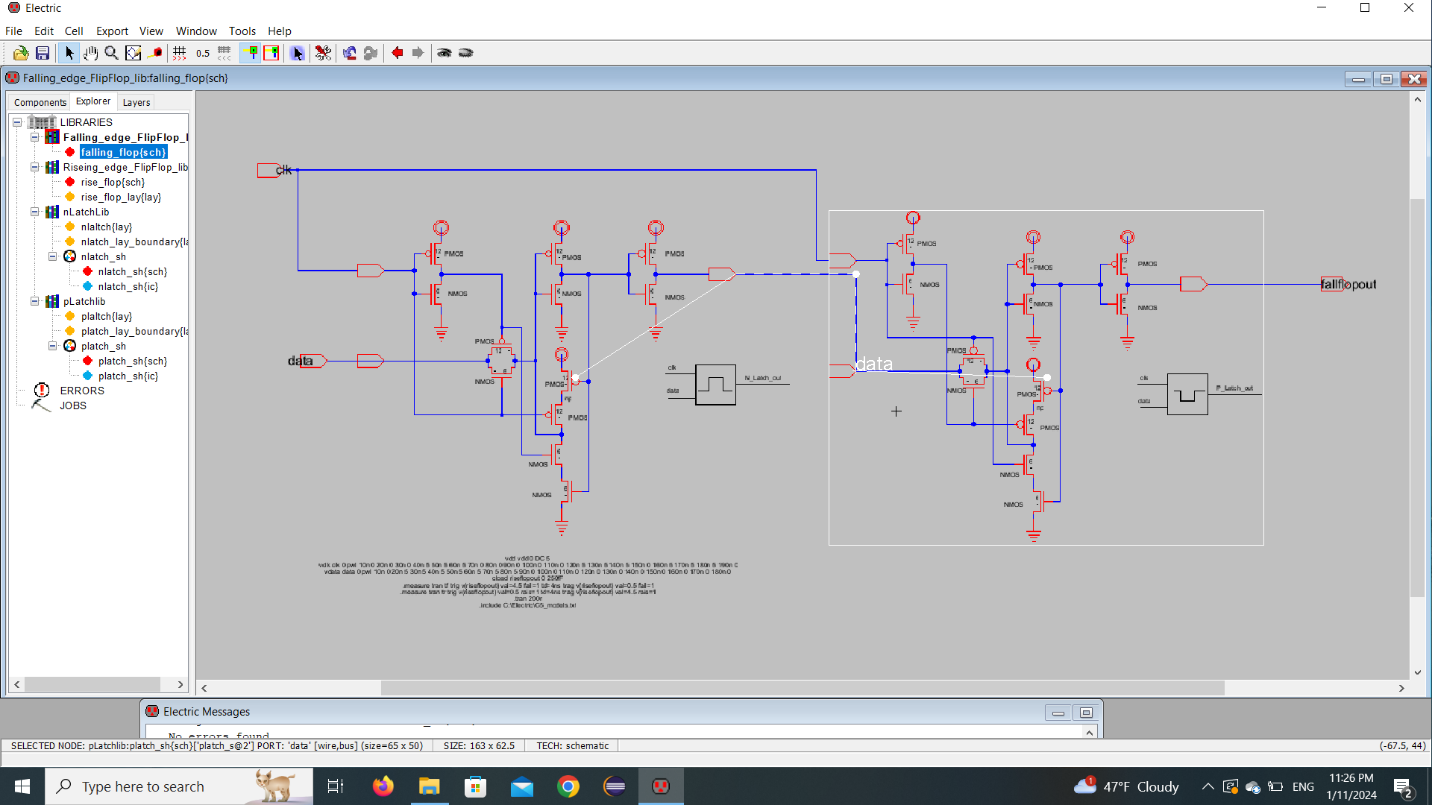
**3.Delay to out and clk to out as appears in the following figure.**

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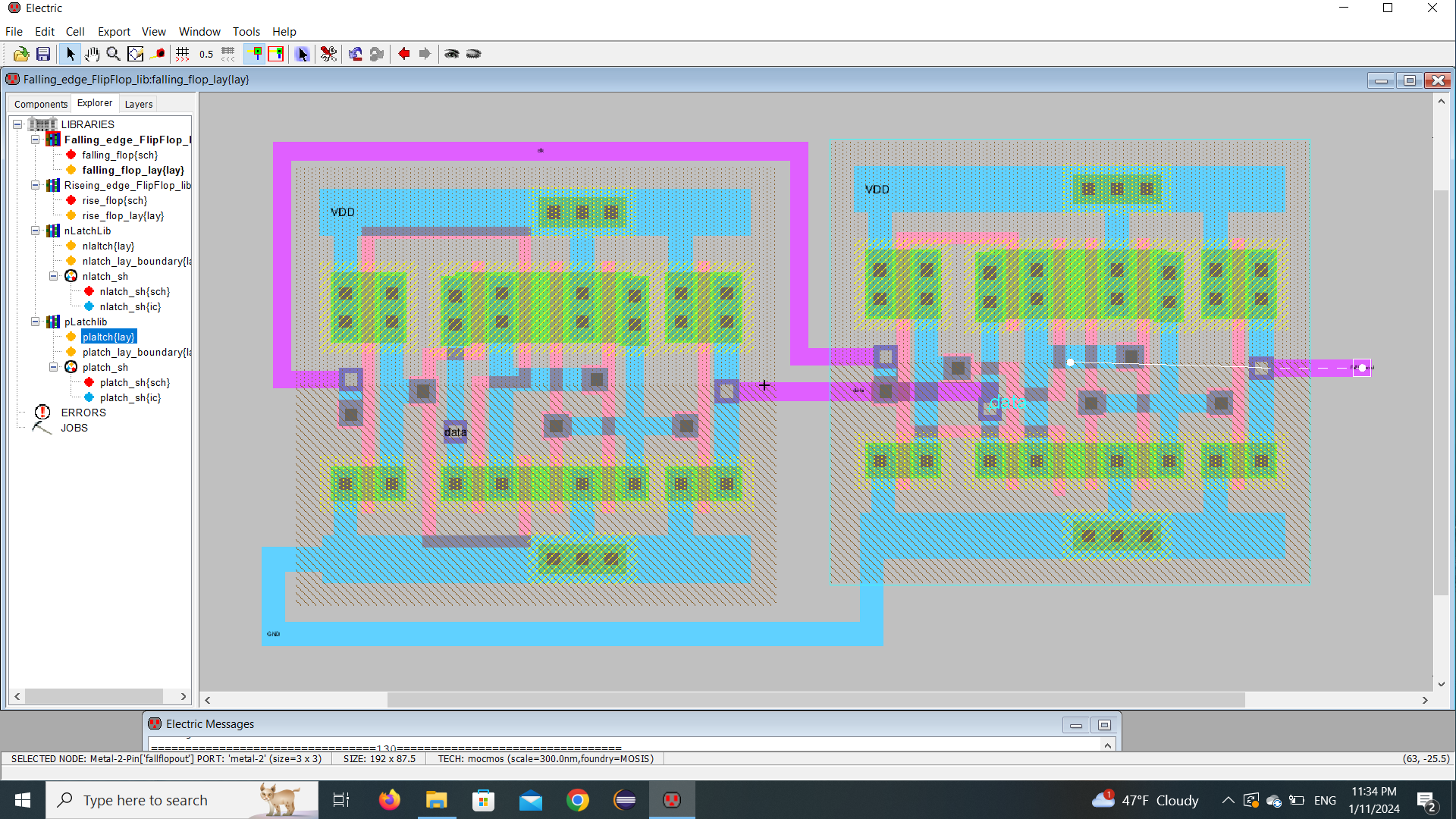
**Falling Edge Flip Flop**

1. **Schematic view**

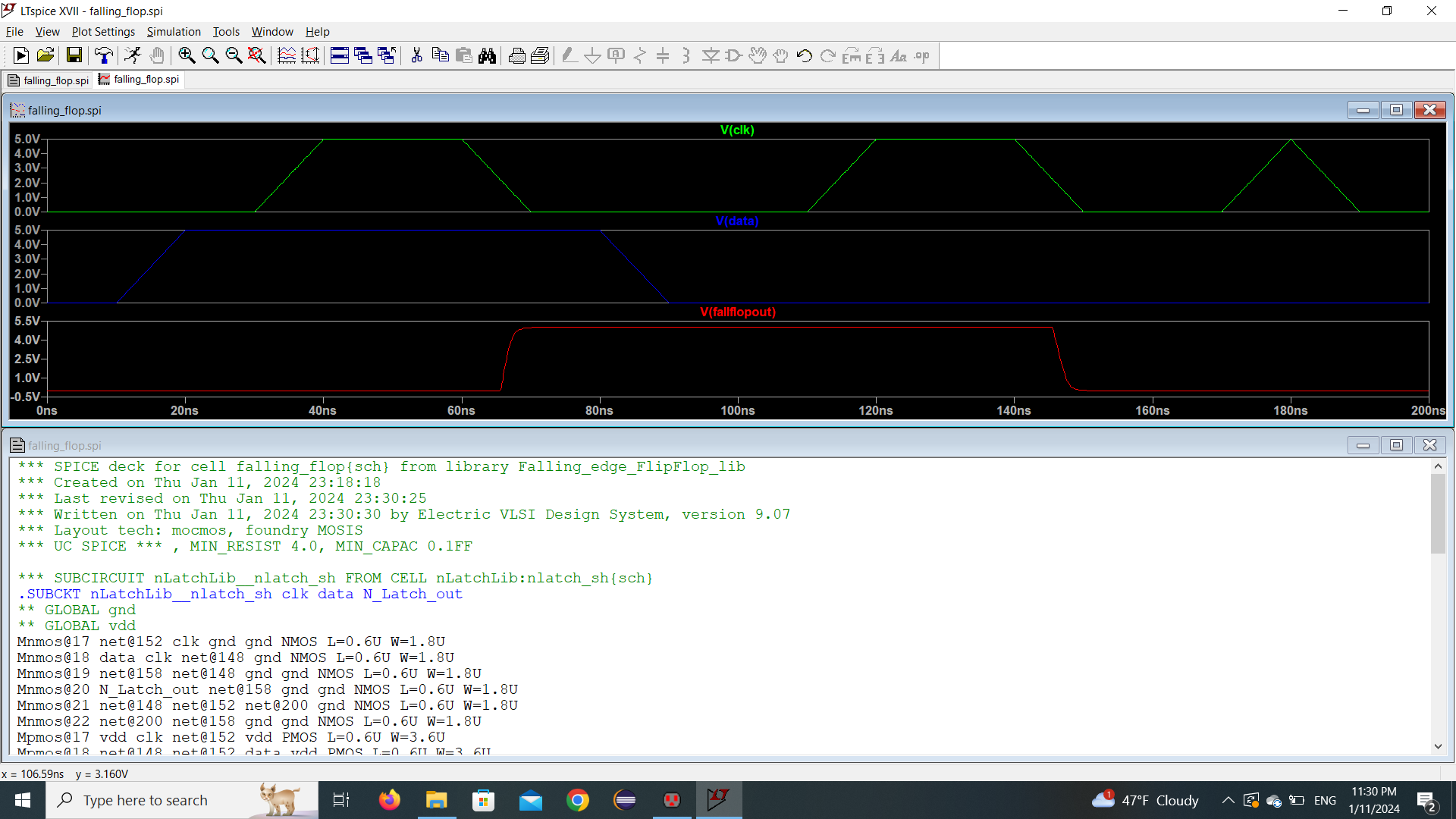
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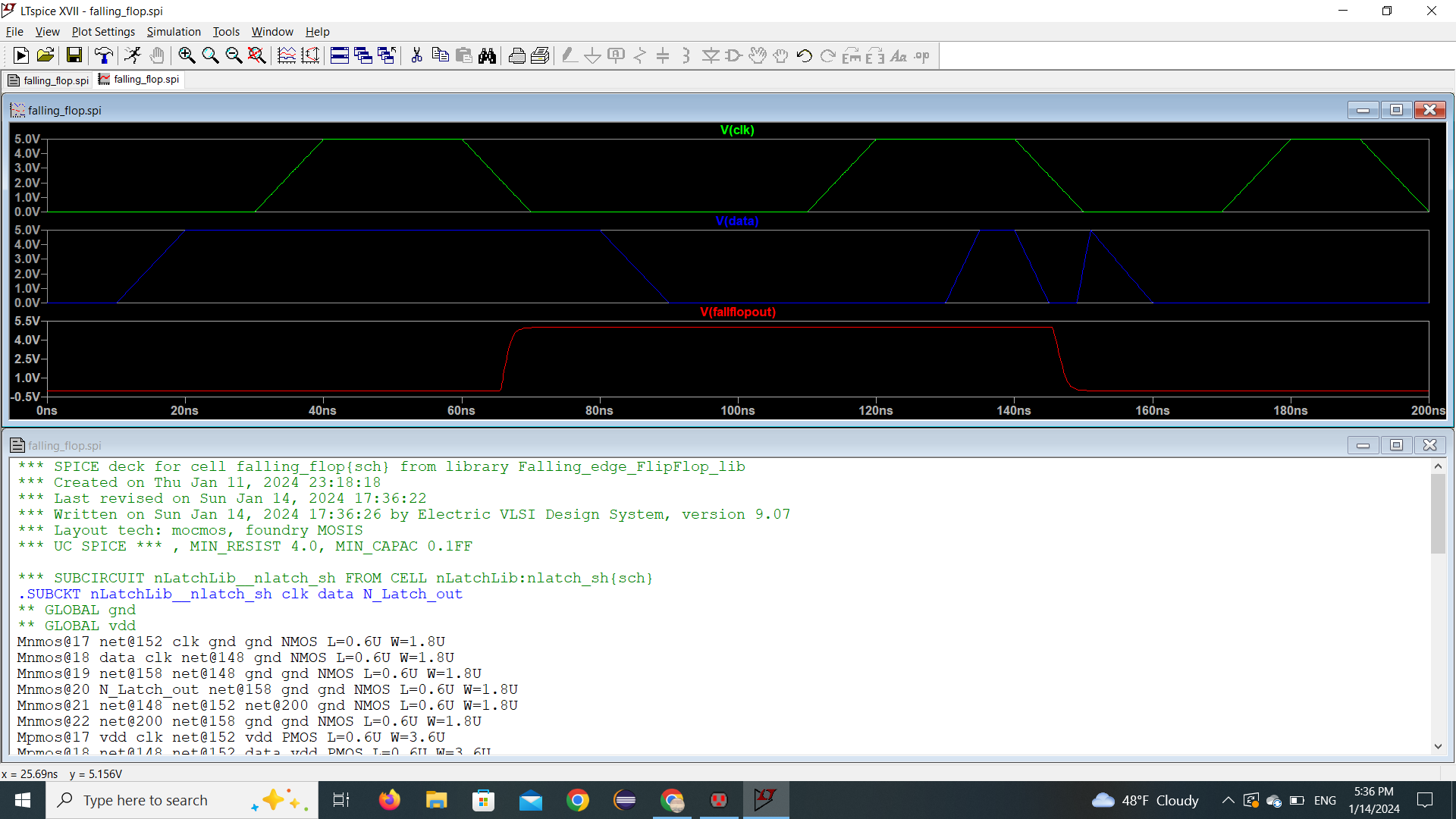
**2.Layout**

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**3.Delay to out and clk to out as appears in the following figure.**

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**4.Cases when simulation failed when missing setup/Hold windo**

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