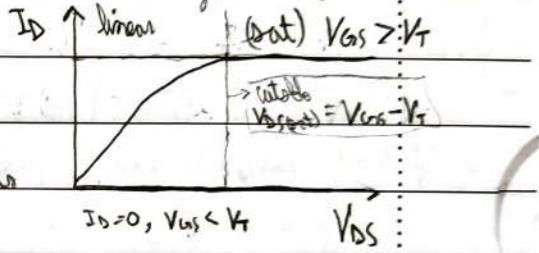
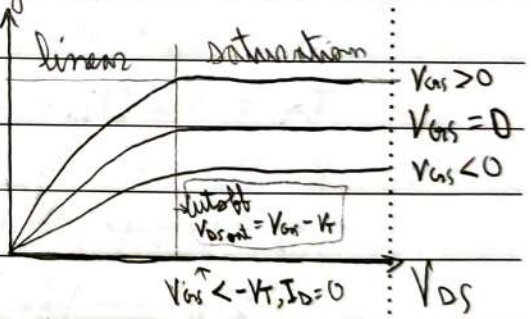
Subject Chapter 7: NMOS logic Date 24/4/2021 No.

* MOSFET: N-channel or P-channel
  - subcategory: enhancement or depletion (simplified to single letter)
    → NMOS: E-NMOS / D-NMOS | PMOS: E-PMOS / D-PMOS
- depletion type (D-NMOSFET) is normally on, whereas enhancement mode (E-NMOSFET) is normally off
- depletion type has a built in channel whereas enhancement type must create it
- the V_{GS} required to create the channel is called the threshold voltage (V_T) and is positive for E-NMOS and negative for D-NMOS.

E-NMOSFET IV characteristics

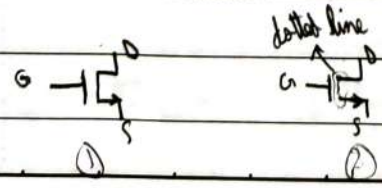


- for D-NMOS, the required V_{GS} to deplete the channel is the threshold voltage (V_T) and is negative
- an oxide separates the gate from the p-substrate (which separates the source and drain). The thickness of this oxide layer is (t_{ox}).

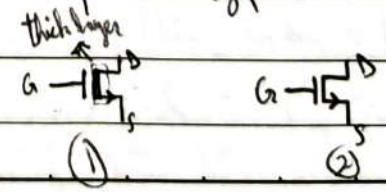


* symbols for enhancement type NMOSFET, and corresponding symbols for depletion type

enhancement type:



depletion type



① ② ① ②

either ① or ② will be consistently used.

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* three modes of operation of the NMOS:

1- cutoff:

$V_{GS} < V_{TN}$, $I_D = 0$ for enhancement: $V_{GS} > 0$

2- saturation:

$V_{GS} > V_{TN}$

$V_{DS} > V_{GS} - V_{TN}$

$I_D = k_n (V_{GS} - V_{TN})^2$

V_{TN}: threshold voltage

k_n: channel conduction parameter, $k_n = \frac{W}{L} \cdot \frac{\mu_n C_{ox}}{2}$

W & L: channel length and width, C_{ox}: capacitance of oxide per unit area

The main two parameters of a MOSFET are V_T & k_n

3- ohmic (linear):

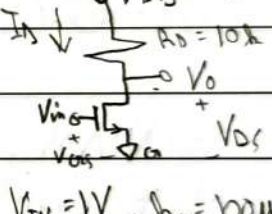
$V_{GS} > V_{TN}$

$V_{DS} \leq V_{GS} - V_{TN}$

$I_D = k_n [2(V_{GS} - V_{TN}) V_{DS} - V_{DS}^2]$

* NMOS inverter with resistive load:

R_D is the pulling network



$V_{TN} = 1V$, $k_n = 100 \mu A/V^2$

$R_D \cdot k_n = 1 V^{-1}$

$V_{GS} = V_{in}$ & $V_o = V_{DD} - I_D \cdot R_D$

+ if $V_{GS} < V_{TN}$: $I_D = 0$ & $V_o = V_{DD} = 5V$

+ if $V_{in} > V_{TN}$:

- assume sat then check assumption:

$I_D = k_n (V_{in} - V_{TN})^2$

$V_o = V_{DS} = V_{DD} - [k_n (V_{in} - V_{TN})^2] \cdot R_D > V_{in} - V_{TN}$ (for sat)

$\rightarrow V_o = V_{DS} = 5 - (V_{in} - 1)^2 > V_{in} - 1$

solving $V_{DD} - k_n R_D [V_{GS} - V_{TN}]^2 = V_{GS} - V_{TN}$

for $V_{GS} = V_{in} = V_S$

$\rightarrow$

$$V_S = V_{TN} - \frac{1}{2 k_n R_D} \pm \sqrt{\left(\frac{1}{2 k_n R_D}\right)^2 + \frac{V_{DD}}{k_n R_D}}$$

$\rightarrow V_S = 2.79 V$

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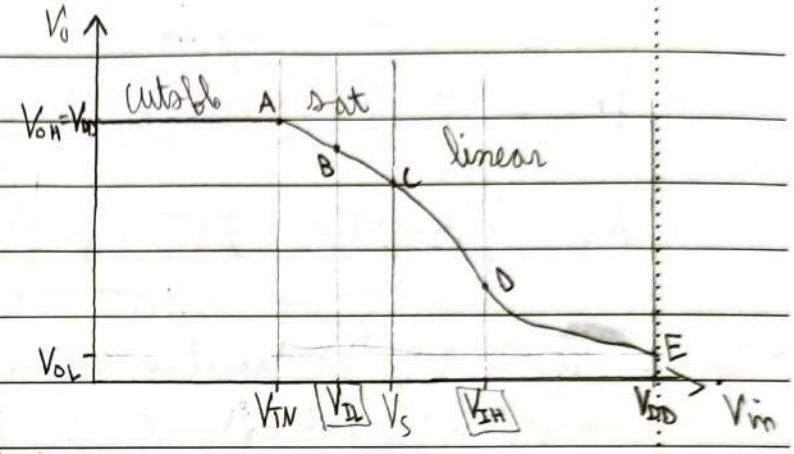
- assume linear:

$$I_D = k_n \left[2 (V_{GS} - V_{TN}) V_{DS} - V_{DS}^2 \right]$$

$$\rightarrow V_o = V_{DD} - R_D k_n \left[2 (V_{GS} - V_{TN}) V_{DS} - V_{DS}^2 \right]$$

$$\therefore V_o = 5 - \left[2 (V_{GS} - 1) V_{DS} - V_{DS}^2 \right]$$



- point A: $V_{in} = V_{TN}$ and transistor leaves cutoff. (output voltage is high)
- point B: $\frac{dV_o}{dV_{in}} = -1$ (gain), here the input voltage is maximum low (any voltage level below is low);
- point C: The device leaves sat and enters linear mode
- point D: $\frac{dV_o}{dV_{in}} = -1$, voltages larger than V_{in} at this point will be high
- point E: the output at this point is low, $V_{input} = V_{DD} = V_{OH}$

+ to calculate input voltage low (V_{IL}):

$$\frac{dV_o}{dV_{in}} = -1 = -2 R_D k_n (V_{in} - V_T)$$

$$\rightarrow \boxed{V_{in} = \frac{1}{2 R_D k_n} + V_{TN}}$$

$$\wedge \boxed{V_o = V_{DD} - \frac{1}{4 R_D k_n}}$$

+ to calculate input voltage high (V_{IH}):

V_o at D: $V_o = \sqrt{\frac{V_{DD}}{3 R_D k_n}}$

$$\rightarrow V_{IH} = \frac{2}{\sqrt{3}} \sqrt{V_{DD} \cdot R_D k_n + V_{TN} \cdot R_D k_n - \frac{1}{2}}$$

+ to calculate output voltage low (V_{OL}):

$$V_{OL} = \left[(V_{DD} - V_{TN}) + \frac{1}{2 R_D k_n} \right] \pm \sqrt{\left[(V_{DD} - V_{TN}) + \frac{1}{2 R_D k_n} \right]^2 - \frac{V_{DD}}{2 R_D}}$$

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∴ for a resistive load inverter:

$$V_{OH} = V_{DD}$$

$$V_{IL} = V_{TN} + \frac{1}{2R_D k_n}$$

$$V_{IH} = V_{TN} + 2\sqrt{\frac{V_{DD}}{3R_D k_n} - \frac{1}{2R_D k_n}}$$

$$V_{OL} = \left[V_{DD} - V_{TN} + \frac{1}{2R_D k_n}\right] \pm \sqrt{\left[V_{DD} - V_{TN} + \frac{1}{2R_D k_n}\right]^2 - \frac{V_{DD}}{R_D k_n}}$$

- the sharpness of the transition region increases with increasing R_D (as $R_D \cdot k_n$ increases)
- the minimum output voltage (the logic zero level) for a high input decreases with increasing R_D.
  (V_{OL} decreases as $R_D \cdot k_n$ increases)
- hence the inverter approaches ideal as R_D increases.
  (limit $R_D \cdot k_n \to \infty$)
- power dissipation: $P_D = \frac{V_{DD}}{2}\left[I_D(V_{in} = V_{OL}) + I_D(V_{in} = V_{OH})\right]$

for inverter with resistive load: $P_D = \left[\frac{V_{DD}}{2}\right] \cdot \left[\frac{V_{DD} - V_{OL}}{R_D}\right]$

* steps to solving:

1- check V_{GS}, if $V_{GS} > V_T$ then transistor on. else off.

2- check V_{DS}. if $V_{DS} > V_{GS} - V_T$, then saturated
   else if $V_{DS} < V_{GS} - V_T$, then linear active

3- if V_{DS} can't be checked first, assume one then check if assumption is correct.

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design example: $k_n = 150\ \mu A/V^2$, $V_{TN} = 0.5V$

(a) R_D for $V_o = 0.1V$ when $V_i = 3V$

∴ linear → $V_o = V_{DD} - R_D \cdot k_n [2(3-0.5)\cdot 0.1 - 0.1^2]$

→ $0.1 = 3 - R_D \cdot 150\mu [0.49]$ → $R_D = \frac{2.9}{7.35\times10^{-5}} = 39.5k\Omega$

(b) transition point: $V_o = V_S - V_{TN}$ sat

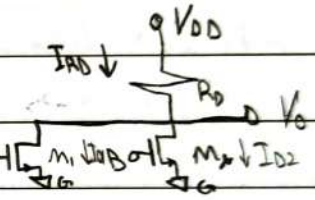
→ $V_{DD} - 39.5k \cdot 150\mu [V_S - \frac{1}{2}]^2 = V_S - \frac{1}{2}$

define: $x = V_S - \frac{1}{2}$ → $39.5k \cdot 150\mu \cdot x^2 + x - V_{DD} = 0$

→ $x = 0.63217$ or -0.8809

→ $V_S = 1.13217\ V$

* NMOS NOR with resistive load:



- transistors do not saturate

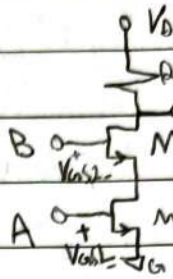
A	B	V_o	M_1	M_2	V_o logic	
0	0	V_{DD}	off	off	1	$V_o = V_{DD} - I_{RD} R_D$
0	1	V_{DS1}	off	linear	0	$V_o = V_{DS1} = V_{DS2}$
1	0	V_{DS2}	linear	off	0	
1	1	$V_{DS1,2}$	linear	linear	0	

∴ $I_{D1} = k_{n1} V_{DS1} [2(V_{GS1} - V_{T1}) - V_{DS1}]$ ∧ $I_{RD} = \frac{V_{DD} - V_o}{R_D} = I_{D1} + I_{D2}$

for A=B, $I_{D1} = I_{D2}$ → $I_{RD} = m \cdot I_{D1}$, m: number of transistors (here m = 2)

→ $\frac{V_{DD} - V_o}{R_D} = m k_n V_o [2(A - V_{T1}) - V_o]$, ∴ A = voltage input at A

* NMOS NAND with resistive load:



A	B	V_o (logic)	V_o (V)	M_1	M_2
0	0	1	V_{DD}	off	off
0	1	1	V_{DD}	off	linear
1	0	1	V_{DD}	linear	off
1	1	0	$V_{DS1}+V_{DS2}$	linear	linear

$V_o = V_{DD} - I_{RD} \cdot R_D = V_{DS2} + V_{DS1}$

$\therefore I_{D1} = k_{n1} V_{DS1}\left[2(V_{GS1} - V_{T1}) - V_{DS1}\right]$ $\wedge$ $I_{RD} = \dfrac{V_{DD} - V_o}{R_D} = I_{D1} = I_{D2}$

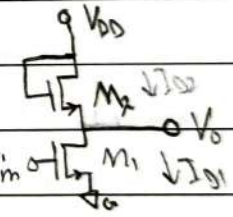
$\wedge I_{D2} = k_{n2} V_{DS2}\left[2(V_{GS2} - V_{T2}) - V_{DS2}\right]$

if $V_{GS1} = A$ $\wedge$ $V_{GS2} = B - V_{DS1}$

$\rightarrow \dfrac{V_{DD} - (V_{DS1} + V_{DS2})}{R_D} = k_{n1} V_{DS1}\left[2(A - V_{T1}) - V_{DS1}\right]$

$= k_{n2} V_{DS2}\left[2(B - V_{DS1} - V_{T2}) - V_{DS2}\right]$

* NMOS inverter with active load



$\therefore V_{DS2} = V_{GS2} \rightarrow V_{GS2} - V_T < V_{DS2}$

$\rightarrow M_2$ is always saturated regardless of M_1

* Cases:

1- $V_{in} < V_T \rightarrow M_1$ is off $\wedge$ I_{D1} is zero:

$I_{D1} = I_{D2} = 0 \rightarrow k_{n2}(V_{GS2} - V_{TN2})^2 = 0 \rightarrow V_{GS2} = V_{TN2}$

$\therefore V_o = V_{DD} - V_{GS2} = V_{DD} - V_{TN2}$

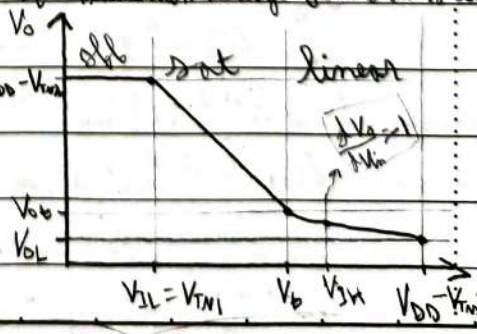
2- $V_{TN1} < V_{in} < V_t \rightarrow M_1$ is sat., V_t: transition voltage from sat to linear

$I_{D1} = k_{n1}(V_{GS1} - V_{TN1})^2 = k_{n1}(V_{in} - V_{TN1})^2$

$V_{GS2} = V_{DD} - V_{DS1} = V_{DD} - V_o$

$I_{D2} = k_{n2}\left[V_{GS2} - V_{TN2}\right]^2 = k_{n2}\left[V_{DD} - V_o - V_{TN2}\right]^2$

$\therefore I_{D1} = I_{D2} \rightarrow k_{n2}(V_{DD} - V_o - V_{TN2})^2 = k_{n1}(V_{in} - V_{TN1})$



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$\therefore V_o = V_{DD} - V_{TN2} - \sqrt{\frac{k_{n1}}{k_{n2}}}\cdot(V_{in} - V_{TN}) \rightarrow V_{TL} = V_{TN1}$

3- $V_{in} = V_t \rightarrow M_1$ saturated / ohmic (edge)

$V_{DS1} = V_{GS1} - V_{TN1} \rightarrow V_{ot} = V_t - V_{T1}$ & $I_{D1} = I_{D2}$

$k_{n1}(V_{GS1} - V_{T1})^2 = k_{n2}(V_{GS2} - V_{TN2})^2$

$\rightarrow k_{n1}(V_t - V_{T1})^2 = k_{n2}(V_{DD} - V_{ot} - V_{T2})^2 = k_{n2}(V_{DD} - V_t + V_{T1} - V_{T2})^2$

4- $V_{in} > V_t \rightarrow M$ is ohmic:

$I_{D1} = k_{n1} V_{DS1}[2(V_{GS1} - V_{T1}) - V_{DS1}]$, $V_o = V_{DS1}$, $V_{GS1} = V_{in}$

& $V_{GS2} = V_{DD} - V_o$

$\because I_{D1} = I_{D2}$ & $I_{D2} = k_{n2}(V_{GS2} - V_{T2})^2$

$\rightarrow k_{n1} V_{DS1}[2(V_{GS1} - V_{T1}) - V_{DS1}] = k_{n2}(V_{GS2} - V_{T2})^2$

- in this region, V_{TH} can be found by taking the derivative of the above equation: $\frac{dV_o}{dV_{in}} = -1$

- taking the second case and solving for V_t:

$$V_t = \frac{\sqrt{\frac{k_{n1}}{k_{n2}}}\cdot V_T + V_{DD}}{1 + \sqrt{k_{n1}/k_{n2}}}$$, define $k_R = \frac{k_{n1}}{k_{n2}}$

$$\rightarrow V_t = \frac{\sqrt{k_R}\cdot V_T + V_{DD}}{1 + \sqrt{k_R}}$$, k_R should be large

$\because k_{n1} = \frac{W_1}{L_1}\frac{\mu_n C_{ox}}{2}$ & $k_{n2} = \frac{W_2}{L_2}\frac{\mu_n C_{ox}}{2}$, $\frac{\mu_n C_{ox}}{2}$ is usually constant

$\therefore k_R = \left(\frac{W_1/L_1}{W_2/L_2}\right)$, ratio of the aspect ratios of the transistors

$\rightarrow M_1$ should be wide and M_2 narrow

example: $V_T = 1V$, $k_{n1} = 10^{-3}$ A/V², $k_{n2} = 0.34\times10^{-3}$ A/V², $V_{DD} = 5V$

1) $V_t = \frac{\sqrt{k_R}\cdot V_T + V_{DD}}{1 + \sqrt{k_R}}$ & $\sqrt{k_R} = 1.715 \rightarrow V_t = 2.493V$

$V_{ot} = V_t - V_T = 1.493V$

2) for $V_{in} = V_{DD} - V_T = 4V$, ohmic $\rightarrow V_o[2(3) - V_o] = \frac{k_{n2}}{k_{n1}}(5 - V_o - 1)^2$

$\rightarrow \frac{k_{n1} + k_{n2}}{k_{n1}}V_o^2 - \frac{6k_{n1} + 8k_{n2}}{k_{n1}}\cdot V_o + \frac{k_{n2}}{k_{n1}}16 = 0$

$\rightarrow$ **$V_o = 0.6989V$** or 5.8089 out of range

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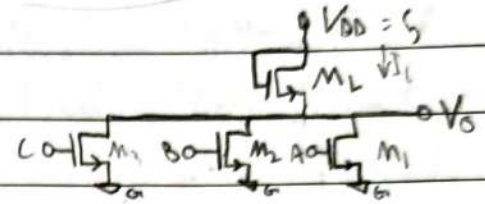
- note on previous example: maximum output voltage of the circuit is $V_{DD} - V_T$, hence the high input corresponding to V_{OL} is $V_{in} = V_{DD} - V_T$

* NMOS NOR gate:

A	B	C	V_{out}	
0	0	0	1	$V_{DD} - V_T$
0	0	1	0	
0	1	0	0	
1	1	1	0	



$\therefore I_D = k_{n1} V_{DS1} [2(V_{GS1} - V_{T1}) - V_{DS1}]$

$I_L = k_{nL} (V_{GSL} - V_{TL})^2$, $I_L = m I_{D1}$

$\therefore k_{nL} (V_{GSL} - V_{TL})^2 = m k_{n1} V_{DS1} [2(V_{GS1} - V_T) - V_{DS1}]$

- Worst case when $m = 1$ (one transistor), hence $V_{OL} < V_T$ always

example: $V_T = 1V$, $k_{n1} = 10^{-3}\ A/V^2$, $k_{nL} = 0.34 \times 10^{-3}\ A/V^2$

$\rightarrow k_R = \frac{10^{-3}}{0.34 \cdot 10^{-3}} = 2.94$

1) V_{OL} if $A = B = C = 4V$

$k_{nL} (V_{GSL} - V_{TL})^2 = 3 \cdot k_{n1} \cdot V_{OL} [2(4-1) - V_{OL}]$

$\rightarrow (5 - V_{OL} - 1)^2 = 3 \cdot 2.94 \cdot V_{OL} [6 - V_{OL}]$

$\rightarrow 16 - 8V_{OL} + V_{OL}^2 = 8.82 \cdot [6V_{OL} - V_{OL}^2]$

$\rightarrow 9.92 \cdot V_{OL}^2 - 60.92 V_{OL} + 16 = 0 \rightarrow V_{OL} = 0.295\ V$

2) $m = 1 \rightarrow 16 - 8V_{OL} + V_{OL}^2 = 2.94 [6V_{OL} - V_{OL}^2]$

$\rightarrow 3.94 V_{OL}^2 - 25.64 V_{OL} + 16 = 0 \rightarrow V_{OL} = 0.699\ V$

- hence, one active gate gives the highest output voltage

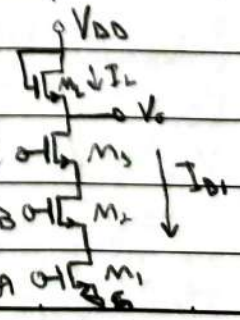
* NMOS NAND gate:

- if any input is low then $V_o = V_{DD} - V_T$
- if all inputs high then output: low logic

all transistors will be ohmic, $V_o = V_{DS1} + V_{DS2} + V_{DS3}$

$V_{GS1} = A = V_{DD} - V_T$, $V_{GS2} = V_{DD} - V_T - V_{DS1}$

$V_{GS3} = V_{DD} - V_T - V_{DS1} - V_{DS2}$



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example: $k_1 = k_{n1} = k_2 = k_n = 2\times10^{-3}\ A/V^2$, $V_{T1} = V_{T2} = V_{T3} = 1V$

$I_D = 1mA$, $V_{DD} = 5V$

1) $V_{OL} = V_{DS3} + V_{DS2} + V_{DS1}$

$\because V_{GS1} = 5 - 1 = 4V$

ohmic $\rightarrow I_D = k_n \cdot V_{DS1}[2(V_{GS1} - V_T) - V_{DS1}] = 1mA$

$\Rightarrow 0.5 = 6V_{DS1} - V_{DS1}^2 \rightarrow V_{DS1} = 84.52\ mV$

$\because V_B = V_{DD} - V_T \rightarrow V_{GS2} = V_B - V_{DS1} = 3.9155V$

$\therefore I_D = k_n V_{DS2}[2(V_{GS2} - V_T) - V_{DS2}] \rightarrow -V_{DS2}^2 + 5.831 V_{DS2} - 0.5 = 0$

$\rightarrow V_{DS2} = 89.054\ mV$

$\because V_C = V_{DD} - V_T \rightarrow V_{GS3} = V_C - V_{DS1} - V_{DS2} = 3.8284V$

$\rightarrow -V_{DS3}^2 + 5.65686 V_{DS3} - 0.5 = 0 \rightarrow V_{DS3} = 89.81\ mV$

$\therefore V_{OL} = 89.81 + 89.05 + 84.52 = \boxed{0.2614\ V}$

2) $\because$ load always saturated: $I_D = k_L(V_{GSL} - V_T)^2$

$V_{GSL} = V_{DD} - V_T - V_{OL} = 3.739V \rightarrow k_L = 71.55\mu A/V^2$

$k_3\ k_2\ k_1\ k_0$ 1001

$k_3\ k_2\ k_1\ k_0$ 0011

1100

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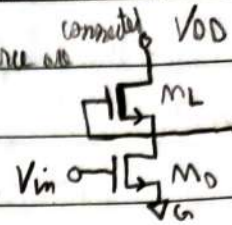
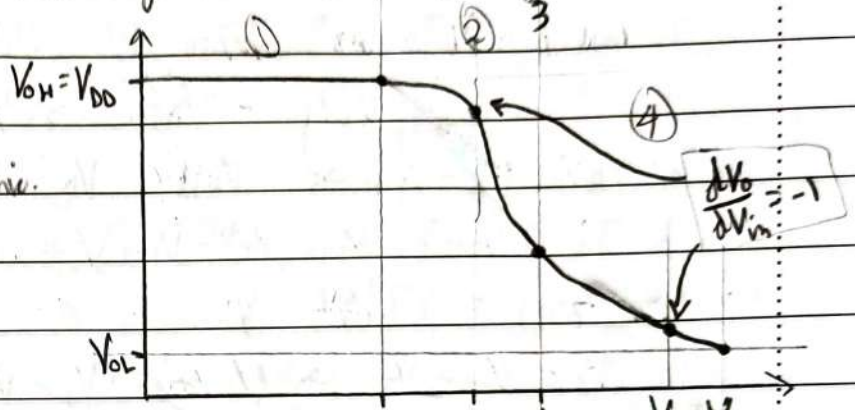
$V_{GSL} = 0 \rightarrow M_L$ is always on, since gate and source are connected

$V_{DSL} < V_{GSL} - V_{TL} \rightarrow M_L$ is linear

$V_{DSL} > V_{GSL} - V_{TL} \rightarrow M_L$ is saturated



- since the depletion NMOS has a negative threshold voltage, the device is normally on



① $V_{in} < V_{TD}$, M_D is off, $I_D = 0$:

- M_L could be sat or ohmic.

assuming sat:

$I_D = k_L (0 - V_T)^2 \neq 0$

hence not sat $\Rightarrow$ linear

$\therefore I_D = k_L V_{DSL} \left[2(V_{GSL} - V_T) - V_{DSL} \right] = 0$

$\rightarrow \boxed{V_{DSL} = 0}$ or $V_{DSL} = -2V_{TL}$, which is larger than $V_{GSL} - V_{TL}$ hence breaks the condition for sat

$\therefore \boxed{V_o = V_{DD}}$

② $V_{in} > V_{TD}$, M_D becomes saturated, M_L remains linear:

$k_1 (V_{GS1} - V_{TD})^2 = k_L V_{DSL} \left[2(V_{GSL} - V_{TL}) - V_{DSL} \right]$

$\therefore k_1 (V_i - V_{TD})^2 = k_L (V_{DD} - V_o) \left[-2V_{TL} - (V_{DD} - V_o) \right]$

then find V_{IL}

③ at $V_{in} = V_{SS}$, M_D will stay in sat, whereas M_D will enter sat:

EOS: $V_{DS1} = V_{GS1} - V_{T1} = V_{SS} - V_{T1} = V_{OSS}$

$\Rightarrow k_1 (V_{GS1} - V_{TD})^2 = k_L (V_{GSL} - V_{TL})^2$ $\because V_{GSL} = 0$ $\therefore V_{GS1} = V_{SS}$

$\therefore V_{SS} = V_{TD} \pm \sqrt{\frac{k_L}{k_1}} \cdot V_{TL}$

$\rightarrow \boxed{V_{OSS}^2 = \frac{k_L}{k_1} \cdot V_{TL}^2}$

	①	②	③	④
M_L	linear	linear	sat	sat
M_D	cutoff	linear	sat	linear

④ $V_{in} > V_{SS}$, M_D is linear, M_L remains saturated

$k_1 V_{DS1}[2(V_{GS1} - V_{T1}) - V_{DS1}] = k_L(V_{GSL} - V_{TL})^2$

$\rightarrow k_1 V_o[2(V_i - V_{T1}) - V_o] = k_L(0 - V_{TL})^2$

then find V_{IH}, or V_{OL} if $V_i = V_{DD}$

- V_{OL} is the output voltage corresponding to an input equal to V_{DD}
- larger $\frac{k_L}{k_1}$ makes the curve steeper and closer to ideal

example: $V_{T1} = 1V$, $V_{TL} = -1V$, $k_1 = 1\times10^{-3}\ A/V^2$

$k_L = 0.2\times10^{-3}\ A/V^2$, $V_{DD} = 5V$. find V_{IL}, V_{IH}, and V_{OL}:

$\therefore V_{IL} = V_{T1} \pm \sqrt{\frac{k_L}{k_1}} \cdot V_{TL} \rightarrow V_{IL} = 0.553V$ or $1.447V$

$0.553 \rightarrow V_{GSL} = V_{in} - V_{T1} \rightarrow$ negative $\rightarrow M_1$ cutoff ✗

$\therefore V_{IL} = 1.447\ V$

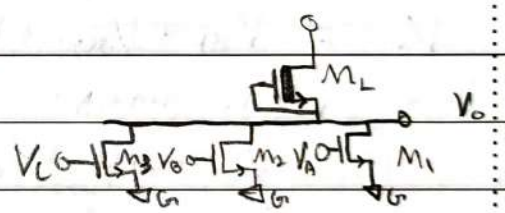
$\therefore V_{IH} = \pm V_{TL}\sqrt{\frac{k_L}{k_1}} \rightarrow V_{IH} = 0.447V$

for V_{OL} ④ $\rightarrow k_1 V_o[2(V_{DD} - V_{T1}) - V_o] = k_L(-V_{TL})^2$

$\therefore 2V_o \cdot (4) - V_o^2 = 0.2 \rightarrow V_o = 25\ mV$

* N-MOS NOR gate:

A	B	C	V_o
0	0	0	1 V_{DD}
0	0	1	0 V_{DS1}
↓	↓	↓	↓
1	1	1	0 V_{DS1}



load is sat and others active $\rightarrow I_L = k_L(V_{GSL} - V_{TL})^2$

$\wedge\ I_L = mI_D$, m: number of transistors for input

$M_1 \rightarrow 3$ are linear: $I_D = k_D \cdot V_{DSD}[2(V_{GSD} - V_{TD}) - V_{DSD}]$

$\therefore mI_D = m k_D \cdot V_{DSD}[2(V_{GSD} - V_{TD}) - V_{DSD}] = k_L(V_{GSL} - V_{TL})^2$

- worst case is when $m=1$ $\wedge$ $V_{OL} < V_{T1}$

example on NMOS NOR

① $A=B=C=5V \rightarrow m=3$

$\rightarrow 3 \cdot k' \cdot \frac{W}{L} \cdot V_o[2(V_{DD}-V_{TL})-V_o] = 0.34 \times 10^{-3}(-V_{TL})^2$

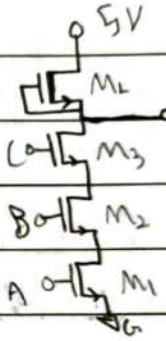
$\rightarrow 8V_o - V_o^2 = \frac{17}{150} \rightarrow V_o = 14.14\ mV$

② if $A=5 \wedge B=C=0V \rightarrow m=1$

$\therefore 8V_o - V_o^2 = 0.34 \rightarrow V_o = 42.73\ mV$

* NMOS NAND gate:

- any low input gives $I_L=0 \wedge V_o=V_{DD}$
- if all inputs are high ($A=B=C=V_{DD}$), then all MOSFETs are in linear mode



$\rightarrow V_{GS1} = A = V_{DD}$

$V_{GS2} = B - V_{DS1} = V_{DD} - V_{DS1}$

$V_{GS3} = V_{DD} - V_{DS1} - V_{DS2}$

$V_o = V_{DS1} + V_{DS2} + V_{DS3}$

example on NMOS NAND:

① $V_{o1} = V_{DS1} + V_{DS2} + V_{DS3} \wedge I_D = 1mA = k_n(-V_{TL})^2$

$= k_n \cdot V_{DSx}[2(V_{GSx}-V_{TL})^2 - V_{DSx}]$

$\therefore -V_{DSx}^2 + 2(V_{GSx}-1) \cdot V_{DSx} - 0.5 = 0$

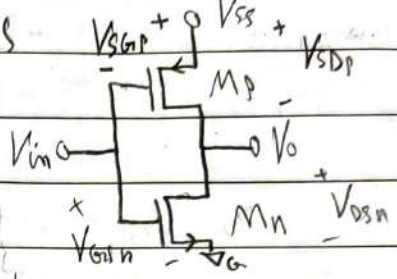
$\rightarrow V_{DS1} = 62.99\ mV,\ V_{DS2} = 64.02\ mV,\ V_{DS3} = 65.09\ mV$

$\therefore V_{o1} = 0.1921\ V$

② $\because 1mA = k_n$

Subject CMOS logic Date 8/5/2021 No.

* CMOS: complementary metal oxide semiconductors
* CMOS inverter: consists of NMOS and PMOS



① $0 < V_{in} < V_{TN}$, M_n off, M_p ohmic:

$k_p V_{SDp}[2(V_{SGp} - |V_{TP}|) - V_{SDp}] = 0 \rightarrow V_{SDp} = 0$

$\rightarrow V_o = V_{DD}$

② $V_{TN} < V_{in} < V_{SS}$, M_n sat, M_p ohmic:

$\rightarrow k_n (V_{GSn} - V_{TN})^2 = k_p V_{SDp}[2(V_{SGp} - |V_{TP}|) - V_{SDp}]$

$\therefore k_n (V_{in} - V_{TN})^2 = k_p (V_{DD} - V_o)[2(V_{DD} - V_{in} - |V_{TP}|) - (V_{DD} - V_o)]$

③ $V_{in} = V_{SS}$, M_n sat, M_p sat:

$\rightarrow k_n (V_{GSn} - V_{TN})^2 = k_p (|V_{SGp}| - |V_{TP}|)^2$

$\therefore k_n (V_i - V_{TN})^2 = k_p (V_{DD} - V_i - |V_{TP}|)^2$

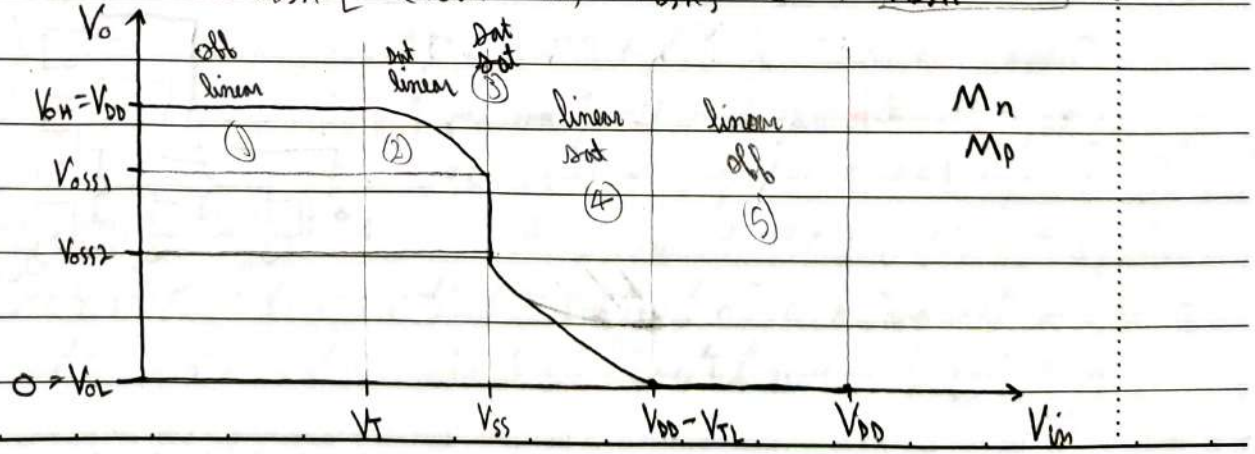
④ $V_{SS} < V_{in} < V_{DD} - V_{TN}$, M_n ohmic and M_p sat:

$k_n V_{DSn}[2(V_{GSn} - V_{TN}) - V_{DSn}] = k_p (V_{GSp} - |V_{TP}|)^2$

$\therefore k_n V_o[2(V_i - V_{TN}) - V_o] = k_p (V_{DD} - V_i - |V_{TP}|)^2$

⑤ $V_{DD} - V_T < V_{in} < V_{DD}$, M_n is ohmic, M_p is off:

$\rightarrow k_n V_{DSn}[2(V_{GSn} - V_{TN}) - V_{DSn}] = 0 \rightarrow V_{DSn} = 0V = V_o$



tips for using PMOS:
- replace V_{GS} with V_{SG} and replace V_{DS} with V_{SD} in order to use NMOS equations
- use $|V_{TP}|$ for the threshold

MODE: $V_{SGp} > |V_{TP}| \rightarrow$ on
$V_{SDp} > V_{SGp} - |V_{TP}| \rightarrow$ sat

Subject Date No.

* advantages of CMOS logic:
- low power dissipation - better packaging design - high noise immunity
- if $I_{Dn} = I_{Dp}$, $k_n(V_{GSn} - V_{Tn})^2 = k_p(V_{SGp} - |V_{Tp}|)^2$

$$\rightarrow V_{SS} = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}\left[V_{DD} - |V_{Tp}|\right]}{1 + \sqrt{\frac{k_p}{k_n}}}$$

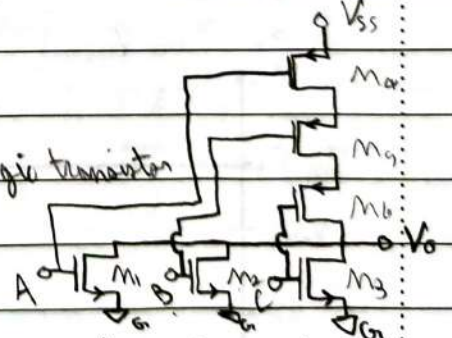
if $k_n = k_p$ & $V_{Tn} = |V_{Tp}|$

$$\rightarrow V_{SS} = \frac{V_{DD}}{2}$$

- at V_{SS}, M_n switches from sat to linear:
EOS $\rightarrow V_{DSn} = V_{GSn} - V_{Tn} = V_{SS} - V_{Tn} = V_{OSS1}$
- at V_{SS}, M_p switches from linear to sat:
$\rightarrow V_{SDp} = V_{SGp} - |V_{Tp}| = V_{DD} - V_{SS} - |V_{Tp}|$
& $V_{SDp} = V_{DD} - V_o \rightarrow V_{DD} - V_{SS} - |V_{Tp}| = V_{DD} - V_o$
$\therefore V_o = V_{SS} + |V_{Tp}| = V_{OSS2}$

example on inverter:
① $k_n = k_p$ & $V_{Tn} = |V_{Tp}| \rightarrow V_{SS} = \frac{V_{DD}}{2} = 2.5V$
② if $V_{in} = V_{SS} \rightarrow$ both on
$I_p = k_p(V_{SGp} - |V_{Tp}|)^2$ & $V_{SG} = V_{DD} - V_{in}$
$\rightarrow I_p = k_p(2.5 - 1)^2 \rightarrow I_p = 4.5\,mA$

* NOR CMOS:
- two transistors are required for every input
- every input transistor requires a complementary logic transistor
- if one input (at least) is high, then one of the logic transistors (at least) will be off
- if a transistor is in linear but its current is zero then the voltage difference between its drain and source will be zero



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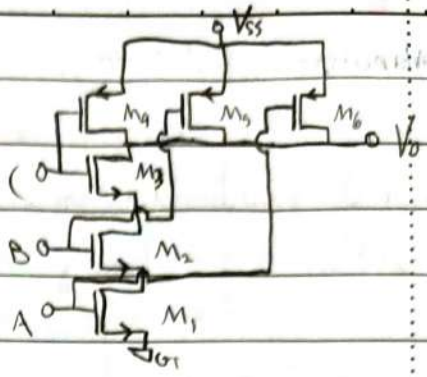
& NAND CMOS:

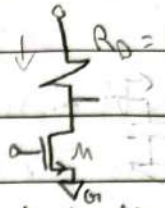
- If one of the input transistors has slow voltage, it will be cutoff, causing the other transistors' currents to equal zero. Hence the output voltage will be high.



Subject Capacitive effects of MOSFETs Date 10/5/2021 No.

given $C_L = 50\,fF = 50 \times 10^{-15}\,F$, $V_{OL} = 0.6V$, $V_{OH} = 5V$

$V_T = 1$ & $k_n = 100\,\mu A/V^2$



- If the input is low, output should switch to high

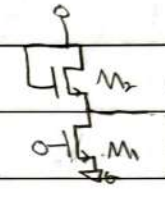
$\therefore i = C\frac{dV_O}{dt} = \frac{V_{DD} - V_O}{R_D}$

- If the input switches from low to high, output should switch back to low : $I_D = I_{RD} + I_{CD}$, $I_{CD} = -\frac{dV_O}{dt} \cdot C$

If $V_O \geq 4$: M → sat → $I_D = k_n[V_{GS} - V_{TN}]^2 = \frac{V_{DD} - V_O}{R_D} - C\frac{dV_O}{dt}$

If $V_O < 4$: M → ohmic → $I_D = k_n \cdot R_D[8V_O - V_O^2] = \frac{V_{DD} - V_O}{R_D} - C\frac{dV_O}{dt}$

* NMOS with saturated ENMOS as load:

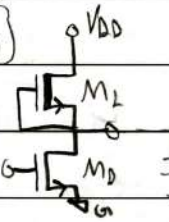


input going from high to low:

$\therefore M_2$ sat → $I_{D2} = k_{n2}(V_{DD} - V_O - V_{T2})^2$

$\therefore i_L = C\frac{dV_O}{dt} = k_{n2}(4 - V_O)^2$

* NMOS inverter with DNMOS as load : $V_{GS1} = 0$



$V_{TL} = -2V$ $V_{DD} = 11V$

$k_L = 25\,\mu A/V^2$

$V_{OL} = 0.1V$

$V_{OH} = 5$ $k_D = 75\,\mu A/V^2$

for $V_O < 3$: $V_{DSL} > V_{GSL} - V_{TL}$ → Sat

$\therefore I_D = C\frac{dV_O}{dt} = k_L(V_{GSL} - V_{TL})^2$

$= k_L(-V_{TL})^2$

$\therefore \boxed{V_O(t) = V_{OL} + \frac{k_L}{C}|V_{TL}|^2 t}$

for $V_O > 3$: $V_{DSL} < -V_{TL}$ → ohmic

$I_D = C\frac{dV_O}{dt} = k_L R_D(2(V_{GSL} - V_{TL}) \cdot V_{DSL} - V_{DSL}^2)$

$\rightarrow C\frac{dV_O}{dt} = k_L \cdot R_D(4(V_{DD} - V_O) - (V_{DD} - V_O)^2)$

} for high to low input

- NMOS with DNMOS load as input goes from low to high

If $V_O > 4$: M_L ohmic, M_D sat $\because V_{DSD} > V_{GSD} - V_{TD}$

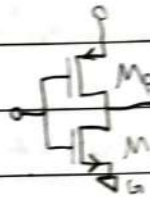
$\rightarrow I_D = k_D \cdot (V_{GSD} - V_{TD})^2 = 1.2mA$

If $V_O > 3$ → M_L : $I_D = k_L(4(V_{DD} - V_O) - (V_{DD} - V_O)^2)$

Subject Date No.

* for $3 < V_o < 4$, M_D & M_L change
M_D: $I_D = k_{nD}(8V_o - V_o^2) = k_{nL}(4(V_{DD}-V_o) - (V_{DD}-V_o)^2)$
* for $V_o < 3$, M_L is sat & M_D is linear
- hence, an ENMOS driver connected to a DNMOS load will pass through three stages (M_L linear & M_D sat, both linear, and M_L sat & M_D linear) while switching from low input to high input (or high input to low)

* CMOS inverter:
• high to low input:



M_p sat initially: $I_D = k_{nP}(V_{DD} - V_i - |V_{Tp}|)^2$
for $V_o < |V_{Tp}|$ $= k_{nP}(V_{DD} - |V_{Tp}|)^2 = C\frac{dV_o}{dt}$
$\therefore V_{SS} - V_o > V_{SS} - V_i - |V_{Tp}|$ $(V_{SD} > V_{SG} - V_{tp})$ condition for sat
- if $V_o > |V_{Tp}| \rightarrow M_p$ goes to ohmic mode

$$\rightarrow C \cdot \frac{dV_o}{dt} = k_{nP}\left(2(V_{DD} - |V_{Tp}|)(V_{DD} - V_o) - (V_{DD} - V_o)^2\right)$$

• for low to high input:
- initially M_n will be sat, M_p will be cutoff
$$\rightarrow C\frac{dV_o}{dt} = -k_{nn}(V_{DD} - V_{Tn})^2$$
- next the drivers will enter linear, whereas M_p will remain off:
$$C\frac{dV_o}{dt} = -k_{nn}\left(2(V_{DD} - V_{Tn})V_o - V_o^2\right)$$