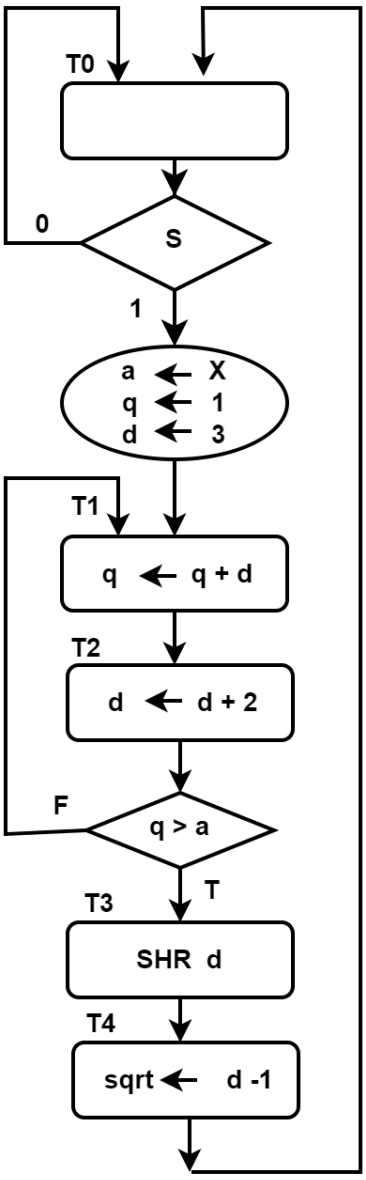
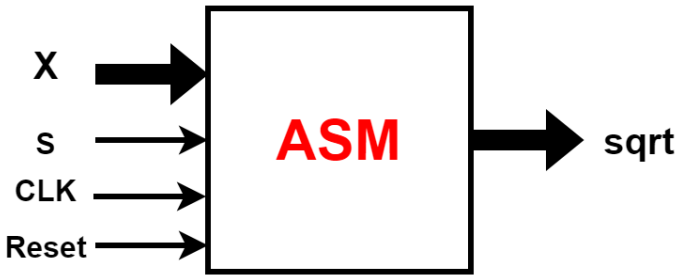
**An-Najah National University**
**Faculty of Engineering and Information Technology**
**Computer Engineering Department**

***Digital Circuit Design II (10636321)***
***Assignment # 1***
***Due to: 29/04/2023***

| (CLO's: VI) | Points:10 |
|---|---|

**Given the following ASM chart which implements an algorithm to find the integer square root for a positive integer number (X)**

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Write a complete **VHDL** code to implement the ASM chart **using 3 processes.**
(Use a positive edge **CLK** and a low-level asynchronous **Reset**)

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity Int_SQRT_Calculator is
  port(   CLK, RESET, S : in  std_logic;
          X       : in  std_logic_vector(7 downto 0);
          Sqrt    : out std_logic_vector(7 downto 0));
end Int_SQRT_Calculator;
```

Notes:

- *The size of the input (X) is 8 bits.*
- *The size of the result sqrt(X) is 8 bits.*
- *SHR: Shift right by one bit.*
- *You can use signals to store the values of **a**, **q**, and **d**.*

**You have to submit two files:**

1. **A VHDL code to implement your ASM.**
2. **A testbench file to simulate and test your design.**

Notes:

1. Select the clock period to be 4 ns
2. You should cover all the values of the input X ( from 1 to 200 ) :-
    - For each case, you have to activate the S signal for 2 clock cycles
    - You have to wait the sufficient time to get the result (e.g. 20 Clock cycles)

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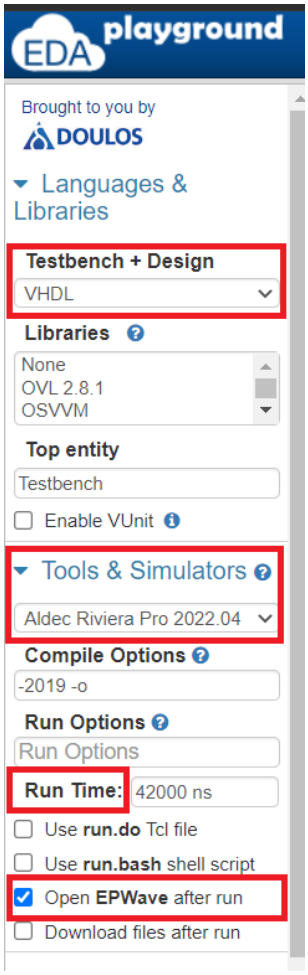
Note: When you select the simulation tool to be "**Aldec Rivera Pro 2022.04**", do not forget to set the **Run Time** to be sufficient to cover the previous test cases.

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