An-Najah National University
Faculty of Engineering
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Department

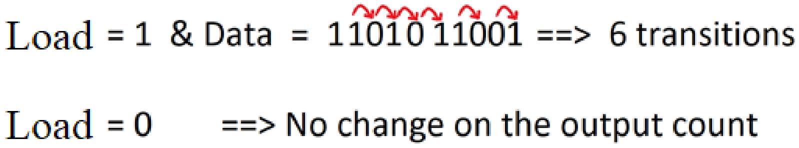
جامعــة النجــاح الوطنيــة
كليــة الهندســة و تكنولوجيا المعلومات
دائرة الهندسة الكهربائية والحاسوب

Due to 28/05/2023

Final Assignment: (CLOs: VI)	Points:10

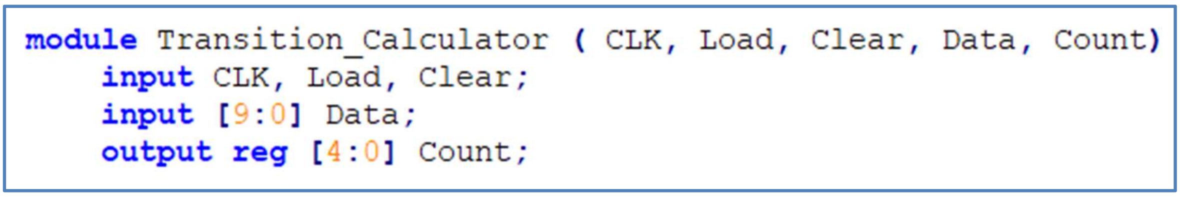
Complete the following Verilog code to implement a digital system that counts the number of bit transitions. This system can load an input data (10-bit) value when the **Load** input is asserted, and then compute the result on the positive edge of the input clock.

e.g.



Load = 1 & Data = 11010 11001 ==> 6 transitions

Load = 0 ==> No change on the output count



```
module Transition_Calculator ( CLK, Load, Clear, Data, Count)
    input CLK, Load, Clear;
    input [9:0] Data;
    output reg [4:0] Count;
```

Your design should include the following pins:

1. **CLK:** (positive edge trigger input clock)
2. **Load:** Synchronous **Active High** Load signals
3. **Clear:** Asynchronous **Active Low** Input (Clear the output)
4. **Count:** The output result which represents the number transitions in the loaded data.

Notes:

- Use behavioral description
- The calculation should be synchronous with the clock when the Load signal is equal to 1. (*the number of transitions should be calculated in a single clock cycle at the rising edge*)

You have to submit two files:

1. A Verilog code to implement your Design.
2. A testbench file to simulate and test your design:
    a. You have to give a test case for the Asynchronous **Clear**,
    b. You have to cover all the possible cases for the input **Data** (1024 different cases)
        i. For each case you have to:
            1. Select a different value for the input **Data**
            2. Set the **Load** signal to **'1'**
            3. Wait for two clock cycles
    c. You have to give a test case to show that no change will occur when the **Load** signal is **'0'**.

`