In the name of the god

# Implementation and test of embedded systems with ASIC

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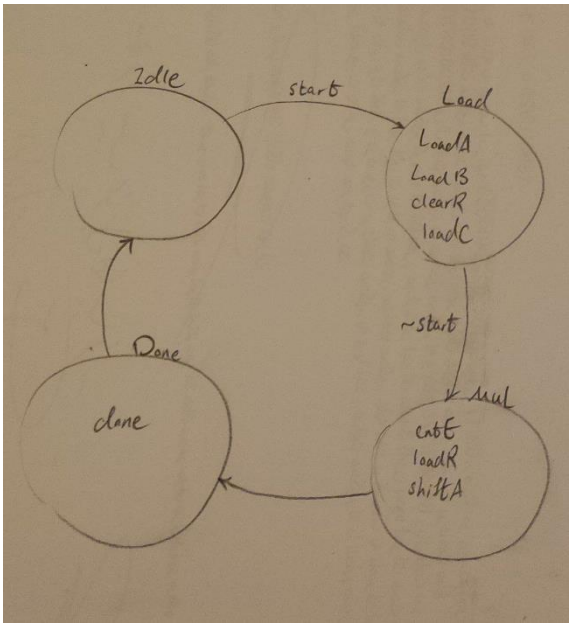
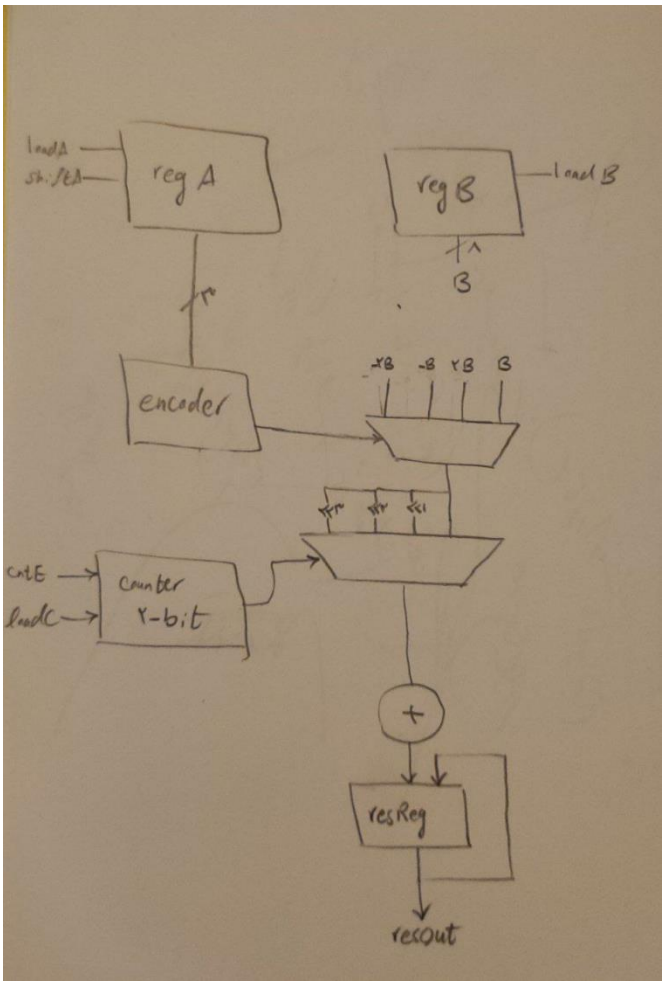
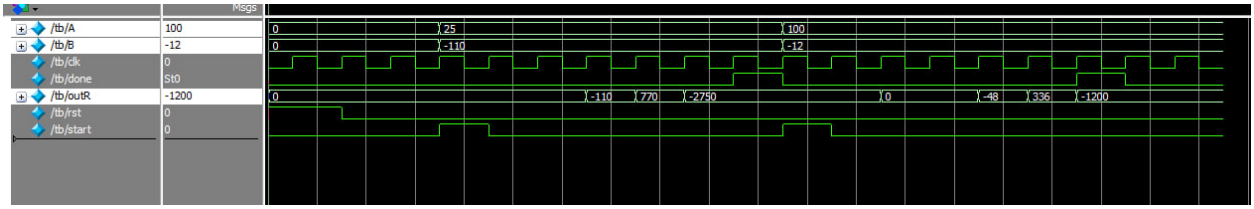
CA1

# Part 1


Idle
start
Load
LoadA
LoadB
clearR
loadC
~start
Done
done
mul
cntE
loadR
shiftA


loadA
reg A
reg B
loadB
B
encoder
-B
counter
Y-bit
cntE
loadC
+
resReg
resOut

# Part 2




In this section two test given and results are shown in the above illustration.

```
VSIM 2> run -all
# Test: A =   36, B = -127, Expected =       -4572, Result =  -4572
# FINE: The result is correct
#        115     tb.done_check done is properly working
# Test: A =    9, B =   99, Expected =         891, Result =    891
# FINE: The result is correct
#        185     tb.done_check done is properly working
# Test: A =   13, B = -115, Expected =       -1495, Result =  -1495
# FINE: The result is correct
#        255     tb.done_check done is properly working
# Test: A =  101, B =   18, Expected =        1818, Result =   1818
# FINE: The result is correct
#        325     tb.done_check done is properly working
# Test: A =    1, B =   13, Expected =          13, Result =     13
# FINE: The result is correct
#        395     tb.done_check done is properly working
# Test: A =  118, B =   61, Expected =        7198, Result =   7198
# FINE: The result is correct
#        465     tb.done_check done is properly working
# Test: A =  -19, B = -116, Expected =        2204, Result =   2204
# FINE: The result is correct
#        535     tb.done_check done is properly working
# Test: A =   -7, B =  -58, Expected =         406, Result =    406
# FINE: The result is correct
#        605     tb.done_check done is properly working
# Test: A =  -59, B =  -86, Expected =        5074, Result =   5074
# FINE: The result is correct
#        675     tb.done_check done is properly working
# Test: A =  -27, B =  119, Expected =       -3213, Result =  -3213
# FINE: The result is correct
#        745     tb.done_check done is properly working
# ** Note: $stop    : D:/Desktop/Asic/CA1/verilog_with_assertion/tb.sv(67)
#    Time: 755 ns  Iteration: 0  Instance: /tb
# Break at D:/Desktop/Asic/CA1/verilog_with_assertion/tb.sv line 67
```

In this section ten random tests are given and checked with assertion.