In the name of God

Digital Electronics

CA4

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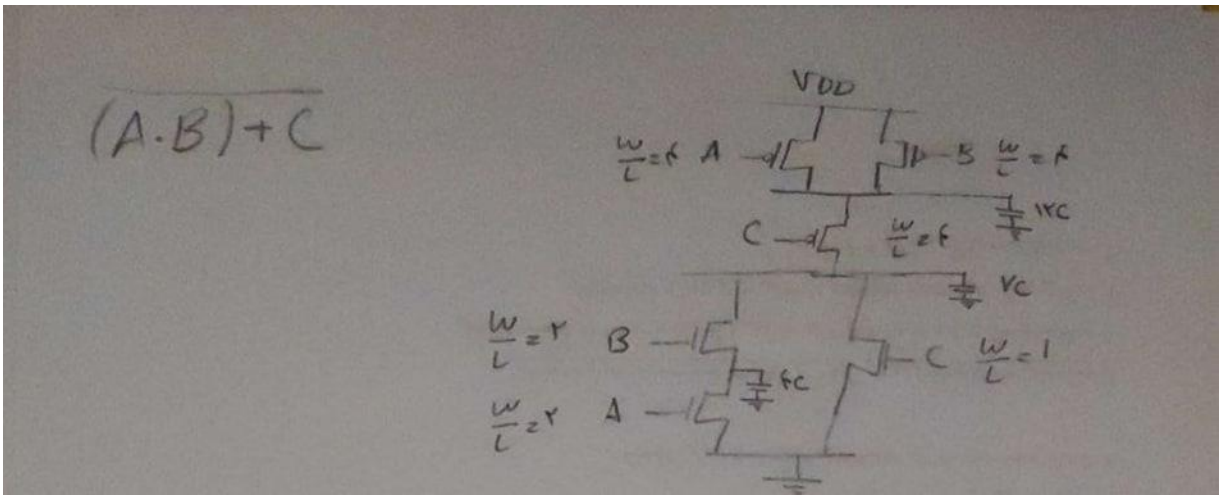
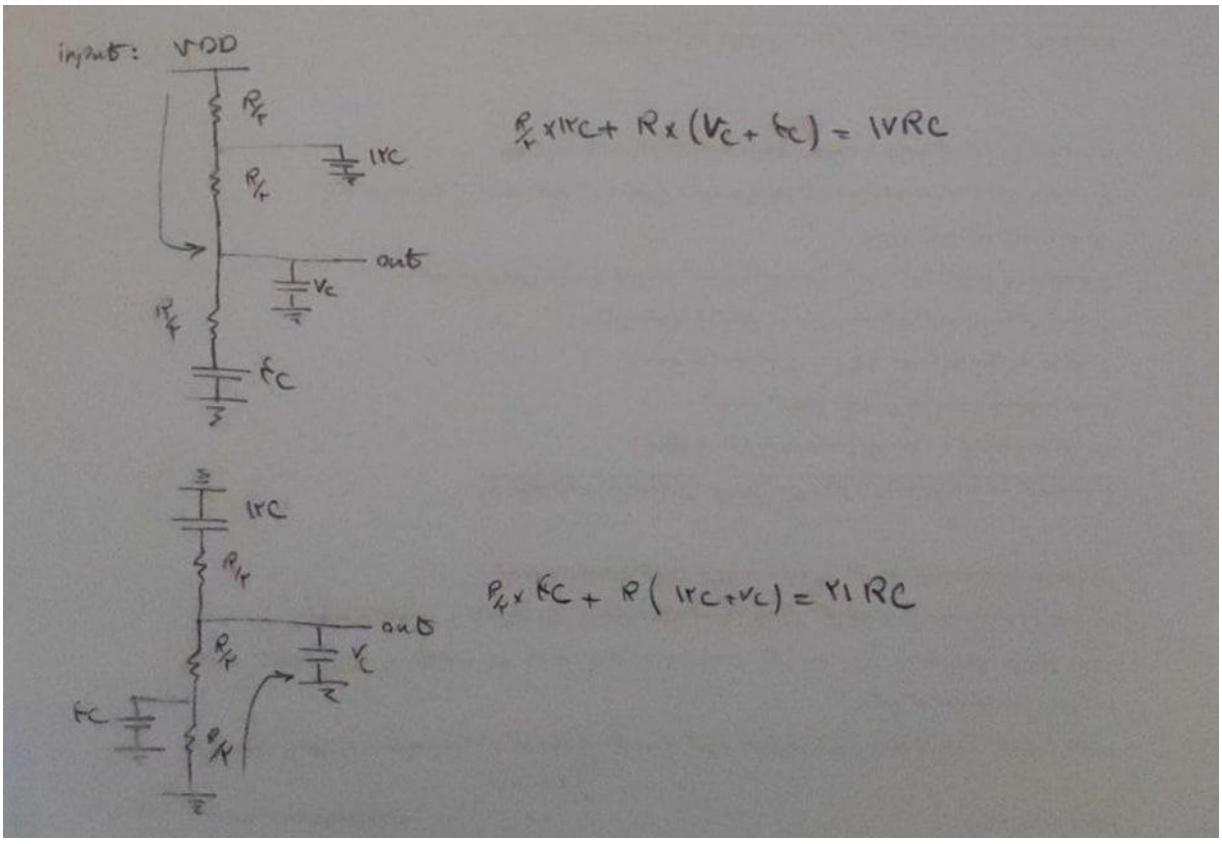
Part 1

1)


(A·B)+C
VDD
A
B
C
Vc

2)


input:
VDD
out
Vc
fc
$\frac{R}{4} \times 11C + R \times (V_C + f_C) = 1VRC$
$\frac{R}{4} \times f_C + R(11C + V_C) = 21RC$

3)

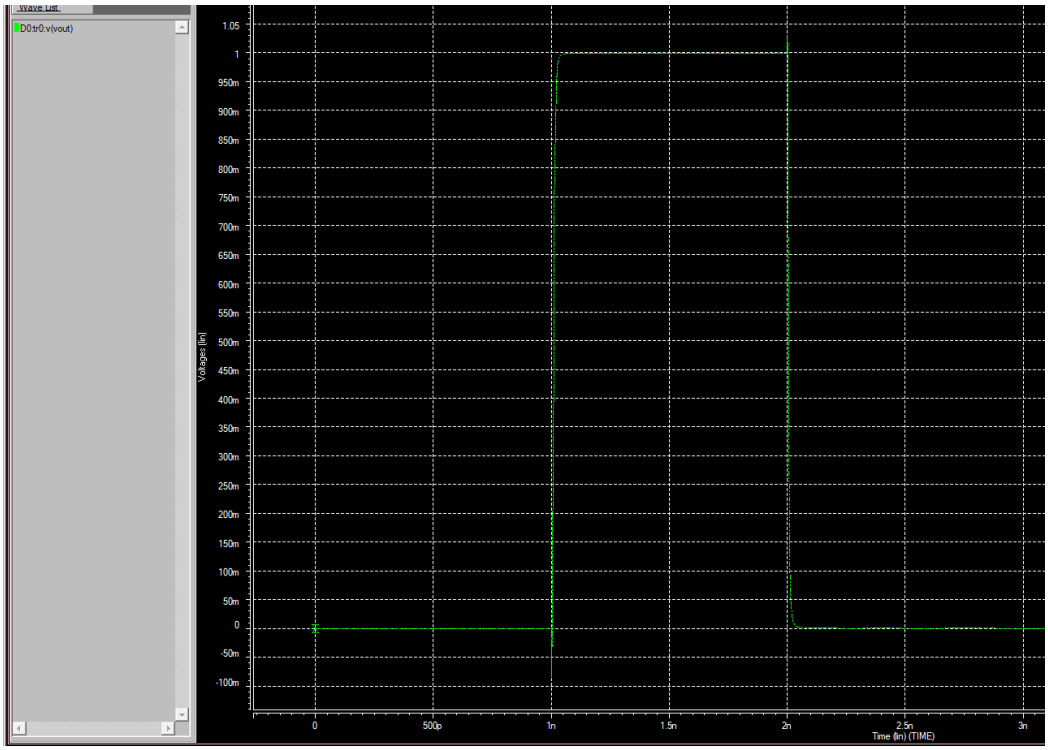
$$\max(0\ to\ 1, 1\ to\ 0) = 21RC$$

4) The inputs are applied using a vector.

VEC_FILE.txt

D: > Desktop > Electronic Digital > CA4 > part 1 > VEC_FILE.txt

```
; specifies # of bits associated with each vector
radix 1 1 1 1
;*****************************************************
; defines name for each vector. For multi-bit vectors,
; innermost [] provide the bit index range, MSB:LSB
vname A B C Vout
;*****************************************************
; defines vector as input, output, or bi-directional
io i i i o
; defines time unit
tunit ns
slope 0.001
PERIOD 1
ODELAY 0.75
;*****************************************************
vih 1 1 1 1 0
vil 0 1 1 1 0
voh 0.85 0 0 0 1
vol 0.15 0 0 0 1
; tabular data section
1 1 0 0
0 1 0 1
1 1 0 0
```



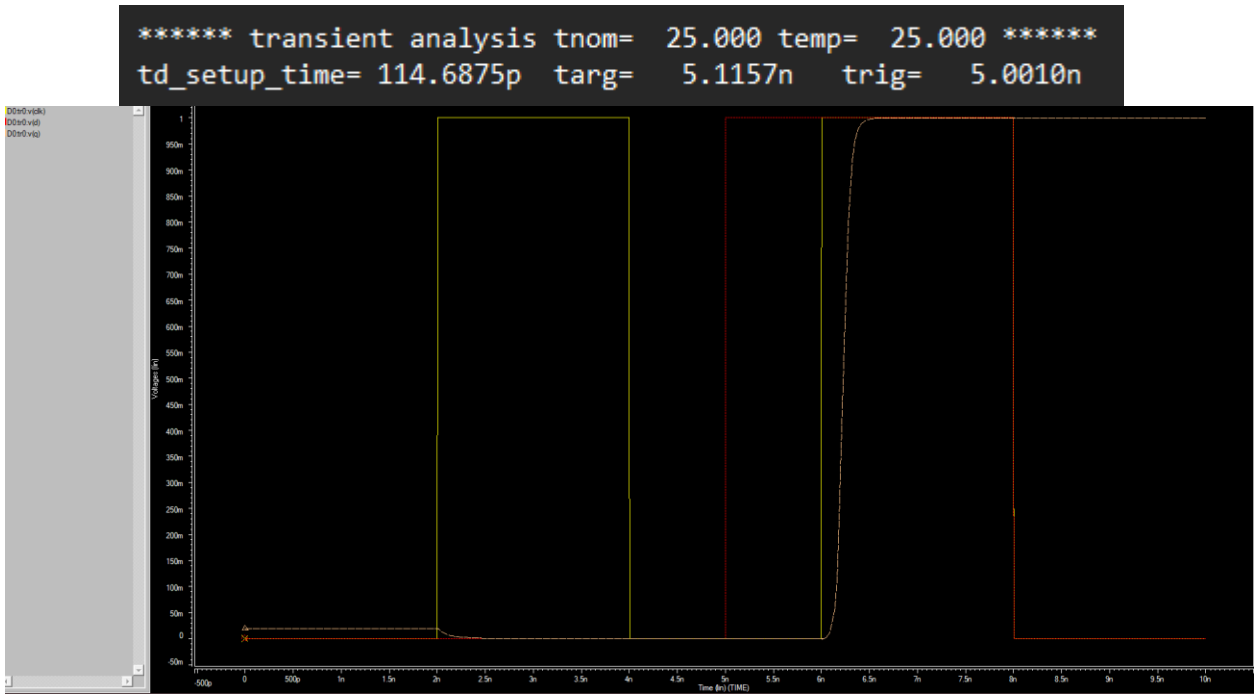
5)

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
td_zero_to_one=   9.7226p  targ=   1.0102n   trig=   1.0005n
td_one_to_zero=   6.1880p  targ=   2.0067n   trig=   2.0005n
```

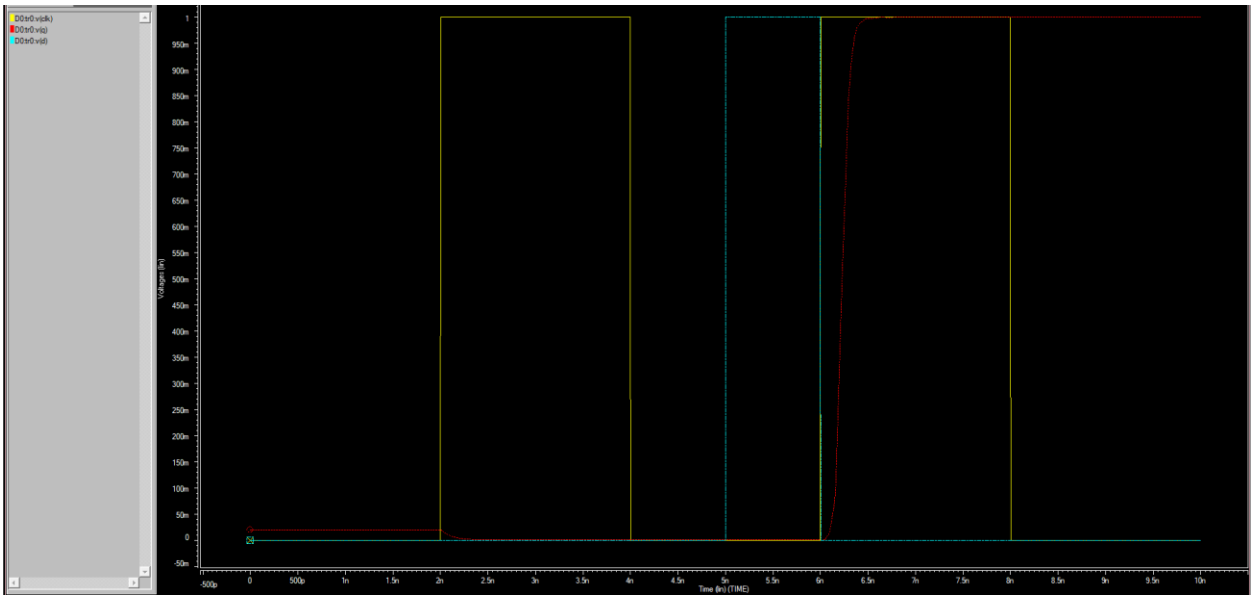
Part 2

1) This register is **dynamic** and **positive-edge triggered** because when the clock is high, the **master section** is sampling the input, and it continues doing so until the clock goes high. Meanwhile, the **slave section** transfers the input to the output and holds it.

2) The calculation is done as follows: when the input **D** passes **50%** of its value, the first node (the one before the first NOT gate) reaches **50%** of its value.



3) **Hold time:** Theoretically, as discussed in class, the **hold time** for this structure is considered to be **zero**.



At the very moment when the clock goes high, the input value becomes **zero**.

rise time：

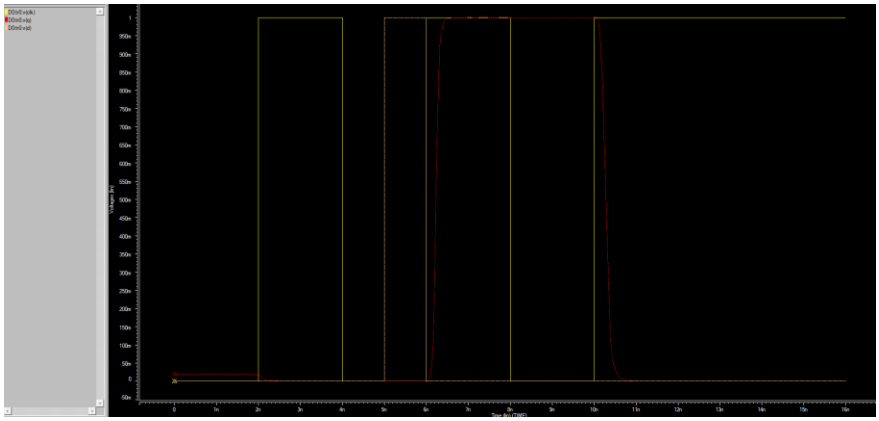
```
td_rise_time= 157.4687p  targ=   6.3163n   trig=   6.1588n
```

fall time：

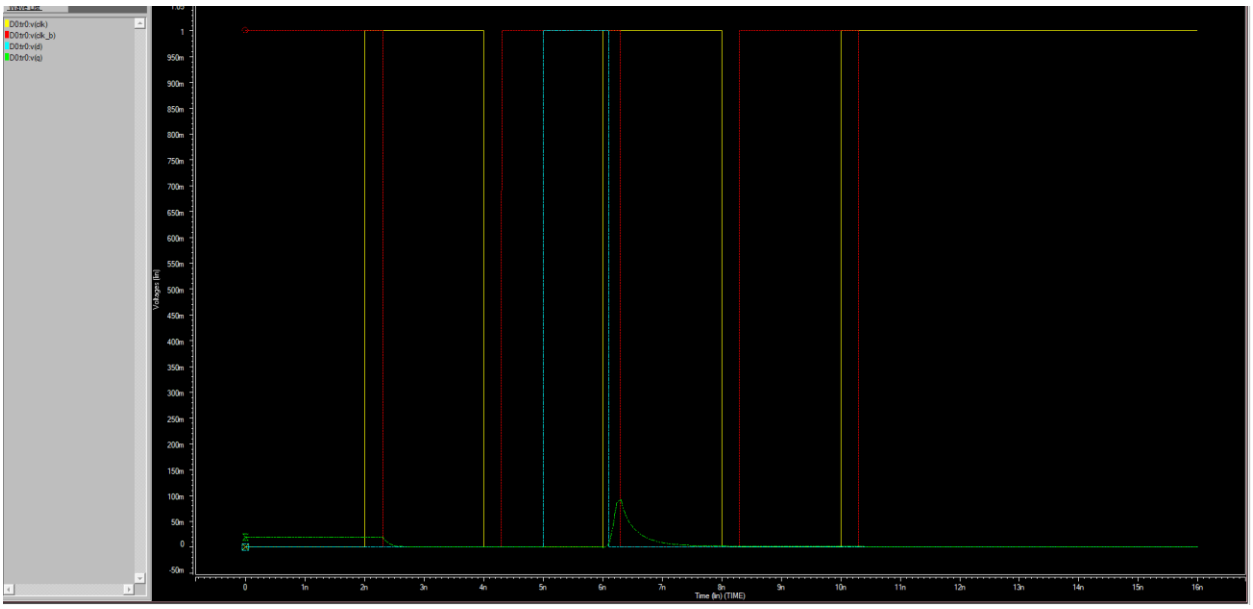
```
td_fall_time= 234.6524p  targ=  10.4030n   trig=  10.1683n
```

Clk-Q：

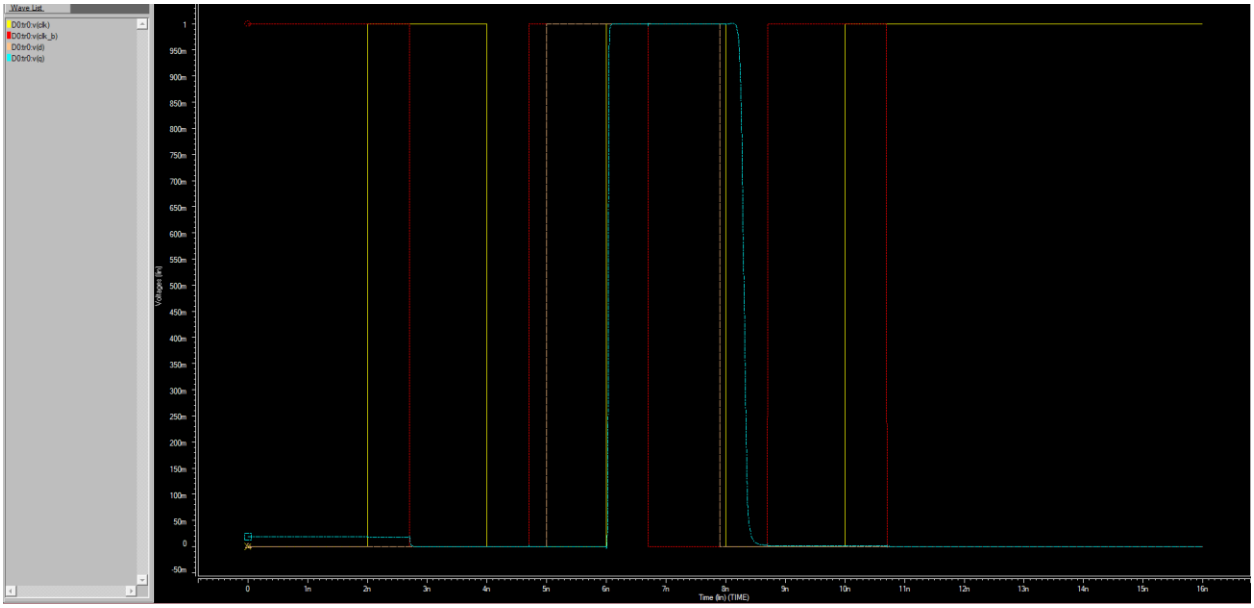
```
td_clk-q= 227.9998p  targ=   6.2290n   trig=   6.0010n
```



4)



As shown in the figure, in the **1-1 state**, the input does not reach the output, even though **0.1 nanoseconds** was considered as the hold time in this scenario.

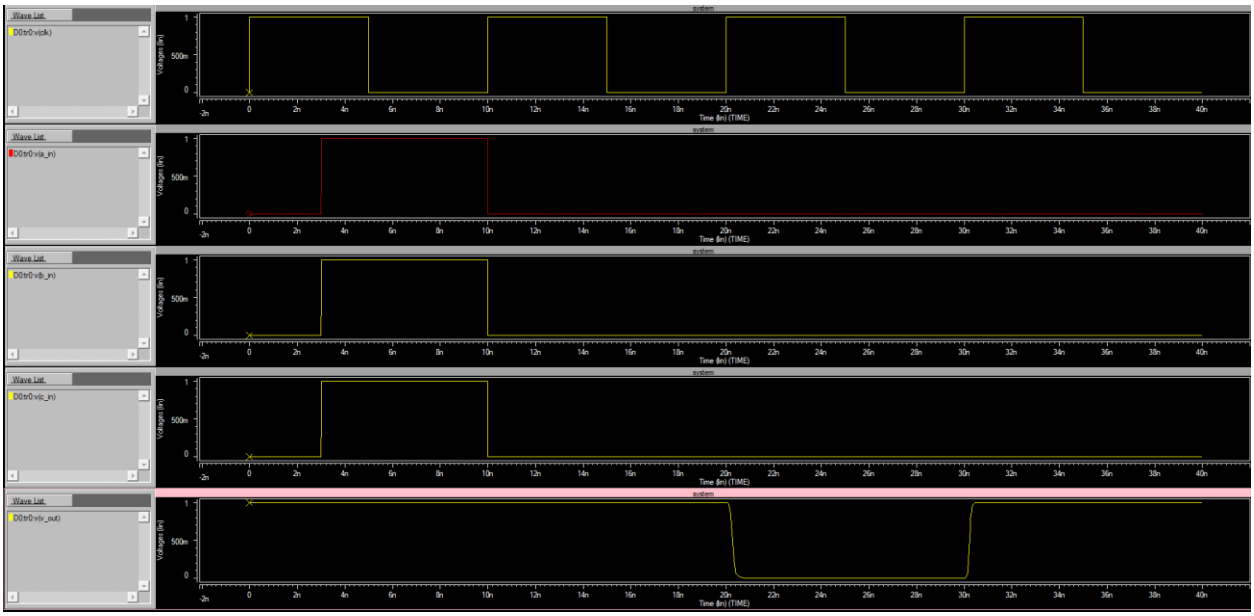


In the figure above, for the **0-0 state**, the output value has changed (for convenience, in this case, the capacitor value was reduced to decrease the circuit delay).

In general, the **overlap of signals** forms a direct path from input to output, which can disrupt the designed register structure. This is especially critical when the **0-0 state** occurs for a register operating with a **positive-edge clock**, because the **negedge of the input** can change the output, which contradicts the intended operation of the register.

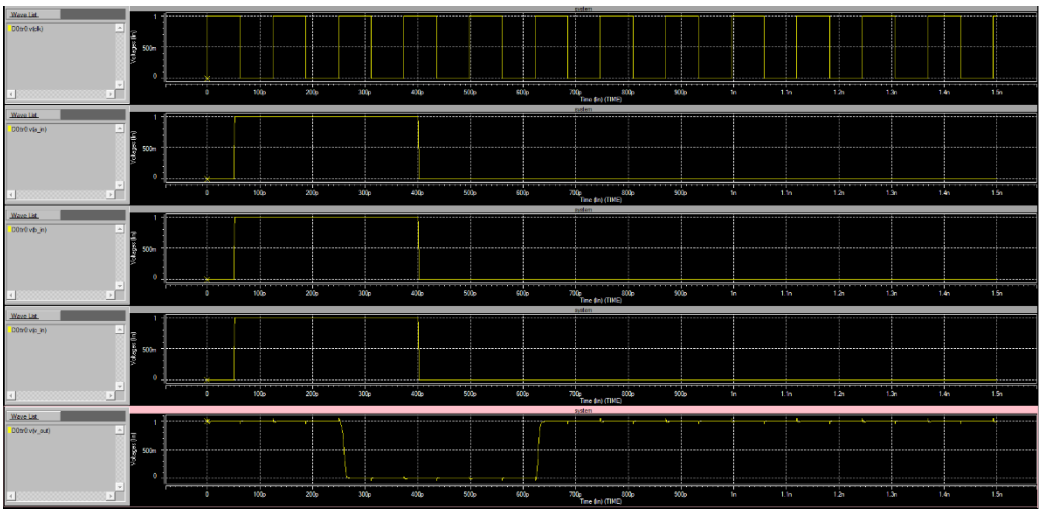
Part 3

1)



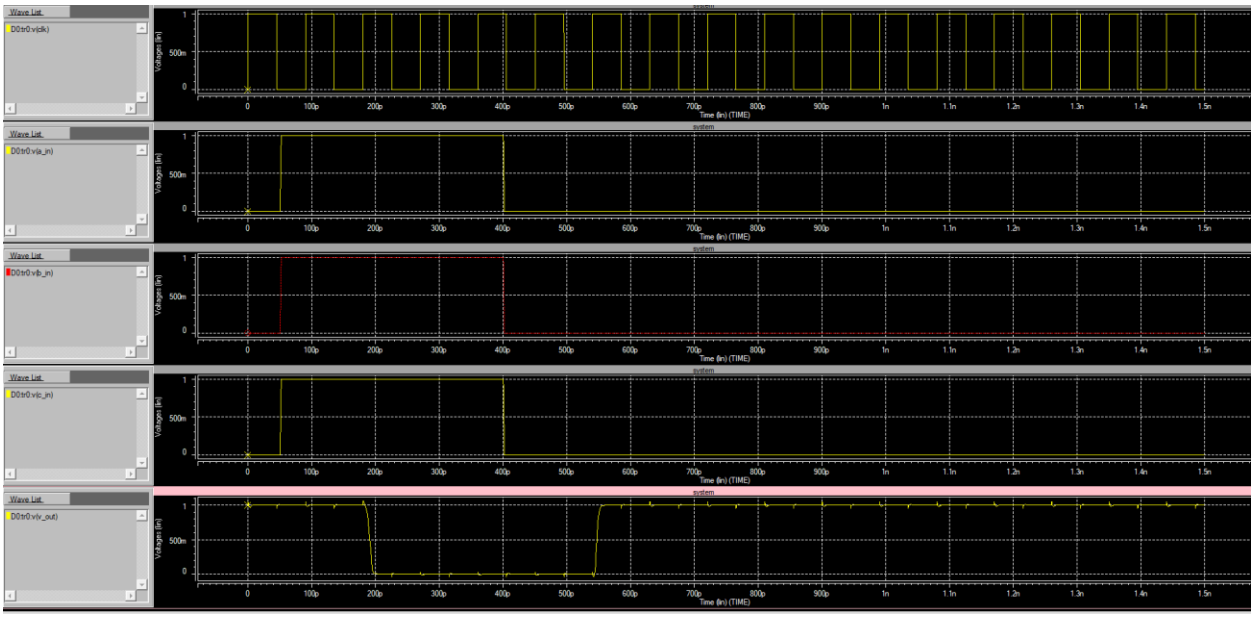
2) The inputs **111** and **000** are applied to the circuit. On the **second clock edge**, the input is captured and stored in the input registers, and in the next cycle, the output registers produce the corresponding output. Additionally, with a **one-cycle delay**, when all inputs become zero, the output also becomes zero. (similar to a **pipeline**)

3)

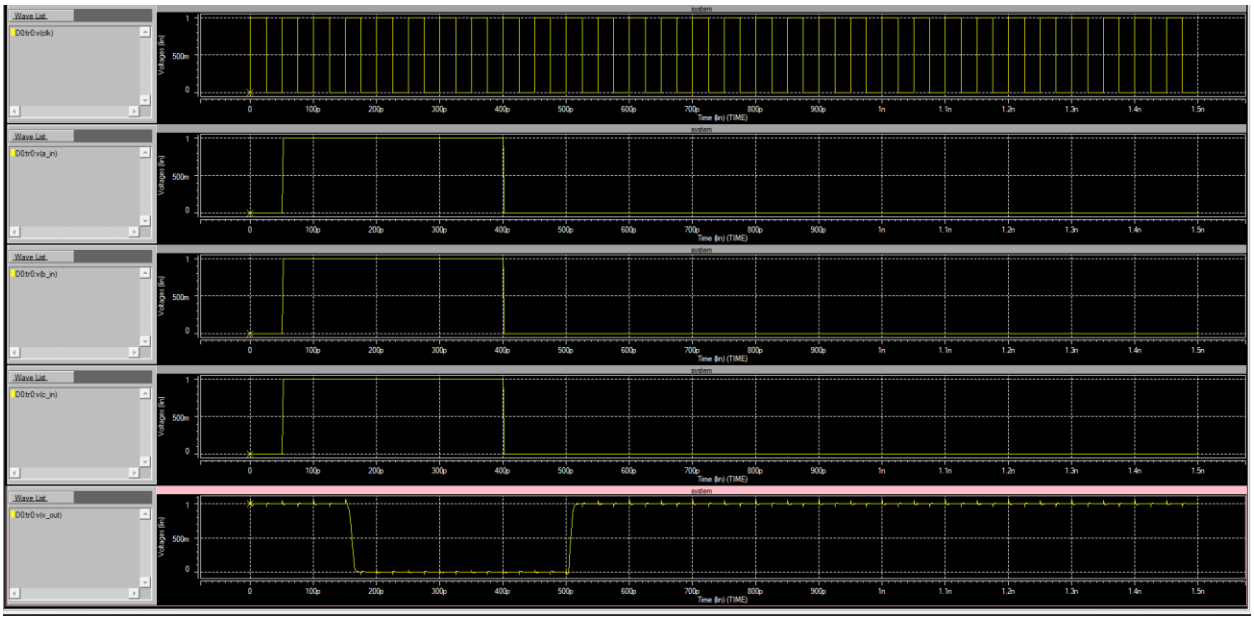


In the figure above, the inputs **000** and **111** are applied to the system, and the **clock period** is **124.41012 picoseconds**, which corresponds to a maximum operating frequency of **8.037 MHz**. As shown in the figure, the circuit operates correctly. Additionally, the **register capacitors** were reduced to **0.01 femtofarads** so that the **hold time** would not increase beyond its current value.

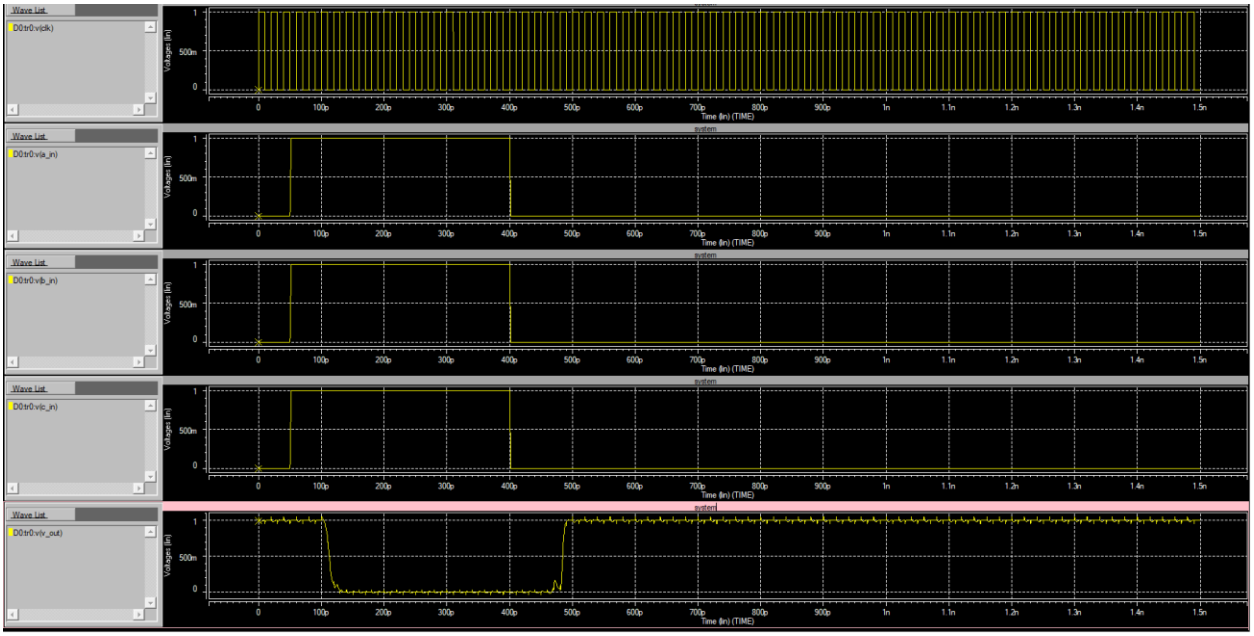
4)



T = 90ps



T = 50ps



T = 20ps

As previously mentioned, increasing the circuit frequency beyond the calculated value prevents the circuit from properly sampling and, in general, does not allow enough time to transfer the output data on the **positive clock edge**. Therefore, in the case of **T = 20 ps**,

the circuit can transfer the input to the output only after several clock cycles, because with each clock pulse, some of the capacitors inside the register gradually charge.