

In the name of god

Implementation and test of embedded systems with ASIC

Mohammad Yahyapour

810100234

CA2

Part A

clock	Timing (slack)	area	Dynamic Power	Leakage Power
100MHz	8.58	296.352003	38.2185 uW	27.2254 pW
200MHz	3.58	296.352003	76.4370 uW	27.2254 pW
500MHz	0.58	296.352003	191.0925 uW	27.2254 pW
5GHz	-0.55	546.603609	6.2998 mW	92.0168 pW

4-a) When we increase clock frequency, it is harder for the design compiler to meet the slack as happens in the last case that it could not meet the timing constraint and there is timing violation.

4-b) Well, as long as the design compiler can make slack upper than zero, it would not change area and power.

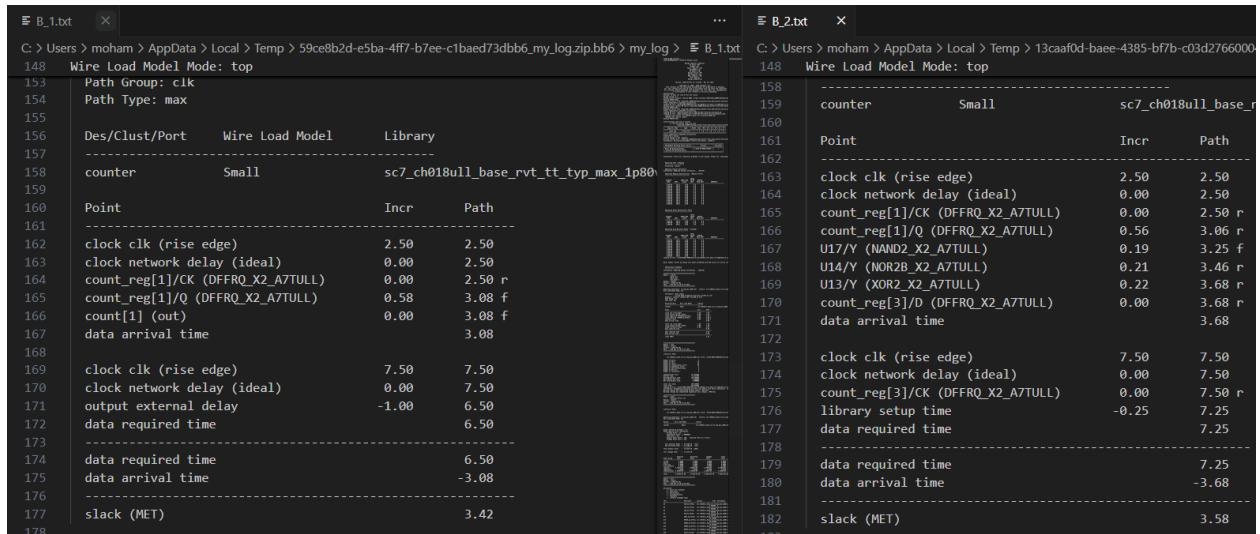
4-c) First three cases slacks are met although in last one it violates it. The design compiler in this case done it best to reach the slack with cost of more area and power but it was not enough.

4-d) As mentioned above as long as slack won't violated power won't change at all but whenever it could not meet constrains add much complex cells that would increase power and area. In the first three cases dynamic power rose linearly cause has linear relation with clock frequency.

4-e) It was addressed before, that as long as design compiler can meet slack it wont changed design but if it could not uses complex cells that increase power consumption and area.

Part B

delay	Timing (slack)	area	Dynamic Power	Leakage Power
1ns	3.42	296.352003	76.4370 uW	27.2254pW
0.2ns	3.58	296.352003	76.4370 uW	27.2254pW



```

C:\> Users > moham > AppData > Local > Temp > 59ce8b2d-e5ba-4ff7-b7ee-c1baed73dbb6_my_log.zip.bb6 > my_log > B_1.txt
148 Wire Load Model Mode: top
153 Path Group: clk
154 Path Type: max
155
156 Des/Clust/Port    Wire Load Model      Library
157 -----
158 counter          Small               sc7_ch018ull_base_rvt_tt_typ_max_1p80
159
160 Point            Incr    Path
161 -----
162 clock clk (rise edge)   2.50   2.50
163 clock network delay (ideal) 0.00   2.50
164 count_reg[1]/CK (DFFRQ_X2_A7TULL) 0.00   2.50 r
165 count_reg[1]/Q (DFFRQ_X2_A7TULL) 0.58   3.08 f
166 count[1] (out)        0.00   3.08 f
167 data arrival time     3.08
168
169 clock clk (rise edge)   7.50   7.50
170 clock network delay (ideal) 0.00   7.50
171 output external delay -1.00   6.50
172 data required time     6.50
173
174 data required time     6.50
175 data arrival time     -3.08
176
177 slack (MET)           3.42

C:\> Users > moham > AppData > Local > Temp > 13caaf0d-bae4-4385-bf7b-c03d27660000
148 Wire Load Model Mode: top
158 -----
159 counter          Small               sc7_ch018ull_base_r
160 Point            Incr    Path
161 -----
162 clock clk (rise edge)   2.50   2.50
163 clock network delay (ideal) 0.00   2.50
164 count_reg[1]/CK (DFFRQ_X2_A7TULL) 0.00   2.50 r
165 count_reg[1]/Q (DFFRQ_X2_A7TULL) 0.56   3.06 r
166 count[1]/Q (DFFRQ_X2_A7TULL) 0.19   3.25 f
167 U17/V (NAND2_X2_A7TULL) 0.21   3.46 r
168 U13/V (XOR2_X2_A7TULL) 0.22   3.68 r
169 U13/V (XOR2_X2_A7TULL) 0.00   3.68 r
170 count_reg[3]/D (DFFRQ_X2_A7TULL) 0.00   3.68 r
171 data arrival time     3.68
172
173 clock clk (rise edge)   7.50   7.50
174 clock network delay (ideal) 0.00   7.50
175 count_reg[3]/CK (DFFRQ_X2_A7TULL) 0.00   7.50 r
176 library setup time     -0.25   7.25
177 data required time     7.25
178
179 data required time     7.25
180 data arrival time     -3.68
181
182 slack (MET)           3.58

```

3-a) In this case I/O delays do not affect our design so much to make them negative. so, nothing changed. But if delay increases it might change area and power to achieve positive slack.

3-b) Nothing has changed cause there is no pressure on slack so design compiler didn't change the design.

3-c) There is no violation here.

3-d) There is no difference between two designs.

B_1.txt						B_2.txt					
C:\Users\moham\AppData\Local\Temp>59ce8b2d-e5ba-4ff7-b7ee-c1baed73dbb6_my_log.zip.bb6>my_log> B_1.txt						C:\Users\moham\AppData\Local\Temp>13caef0d-bae4-4385-bf7b-c03d27660004_my_log.zip.004>my_log> B_2.txt					
Attributes:						Attributes:					
277	n - noncombinational					282	n - noncombinational				
278	r - removable					283	r - removable				
279	u - contains unmapped logic					284	u - contains unmapped logic				
280						285					
281	Cell	Reference	Library	Area	Attributes	286	Cell	Reference	Library	Area	Attributes
283	U3	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	6.585600	d	288	U3	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	6.585600	d
284						289					
285	U4	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	6.585600	d	290	U4	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	6.585600	d
286						291	U5	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	6.585600	d
287	U5	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	6.585600	d	292					
288						293					
289	U6	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	6.585600	d	294	U6	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	6.585600	d
290						295					
291	U13	XOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	19.756800		296	U13	XOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	19.756800	
292						297					
293	U14	NOR2B_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	10.976000		298	U14	NOR2B_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	10.976000	
294						299					
295	U15	XNOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	19.756800		300	U15	XNOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	19.756800	
296						301					
297	U16	XNOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	19.756800		302	U16	XNOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	19.756800	
298						303					
299	U17	NAND2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	8.788000		304	U17	NAND2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	8.788000	
300						305					
301	U18	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	6.585600		306	U18	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	6.585600	
302						307					
303	count_reg[0]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	46.099201	n	308	count_reg[0]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	46.099201	n
304						309					
305	count_reg[1]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	46.099201	n	310	count_reg[1]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	46.099201	n
306						311					
307	count_reg[2]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	46.099201	n	312	count_reg[2]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	46.099201	n
308						313					
309	count_reg[3]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	46.099201	n	314	count_reg[3]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_1p80v.	46.099201	n
310						315					
311	Total 14 cells			296.352003		316					
312	design_vision> Current design is 'counter'.					317	Total 14 cells			296.352003	
313						318	design_vision> Current design is 'counter'.				
314						319					

Part C

	Timing (slack)	area	Dynamic Power	Leakage Power
100%	3.58	296.352003	76.4370 uW	27.2254 pW
80%	3.58	296.352003	76.4370 uW	27.2254 pW

3-a) For this case our design is too small. so basically, design compiler done its best and cannot optimize it more and make it smaller. So, there are no changes.

3-b) As addressed in last part in this case there is no trade-off. However, in larger design it might be possible to affect timing and make it worse.

3-c) If the design was larger, it might be!

3-d) As the illustration below states there are no changes.

C:\Users\moham\AppData\Local\Temp>d0a7f7de-591f-4b19-80c3-a1b0b8bb696_my_log.zip.696>my_log>C_1.txt

284 Attributes:

287 h - hierarchical
288 n - noncombinational
289 r - removable
290 u - contains unmapped logic

291

Cell	Reference	Library	Area	Attributes
294 U3	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
295		6.585600 d		
296 U4	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
297		6.585600 d		
298 U5	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
299		6.585600 d		
300 U6	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
301		6.585600 d		
302 U13	XOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
303		19.756800		
304 U14	NOR2B_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
305		10.976000		
306 U15	XNOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
307		19.756800		
308 U16	XNOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
309		19.756800		
310 U17	NAND2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
311		8.780800		
312 U18	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
313		6.585600		
314 count_reg[0]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
315		46.099201 n		
316 count_reg[1]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
317		46.099201 n		
318 count_reg[2]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
319		46.099201 n		
320 count_reg[3]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
321		46.099201 n		
322				
323 Total 14 cells		296.352003		
324 design_vision> Current design is 'counter'.				

C:\Users\moham\AppData\Local\Temp>44ebcd1-3964-4380-8070-9fd499576a41_my_log.zip.a41>my_log>C_2.txt

284 Attributes:

287 h - hierarchical
288 n - noncombinational
289 r - removable
290 u - contains unmapped logic

291

Cell	Reference	Library	Area	Attributes
294 U3	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
295		6.585600 d		
296 U4	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
297		6.585600 d		
298 U5	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
299		6.585600 d		
300 U6	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
301		6.585600 d		
302 U13	XOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
303		19.756800		
304 U14	NOR2B_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
305		10.976000		
306 U15	XNOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
307		19.756800		
308 U16	XNOR2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
309		19.756800		
310 U17	NAND2_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
311		8.780800		
312 U18	INV_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
313		6.585600		
314 count_reg[0]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
315		46.099201 n		
316 count_reg[1]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
317		46.099201 n		
318 count_reg[2]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
319		46.099201 n		
320 count_reg[3]	DFFRQ_X2_A7TULL	sc7_ch018ull_base_rvt_tt_typ_max_ip80v		
321		46.099201 n		
322				
323 Total 14 cells		296.352003		
324 design_vision> Current design is 'counter'.				