In the name of God

Digital Electronics

CA1

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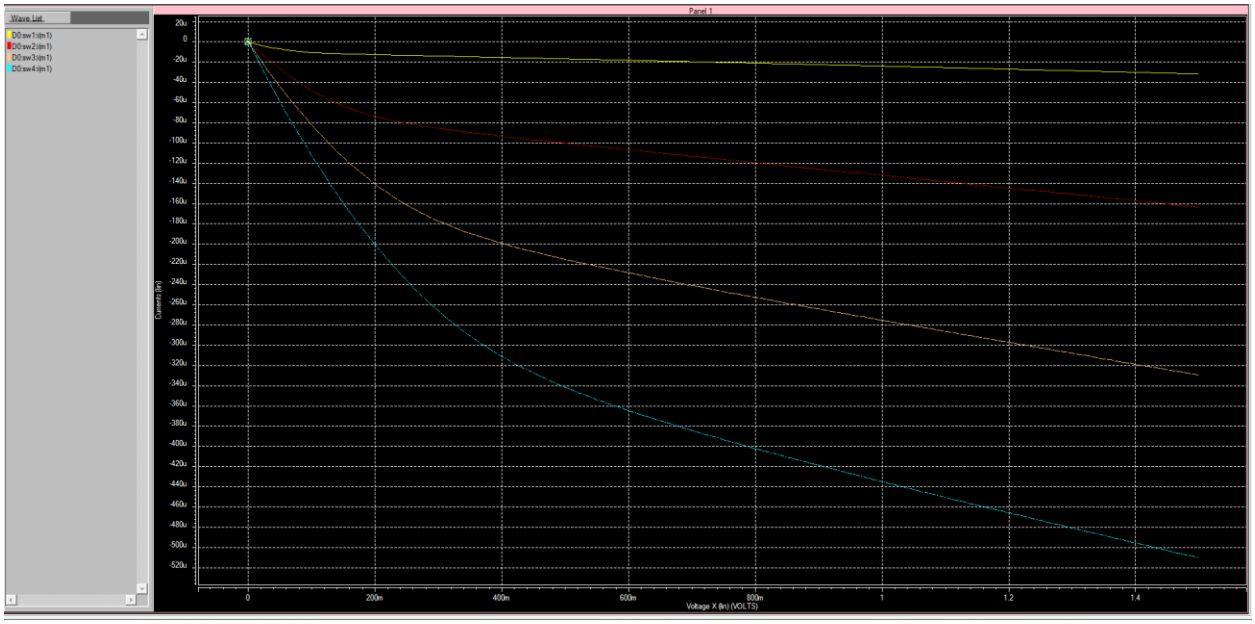
Part 1

In this section, the NMOS transistor was measured under different gate voltages. Using DC analysis, the drain–source voltage was swept from 0 to 1.5 V to obtain the graph shown below. As the gate–source voltage increases, the transistor conducts better because a larger channel is formed, improving conductivity and allowing electrons to move more freely. In the yellow curve, where the gate voltage is 0.4 V, the threshold voltage is not reached and the transistor does not turn on.

Part 2



This section is similar to the previous one, except that a PMOS transistor is used instead of NMOS. Using the *alter* command, different gate voltages were applied so that the curves can be easily compared in a single plot. Using the graphs obtained on the next page, approximate values for the requested parameters and λ were extracted.

$$I_{DS} = \frac{1}{۲} k'_n \frac{W}{L} (V_{GS} - V_{th})^۲ (1 + \lambda V_{DSA})$$

$\xrightarrow{I_{DS}=۰٫۴mA,\ V_{DS}=۱V}$ $۴\times۱۰^{-۴} = \frac{1}{۲} \times k' \times ۲۲٫۲ (۰٫۸ - V_{th})^۲ (1 + \lambda)$

λ: → شیب بعد اشباع $\qquad \lambda_n \simeq \frac{۵\times۱۰^{-۶}}{۲۰۰\times۱۰^{-۳}} = ۲٫۵\times۱۰^{-۴}\,A/V$, $\lambda_p = ۱٫۷۵\times۱۰^{-۴}\,A/V$

برای $V_G = ۰٫۸$ → $V_{DS} \simeq V_G - V_{th}$ → $V_{th} \simeq ۰٫۵V$

↲ نقطه ۳۰۰mV

حل با جایگذاری → $۴\times۱۰^{-۴} = \frac{1}{۲} k' \times (۰٫۳)^۲ (1 + ۲٫۵\times۱۰^{-۴}) \to k'_n \simeq ۴\times۱۰^{-۳}$

pmos: $V_{SD} = ۰٫۴V$, $I_{DS} = ۰٫۲mA$ → $۲\times۱۰^{-۴} = \frac{1}{۲} k'_p \times ۲۲٫۲ (۰٫۳)^۲ (1 + ۱٫۷۵\times۱۰^{-۴} \times ۰٫۴)$

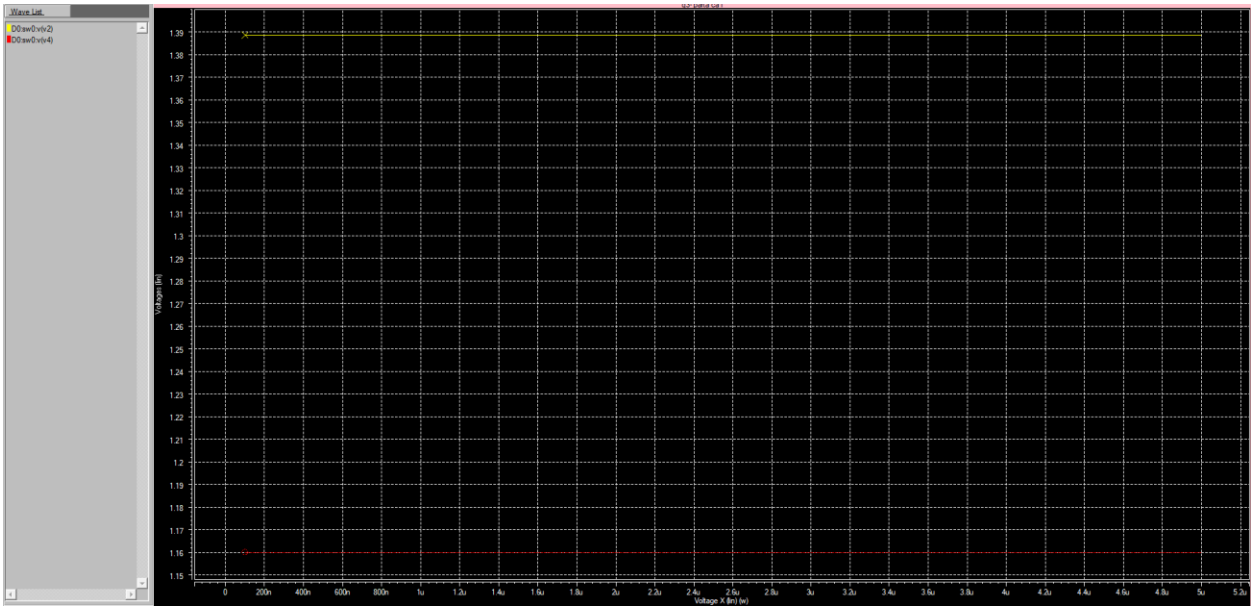
→ $k'_p = ۲\times۱۰^{-۳}$

Part 3 - section A

In this section, the circuits for parts a and b are presented.
A key characteristic of these circuits is that they are configured in such a way that all transistors, when turned on, operate in saturation mode. As the drain–source voltage increases—and since the gate voltage is also the same as the drain voltage—the current through these transistors increases according to the saturation equation.

Part 3 – section B

It is assumed that both widths (W) change together and remain equal. From the saturation equations of both transistors, after simplification, it can be seen that the W terms cancel out, resulting in an output voltage approximately equal to half of VDD. Therefore, the plot does not change.



Part 4

Since W has a direct relationship with current, when the current of the PMOS increases, its resistance decreases. Therefore, the PMOS resistance becomes smaller, causing less voltage drop across it and more voltage to appear at Vout, which leads to an increase in the output voltage. Thus, the PMOS width (W) has a direct relationship with the output voltage.