In the name of God

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Computer Assignment 3

Antenna Effect

Problem

The antenna effect or plasma induced gate oxide damage is done during plasma etching (dry etching) in manufacturing process. This charge can discharge through gate oxide and therefore can damage the gate oxide. During plasma Etching, the charges accumulated on metal or poly. Once it reaches certain potential and hence damages the gate oxide. If $\frac{exposed\ conductor\ area}{gate\ oxide\ area} >$ *Max Antenna Ratio* is true then we have antenna effect.
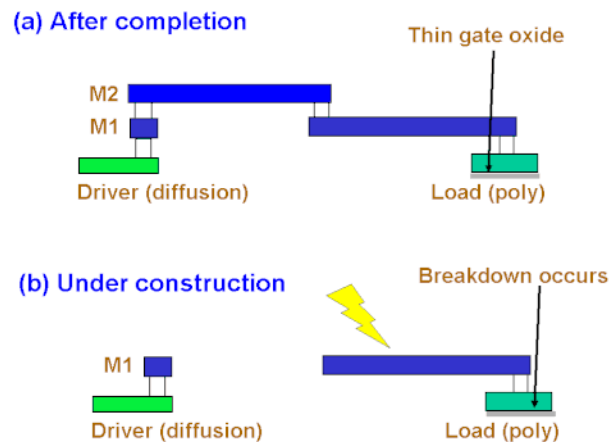

Figure 1 illustrating antenna effect

Solution

- Change the order of the routing layers. If the gate(s) immediately connects to the highest metal layer, no antenna violation will normally occur. The reason for this is because the

highest layer would be constructed at the latest and so the charge can be easily discharged through diffusion area. This solution is shown in Figure 3(a).

- Add vias near the gate(s), to connect the gate to the highest layer used. This adds more vias but involves fewer changes to the rest of the net. This is shown in Figure 3(b).
- Add diode(s) to the net, as shown in Figure 3(c). This diode should be connected to metal reversed biased so if voltage gets too high it saves gate from getting damage.
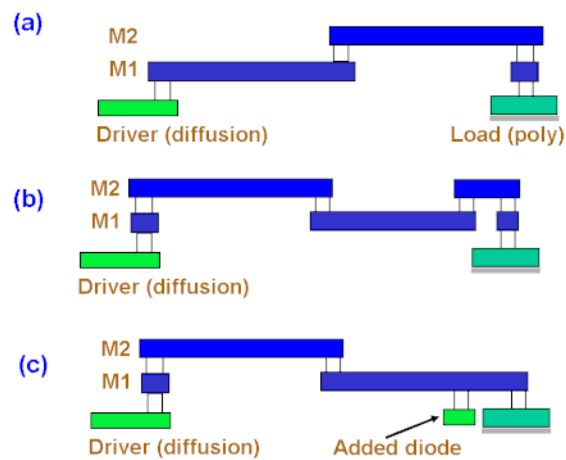

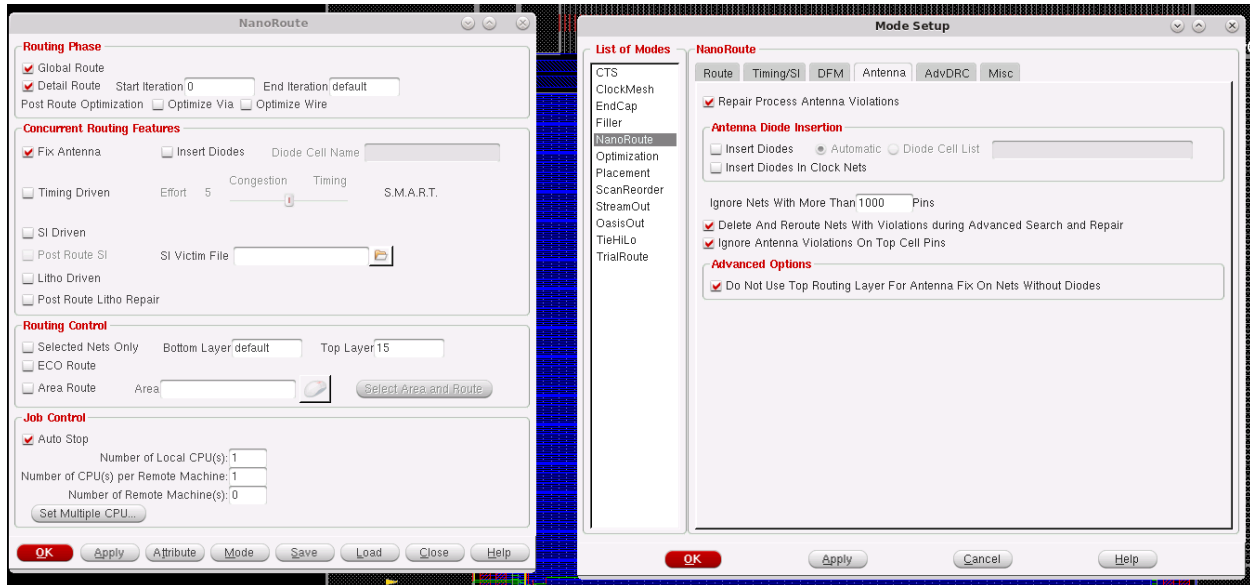*Figure 2 depicts how to fix antenna effect*

Innovus

Figure 3 Antenna setting in Innovus GUI

setNanoRouteMode options:

setNanoRouteMode options:

-drouteFixAntenna

-routeAntennaCellName

-routeAntennaPinLimit

-routeFixTopLayerAntenna

-routeIgnoreAntennaTopCellPin

-routeInsertAntennaDiode

-routeInsertDiodeForClockNets

setAttribute -nets netName -skip_antenna_fix

Example:

setNanoRouteMode -drouteFixAntenna true

setNanoRouteMode -routeAntennaCellName "ANTENNA"

setNanoRouteMode -routeInsertAntennaDiode true

globalDetailRoute

globalNetConnect

Changing the Routing

One method routers use to fix antenna violations is to limit the charge that is collected through the metal nodes exposed to the plasma. To do this, it goes up one layer or pushes the routing down one layer whenever the process antenna ratio exceeds the ratio set in the LEF file.

The router changes the routing by disconnecting nets with antenna violations and making the connections to higher metal layers instead. It does not make the connections to lower layers. This method works because the top metal layer always completes the connection from the gate to the output drain area of the driver, which is a diode that provides a discharge path.

Inserting Antenna Diode Cells

The second method routers use to repair antenna violations is to insert antenna diode cells in the design. The electrical charges on the metal that connects to the diodes is then discharged through the diode diffusion layer and substrate. The router inserts the diode cells automatically.

The following example shows a LEF definition of an antenna diode cell, with the CLASS CORE ANTENNACELL and ANTENNADIFFAREA defined:

MACRO antenna1

  CLASS CORE ANTENNACELL ;

  ...

  PIN ANT1

    AntennaDiffArea 1.0 ;

    PORT

    LAYER metal1 ;

    RECT 0.190 2.380 0.470 2.660 ;

    END

  END ANT1

END antenna1

Virtuoso

Inserting Antenna Diode Cells

There first method which manual for DRC errors file suggested is adding diodes.

	Inside DNWELL	Outside DNWELL
LV Area (Where metal line carrying low voltage (1.8V) signal, in terms of layout, there is no DV2_D layer)	1.8V N+/LVPWELL Diode (np_1p8) 1.8V P+/Nwell Diode (pn_1p8)	1.8V N+/LVPWELL Diode (np_1p8) 1.8V P+/Nwell Diode (pn_1p8)
MV Area (Where metal line carrying MV voltage (6V) signal, in terms of layout, there is DV2_D layer)	6V N+/LVPWELL Diode (np_6p0_dw) 6V P+/Nwell Diode (pn_6p0_dw)	6V N+/LVPWELL Diode (np_6p0) 6V P+/Nwell Diode (pn_6p0)
HV Area (Where metal line carrying HV voltage (30V) signal, in terms of layout, there is DV2_D and LDMOS_MK layer)	HVPDDD/DNWELL Diode (np_30p0)	Psub Diode (np_30p0)

Figure 4 diodes used as Antenna diodes

Changing the Routing

As I recall from the hands-on session, there was an ANT.3 error related to the antenna effect. In this project, I attempted to fix that issue by modifying the routing manually.
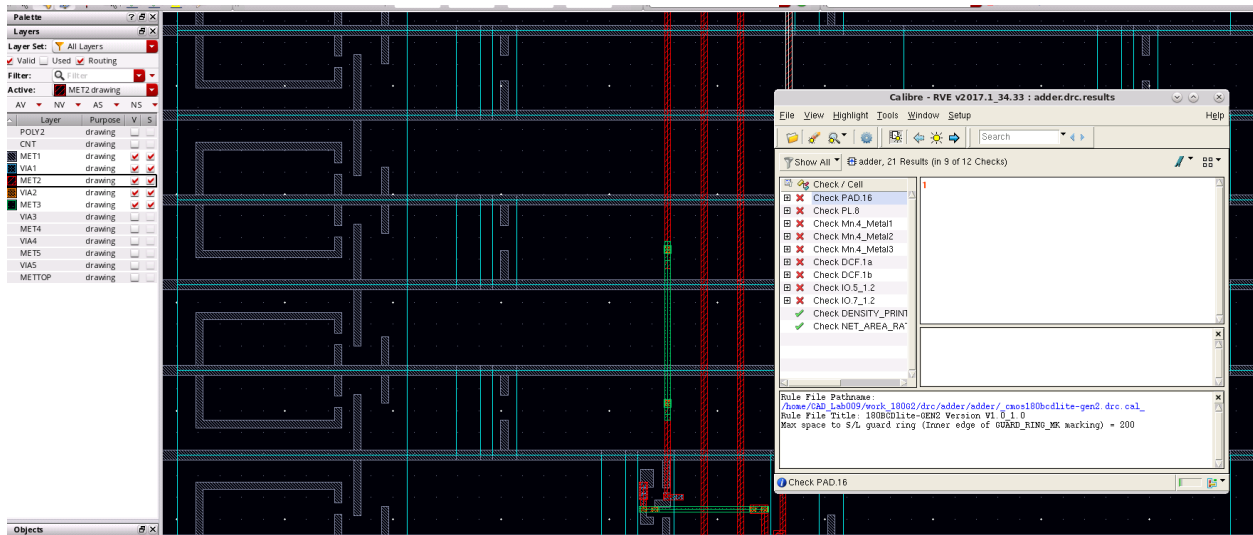
Figure 5 The immediate result
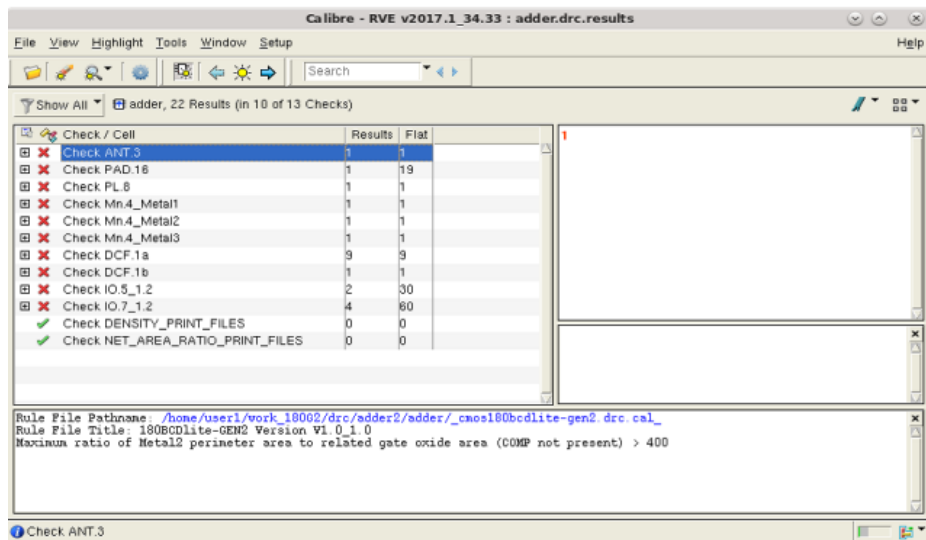
Procedure

Figure 6 All errors without any fix

There is a long metal2 that stretches from the clock IO to a DFF standard cell as illustrated in figure 7.
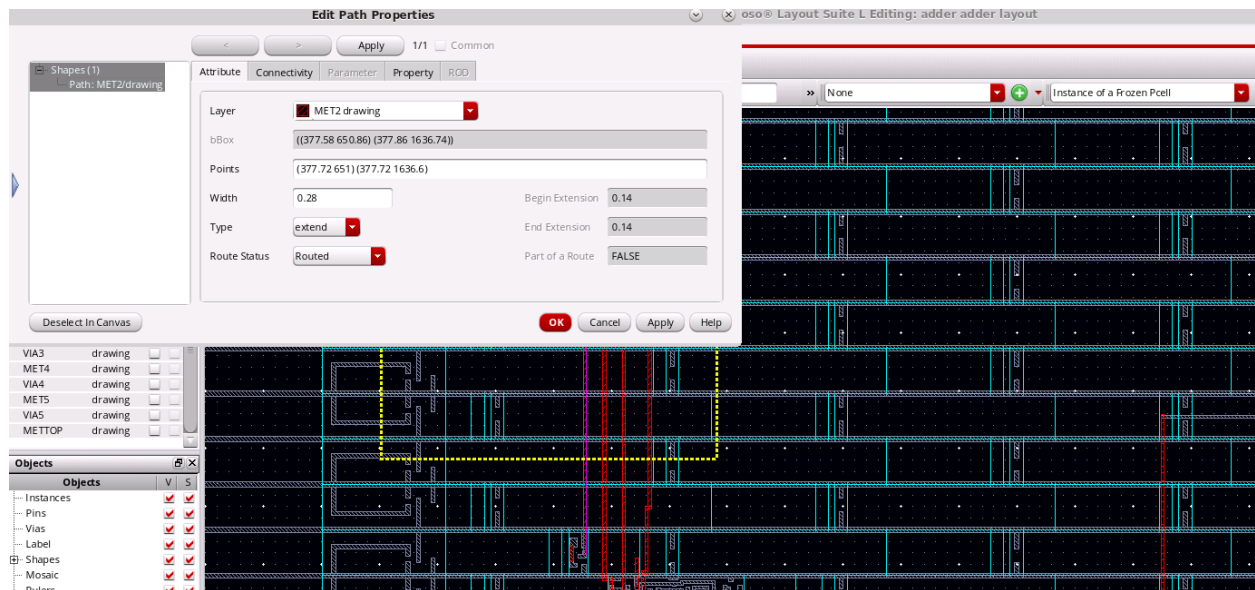

Figure 7 size and the location of routing before change

So as previously explained near where metal2(red) is connected to DFF we cut it and jump to a higher layer metal3(green). Here two visa 2-3 and a small piece of metal3 used. If before reaching the io there was a higher metal, we should continue our work to reach it. In this case it suffices. For every case if reach to the highest level (in our scenario is 5) it will always solve the problem.

How to add vias?

From top toolbar select create and select via. Then place where is needed.

How to add wires?

From top toolbar select create after that wiring and then wire. Select the start location of the wire and end point after that press enter to exit draw wiring mode. By selecting the metal and go to properties you can change the metal number to the wanted one.

Reference

- https://www.youtube.com/watch?v=da9_1-eyJnY
- https://en.wikipedia.org/wiki/Antenna_effect
- https://community.cadence.com/cadence_blogs_8/b/cic/posts/analog-layout-stop-the-antenna-effect-from-destroying-your-circuit?utm_source=chatgpt.com
- **Cadence user manual and help**
- **Virtuoso documents**