In the name of god

Implementation and test of embedded systems with ASIC

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CA2

Part A

clock	Timing (slack)	area	Dynamic Power	Leakage Power
100MHz	8.58	296.352003	38.2185 uW	27.2254 pW
200MHz	3.58	296.352003	76.4370 uW	27.2254 pW
500MHz	0.58	296.352003	191.0925 uW	27.2254 pW
5GHz	-0.55	546.603609	6.2998 mW	92.0168 pW

4-a) When we increase clock frequency, it is harder for the design compiler to meet the slack as happens in the last case that it could not meet the timing constraint and there is timing violation.

4-b) Well, as long as the design compiler can make slack upper than zero, it would not change area and power.

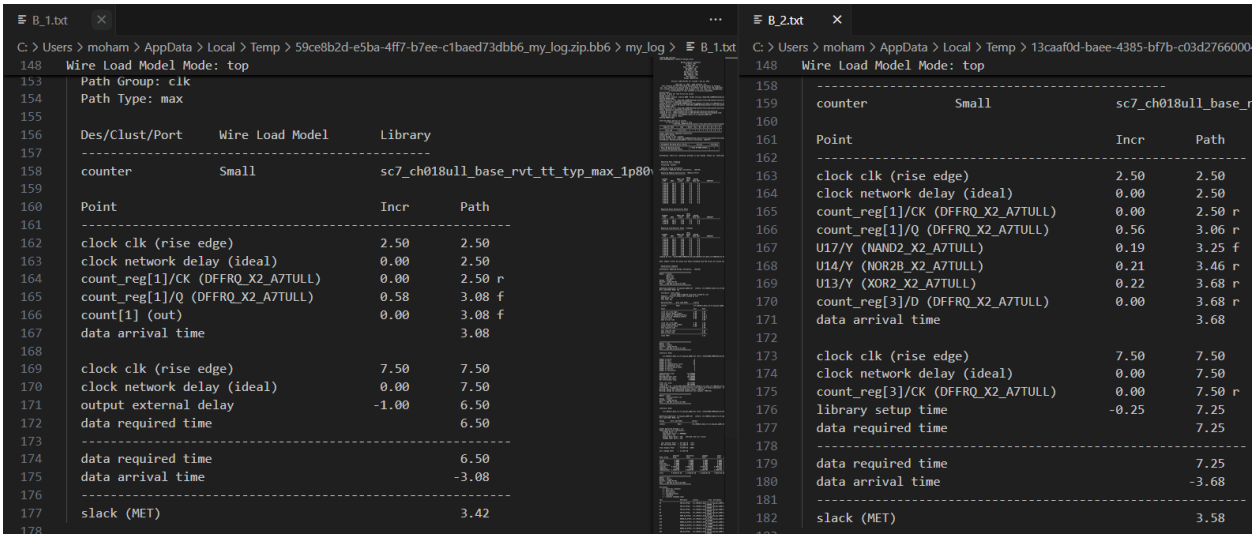
4-c) First three cases slacks are met although in last one it violates it. The design compiler in this case done it best to reach the slack with cost of more area and power but it was not enough.

4-d) As mentioned above as long as slack won't violated power won't change at all but whenever it could not meet constrains add much complex cells that would increase power and area. In the first three cases dynamic power rose linearly cause has linear relation with clock frequency.

4-e) It was addressed before, that as long as design compiler can meet slack it wont changed design but if it could not uses complex cells that increase power consumption and area.

Part B

delay	Timing (slack)	area	Dynamic Power	Leakage Power
1ns	3.42	296.352003	76.4370 uW	27.2254pW
0.2ns	3.58	296.352003	76.4370 uW	27.2254pW



B_1.txt

C: > Users > moham > AppData > Local > Temp > 59ce8b2d-e5ba-4ff7-b7ee-c1baed73dbb6_my_log.zip.bb6 > my_log > B_1.txt

```
Wire Load Model Mode: top

  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  counter            Small                 sc7_ch018ull_base_rvt_tt_typ_max_1p80

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock clk (rise edge)                    2.50       2.50
  clock network delay (ideal)              0.00       2.50
  count_reg[1]/CK (DFFRQ_X2_A7TULL)        0.00       2.50 r
  count_reg[1]/Q (DFFRQ_X2_A7TULL)         0.58       3.08 f
  count[1] (out)                           0.00       3.08 f
  data arrival time                                   3.08

  clock clk (rise edge)                    7.50       7.50
  clock network delay (ideal)              0.00       7.50
  output external delay                   -1.00       6.50
  data required time                                  6.50
  ------------------------------------------------------------
  data required time                                  6.50
  data arrival time                                  -3.08
  ------------------------------------------------------------
  slack (MET)                                        3.42
```

B_2.txt

C: > Users > moham > AppData > Local > Temp > 13caaf0d-baee-4385-bf7b-c03d2766000

```
Wire Load Model Mode: top

  ------------------------------------------------
  counter            Small                 sc7_ch018ull_base_r

  Point                                    Incr       Path
  ------------------------------------------------------------
  clock clk (rise edge)                    2.50       2.50
  clock network delay (ideal)              0.00       2.50
  count_reg[1]/CK (DFFRQ_X2_A7TULL)        0.00       2.50 r
  count_reg[1]/Q (DFFRQ_X2_A7TULL)         0.56       3.06 r
  U17/Y (NAND2_X2_A7TULL)                  0.19       3.25 f
  U14/Y (NOR2B_X2_A7TULL)                  0.21       3.46 r
  U13/Y (XOR2_X2_A7TULL)                   0.22       3.68 r
  count_reg[3]/D (DFFRQ_X2_A7TULL)         0.00       3.68 r
  data arrival time                                   3.68

  clock clk (rise edge)                    7.50       7.50
  clock network delay (ideal)              0.00       7.50
  count_reg[3]/CK (DFFRQ_X2_A7TULL)        0.00       7.50 r
  library setup time                      -0.25       7.25
  data required time                                  7.25
  ------------------------------------------------------------
  data required time                                  7.25
  data arrival time                                  -3.68
  ------------------------------------------------------------
  slack (MET)                                        3.58
```

3-a) In this case I/O delays do not affect our design so much to make them negative. so, nothing changed. But if delay increases it might change area and power to achieve positive slack.

3-b) Nothing has changed cause there is no pressure on slack so design compiler didn’t change the design.

3-c) There is no violation here.

3-d) There is no difference between two designs.

B_1.txt

C: > Users > moham > AppData > Local > Temp > 59ce8b2d-e5ba-4ff7-b7ee-c1baed73dbb6_my_log.zip.bb6 > my_log > B_1.txt

```
Attributes:
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                    Reference       Library             Area  Attributes
--------------------------------------------------------------------------------
U3                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            6.585600  d
U4                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            6.585600  d
U5                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            6.585600  d
U6                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            6.585600  d
U13                     XOR2_X2_A7TULL  sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            19.756800
U14                     NOR2B_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            10.976000
U15                     XNOR2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            19.756800
U16                     XNOR2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            19.756800
U17                     NAND2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            8.780800
U18                     INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            6.585600
count_reg[0]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            46.099201 n
count_reg[1]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            46.099201 n
count_reg[2]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            46.099201 n
count_reg[3]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            46.099201 n
--------------------------------------------------------------------------------
Total 14 cells                                              296.352003
design_vision> Current design is 'counter'.
```

B_2.txt

C: > Users > moham > AppData > Local > Temp > 13caaf0d-baee-4385-bf7b-c03d27660004_my_log.zip.004 > my_log

```
Attributes:
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                    Reference       Library             Area  Attributes
--------------------------------------------------------------------------------
U3                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            6.585600  d
U4                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            6.585600  d
U5                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            6.585600  d
U6                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            6.585600  d
U13                     XOR2_X2_A7TULL  sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            19.756800
U14                     NOR2B_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            10.976000
U15                     XNOR2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            19.756800
U16                     XNOR2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            19.756800
U17                     NAND2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            8.780800
U18                     INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            6.585600
count_reg[0]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            46.099201 n
count_reg[1]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            46.099201 n
count_reg[2]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            46.099201 n
count_reg[3]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                            46.099201 n
--------------------------------------------------------------------------------
Total 14 cells                                              296.352003
design_vision> Current design is 'counter'.
```

Part C

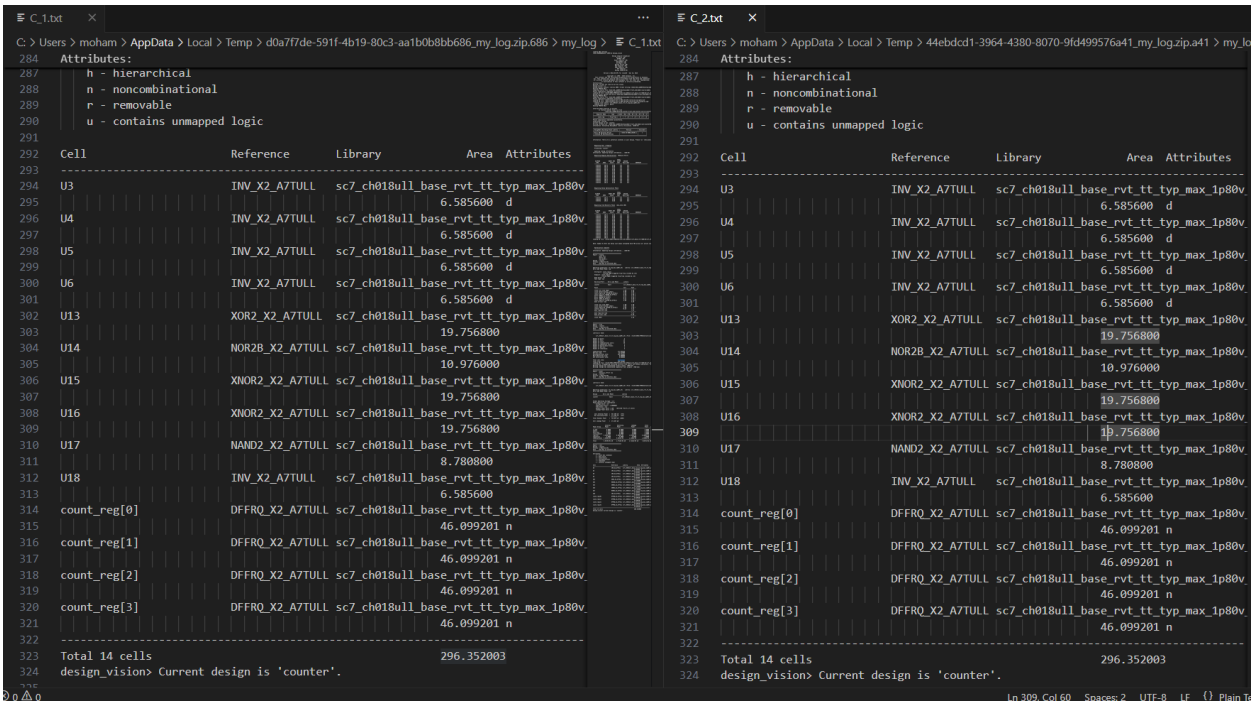
	Timing (slack)	area	Dynamic Power	Leakage Power
100%	3.58	296.352003	76.4370 uW	27.2254 pW
80%	3.58	296.352003	76.4370 uW	27.2254 pW

3-a) For this case our design is too small. so basically, design compiler done its best and cannot optimize it more and make it smaller. So, there are no changes.

3-b) As addressed in last part in this case there is no trade-off. However, in larger design it might be possible to affect timing and make it worse.

3-c) If the design was larger, it might be!

3-d) As the illustration below states there are no changes.



C_1.txt

```
Attributes:
    h - hierarchical
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                    Reference       Library             Area  Attributes
--------------------------------------------------------------------------------
U3                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          6.585600  d
U4                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          6.585600  d
U5                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          6.585600  d
U6                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          6.585600  d
U13                     XOR2_X2_A7TULL  sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         19.756800
U14                     NOR2B_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         10.976000
U15                     XNOR2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         19.756800
U16                     XNOR2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         19.756800
U17                     NAND2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          8.780800
U18                     INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          6.585600
count_reg[0]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         46.099201 n
count_reg[1]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         46.099201 n
count_reg[2]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         46.099201 n
count_reg[3]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         46.099201 n
--------------------------------------------------------------------------------
Total 14 cells                                          296.352003
design_vision> Current design is 'counter'.
```

C_2.txt

```
Attributes:
    h - hierarchical
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                    Reference       Library             Area  Attributes
--------------------------------------------------------------------------------
U3                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          6.585600  d
U4                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          6.585600  d
U5                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          6.585600  d
U6                      INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          6.585600  d
U13                     XOR2_X2_A7TULL  sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         19.756800
U14                     NOR2B_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         10.976000
U15                     XNOR2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         19.756800
U16                     XNOR2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         19.756800
U17                     NAND2_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          8.780800
U18                     INV_X2_A7TULL   sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                          6.585600
count_reg[0]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         46.099201 n
count_reg[1]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         46.099201 n
count_reg[2]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         46.099201 n
count_reg[3]            DFFRQ_X2_A7TULL sc7_ch018ull_base_rvt_tt_typ_max_1p80v
                                                         46.099201 n
--------------------------------------------------------------------------------
Total 14 cells                                          296.352003
design_vision> Current design is 'counter'.
```