UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Implementation and test of embedded systems with ASIC

ECE (8111) 002 – Spring 1403-04

Computer Assignment 2: Exploring Synthesis Constraints in ASIC Design

Due Date: Ordibehesht 25

In this assignment, you will explore how varying synthesis constraints affect the final implementation of a digital design when synthesized using **Synopsys Design Compiler**. You will work with a pre-defined Verilog design and modify constraint files to observe changes in **timing, area, and power**. This assignment will help you develop a practical understanding of the trade-offs that synthesis tools make when trying to meet tighter or looser design goals.

Part A: Timing Constraints

1. Start with the provided design of a counter in the *counter.v* Verilog file. First, import and prepare the design in Design Compiler using the appropriate steps to analyze and elaborate the RTL. Briefly describe the structure and functionality of the counter based on your understanding from the source code and elaborated design using generated schematic in DC.
2. Create and apply three different clock constraints using SDC files:
    a. A clock with a **10 ns** period (100 MHz)
    b. A clock with a **5 ns** period (200 MHz)
    c. A clock with a **2 ns** period (500 MHz)
3. For each clock constraint, perform synthesis using DC, and extract the following results from the synthesis reports:
    a. Timing results: Slack, critical path delay (from report_timing)
    b. Area results: Total cell area and total area (from report_area)
    c. Power results: Total power consumption (from report_power)
4. After collecting the data for all three constraints, compare the results. Specifically, discuss:
    a. How the synthesis results differ as the clock constraint becomes tighter?
    b. Why the area increases or decreases?
    c. Whether timing is met or violated in each case, and why?

    d. How power consumption is affected by the tighter clock?
    e. What design trade-offs the synthesis tool appears to be making in each scenario?
5. Present your findings in a brief report that includes:
    a. A table summarizing timing, area, and power for all three cases.
    b. A discussion with clear reasoning explaining the differences observed.

Part B: Input and Output Delay Constraints

1. Using the adder design in *counter.v* Verilog file, modify the synthesis constraints to explore the effect of I/O delay constraints. Create and apply at least two different sets of *set_input_delay* and *set_output_delay* values:

    a. Input delay = 1 ns, Output delay = 1 ns
    b. Input delay = 0.2 ns, Output delay = 0.2 ns

    Keep the clock constraint fixed (e.g., 5 ns) for both cases.

2. For each case, perform synthesis and extract:

    a. Timing results: Slack, hold/setup violations
    b. Area results: Total cell area
    c. Power results

3. Analyze and compare the results:

    a. How does tightening the I/O delays affect synthesis outcome?
    b. Is there an increase in area to meet the tighter I/O delays?
    c. Are there any timing violations in either case?
    d. Compare the types and sizes of cells used in each case. Do you observe any change in the types or drive strengths of logic cells selected by the tool? Does the tighter constraint lead to usage of faster or larger cells? (Hint: Use *report_cell* or examine the synthesized netlist and cell summary to investigate.)

4. Present your findings:

    a. A table summarizing slack, area, and power.
    b. A brief explanation of how and why synthesis results changed based on I/O constraints.

Part C: Area Constraint Exploration

1. Using the adder design in the *adder.v* Verilog file, modify the synthesis constraints to explore the effect of area limitations. Create and apply at least two different values of set_max_area:
    a. set_max_area equal to **100%** of the area from unconstrained synthesis (baseline)
    b. set_max_area set to **80%** of that value (stricter constraint)

    Keep the clock constraint fixed (e.g., 5 ns) for both cases. Use the same input and output delay values as used previously.

2. For each case, perform synthesis and extract:
    a. Timing results: Slack, setup/hold violations
    b. Area results: Total cell area
    c. Power results: Dynamic and leakage power
3. Analyze and compare the results:
    a. How does tightening the area constraint affect the synthesis outcome?
    b. Does the tool make timing trade-offs to meet the area target?
    c. Are there any timing violations (especially slack degradation) due to area limitation?
    d. Compare the types and drive strengths of cells used in each case. Do you observe a shift from faster (larger) cells to smaller/slower ones in the tighter constraint scenario?
    (Hint: Use report_cell, report_area, or inspect the synthesized netlist.)
4. Present your findings:
    a. A table summarizing **Slack**, **Total Area**, and **Power** for both area constraints.
    b. A short explanation of how synthesis results changed under area constraints:
        - What changed in the netlist?
        - Were slower/simpler cells used?
        - Was timing affected?
        - Was power reduced or increased?

Deliverables:

You are required to submit a report that includes the following:

1. **Section-wise documentation** for all parts of the assignment (Part A, Part B, and Part C), including:
    - A brief explanation of your synthesis setup and applied constraints
    - Tables summarizing results (timing, area, power) for each scenario
    - Screenshots of key synthesis reports (e.g., timing paths, area breakdown)
    - For Part A and B: Comparison of results across different constraint values, along with your analysis and reasoning
    - For Part B: Cell-level comparison between the two I/O delay scenarios
    - For Part C: Description of the exception used (multicycle or false path), how it affects results, and when such exceptions should be used in practice
2. **Result Tables** for each part with clearly labeled columns for:
    - Constraint values
    - Slack / delay
    - Total cell area
    - Power consumption
    - Additional observations (e.g., cell types used)
3. **Discussion Section** where you reflect on the following:
    - How constraints influence synthesis trade-offs
    - The relationship between timing, area, and power
    - Insights or challenges faced during synthesis and report interpretation
4. (Optional) **Bonus**: If you explore additional constraints or test cases beyond those required, include them in a separate section labeled “Bonus Work.”

Great designs, like great minds, grow stronger under pressure—keep pushing your limits!