UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Implementation and test of embedded systems with ASIC

ECE (8111) 002 – Spring 1403-04

Computer Assignment 3: Exploring PnR Tools in ASIC Design

Due Date: Khordad 24

In this computer assignment, you will explore and analyze the **features of Place and Route (P&R) tools** used in ASIC design. The goal is to understand each feature in depth, how it operates within the design flow, and how it can be used effectively in real-world scenarios.

Each student will be assigned one specific feature or stage of the Place and Route process to investigate. You are expected to use industry-standard tools (**Cadence Innovus and Cadence Virtuoso**) and study the feature both theoretically and practically.

Features/Stages to be Explored:

1. **Analysis of Physical Cells: Endcap, Filler, IO Filler, and Well Tap Cells**
   An in-depth study of essential physical cells used in ASIC layout design. This includes their purpose, material composition, functional differences, and specific layout constraints, such as IO power connectivity and row-level well tap cell placement strategies.

2. **In-Depth Analysis of Placement in ASIC Design**
   Explore the placement stage in ASIC physical design, including available placement algorithms, command-line and GUI-based configuration in Cadence Innovus, and how different placement strategies affect timing, power, and congestion.

3. **Clock Tree Synthesis (CTS) and Its Impact on Timing and Skew**
   A comprehensive study of the CTS process, including CTS engines, clock buffer insertion, clock tree styles, useful skew optimization, and analysis of how CTS affects overall chip performance and clock domain balancing.

4. **Routing Strategies and Analysis in ASIC Layout**
   Examine the routing stage, including global and detailed routing methods, DRC rule adherence, congestion-aware routing, and evaluation of how routing options impact timing closure and physical integrity.

5. **Power Planning**
   Analyze various power distribution strategies such as power rings, and power stripes. Study the setup of power domains and the use of related commands to ensure proper power integrity across the chip.

6. **Floorplanning Techniques and Optimization**
   Investigate floorplanning methods including macro placement, IO pad arrangement, and standard cell row generation. Evaluate the impact of floorplan quality on downstream stages such as placement, CTS, and routing.

7. **Placement Blockage and Halo Definitions for Macro and IO Isolation**
   Understand the role of placement blockages (hard and soft) and halo definitions in maintaining routing and placement integrity near large macros and IO cells. Learn how to define and configure these regions effectively.

8. **Design Rule Checking (DRC) in the Physical Implementation Flow**
   Explore the role of Design Rule Checking (DRC) in the place and route flow. Learn how DRC verifies layout compliance with foundry rules, how violations are detected and reported during different stages, and the methods to resolve these violations to ensure manufacturability.

9. **Layout vs. Schematic (LVS) in the Physical Implementation Flow**
   Investigate the integration of Layout vs. Schematic (LVS) verification within the physical implementation process. Understand how LVS ensures that the final layout matches the original circuit schematic, the detection and reporting of mismatches, and how these issues are fixed before tape-out.

10. **Antenna Effect Prevention and Fixing during Routing**
    Study the antenna effect caused by long metal traces during fabrication. Learn prevention and fixing techniques such as diode insertion or route fragmentation and how to enable these features in routing tools.

11. **Scan Chain Reordering and Placement Considerations for DFT**
    Investigate scan chain design in the context of physical layout. Understand how placement decisions and chain reordering influence test timing, wirelength, and routing congestion.

12. **Utilization and Congestion Analysis Throughout the Flow**
    Study how to monitor and analyze cell utilization and routing congestion. Learn how to

identify problematic regions (hotspots) and how placement or floorplanning changes can improve physical metrics.

Deliverables:

1. A **detailed report** explaining:
    - What the assigned feature does in the context of ASIC P&R.
    - Its **role and significance** in the overall flow.
    - **Commands**, scripts, or GUI paths used to activate or configure it.
    - Various **modes, options, and settings** available for that feature.
2. A **hands-on exploration** using a sample design:
    - Apply the feature under **different configurations** or modes.
    - Report and compare **how these different settings affect** the outcome (e.g., timing, area, congestion).
    - Include screenshots, plots, or any evidence to support your observations.
3. The report must be clearly organized, technically accurate, and properly referenced (if you use external resources).

As this is your final assignment for this course and the semester, it is expected to reflect the depth of your understanding, attention to detail, and the practical skills you have developed throughout the term. ***Make it count.***