In the name of God

Digital Electronics

CA5

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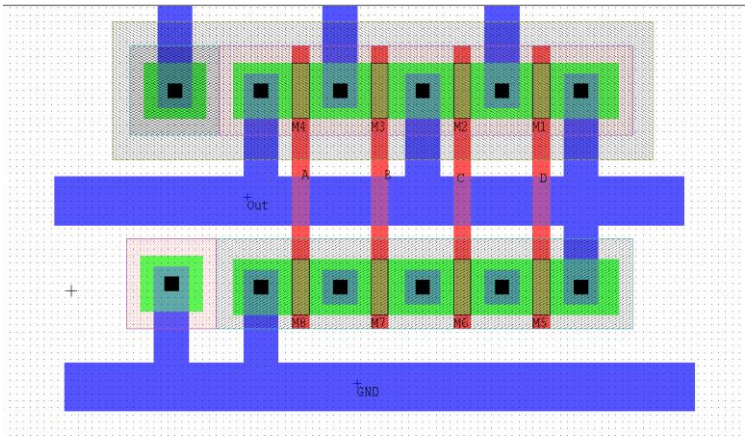
Part 1

1)

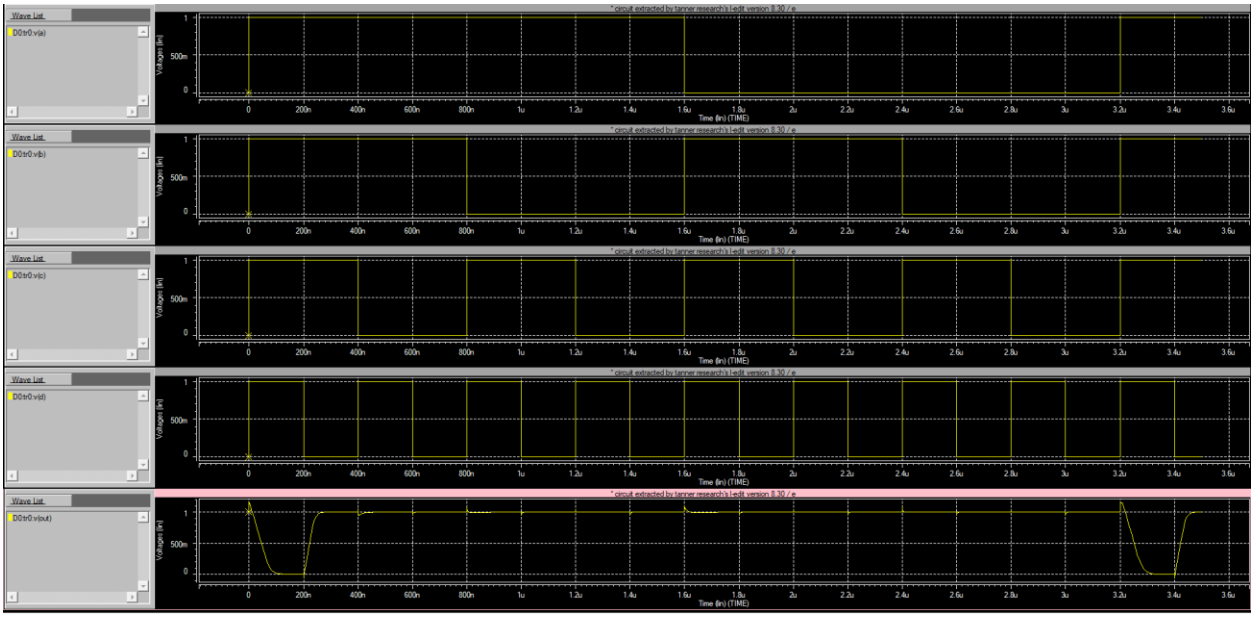



```
Cpar1 GND 0 C=131.196f
Cpar2 Out 0 C=283.612f
Cpar3 VDD 0 C=204.246f
Cpar4 4 0 C=39.564f
Cpar5 5 0 C=41.712f
Cpar6 6 0 C=39.564f
* Warning: Node A has zero nodal parasitic capacitance.
* Warning: Node B has zero nodal parasitic capacitance.
* Warning: Node C has zero nodal parasitic capacitance.
* Warning: Node D has zero nodal parasitic capacitance.

M1 Out D VDD VDD PMOS L=2.5u W=8u AD=80p PD=36u AS=36p PS=17u
* M1 DRAIN GATE SOURCE BULK (67 25 69.5 33)
M2 VDD C Out VDD PMOS L=2.5u W=8u AD=36p PD=17u AS=38p PS=17.5u
* M2 DRAIN GATE SOURCE BULK (55.5 25 58 33)
M3 Out B VDD VDD PMOS L=2.5u W=8u AD=38p PD=17.5u AS=36p PS=17u
* M3 DRAIN GATE SOURCE BULK (43.5 25 46 33)
M4 VDD A Out VDD PMOS L=2.5u W=8u AD=36p PD=17u AS=68p PS=33u
* M4 DRAIN GATE SOURCE BULK (32 25 34.5 33)
M5 Out D 4 GND NMOS L=2.5u W=8u AD=80p PD=36u AS=36p PS=17u
* M5 DRAIN GATE SOURCE BULK (67 -3.5 69.5 4.5)
M6 4 C 5 GND NMOS L=2.5u W=8u AD=36p PD=17u AS=38p PS=17.5u
* M6 DRAIN GATE SOURCE BULK (55.5 -3.5 58 4.5)
M7 5 B 6 GND NMOS L=2.5u W=8u AD=38p PD=17.5u AS=36p PS=17u
* M7 DRAIN GATE SOURCE BULK (43.5 -3.5 46 4.5)
M8 6 A GND GND NMOS L=2.5u W=8u AD=36p PD=17u AS=68p PS=33u
* M8 DRAIN GATE SOURCE BULK (32 -3.5 34.5 4.5)

* Total Nodes: 10
* Total Elements: 14
* Total Number of Shorted Elements not written to the SPICE file: 0
* Extract Elapsed Time: 0 seconds
```

The **L-Edit output code** is shown above, indicating the **capacitors**

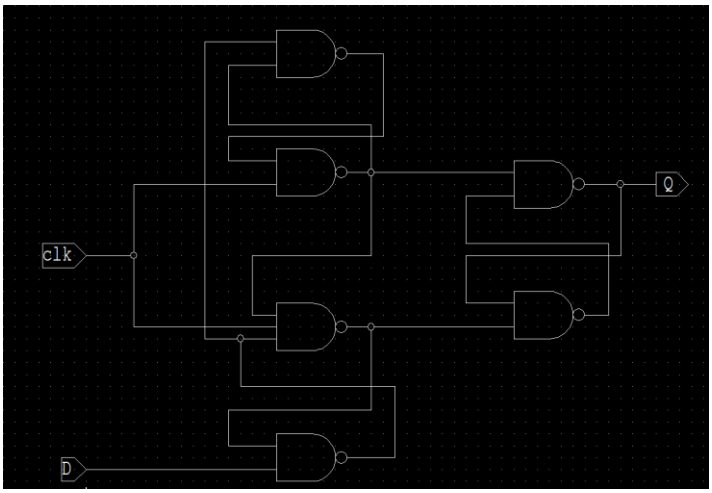
and the **W and L** of the transistors.

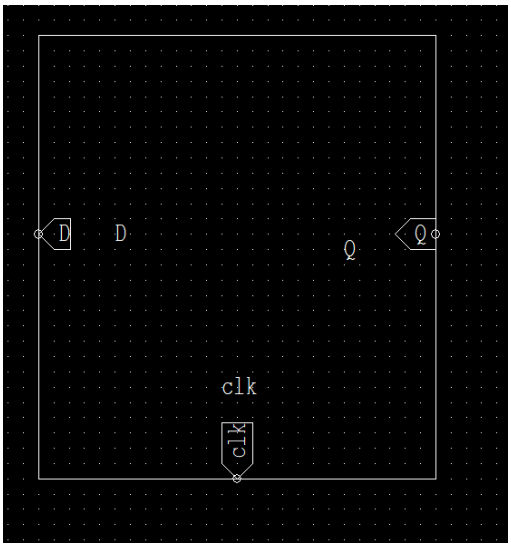
2)



Part 2

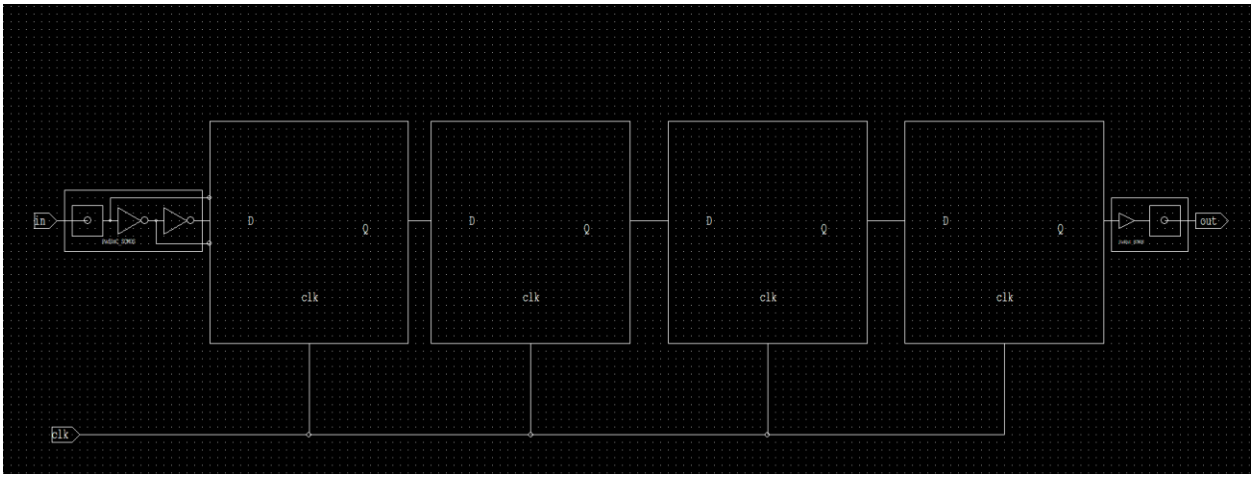
1)





This flip-flop is constructed using **NAND gates**, which are **zero-sensitive**. When the clock is **0**, the two gates connected to the clock always output **1**, causing the latch connected to the output to form **two NOT gates in series** and hold its internal data. When the clock becomes **1**, if **data = 0**, the lower latch outputs **0** to the front latch, and the upper latch transfers a **1**. If **data = 1**, the upper latch outputs **0**, and the lower latch, once it becomes stable, transfers **1** to the front latch. Based on this behavior, this flip-flop is **positive-edge triggered**.

2)



3)