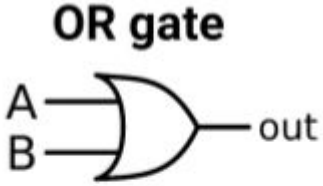
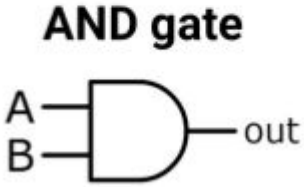


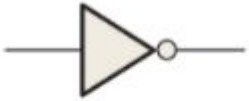


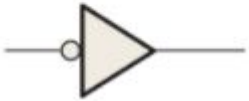
Logic Gates

Chapter 3

Sumaiyah Zahid

Inverter Or NOT Gate



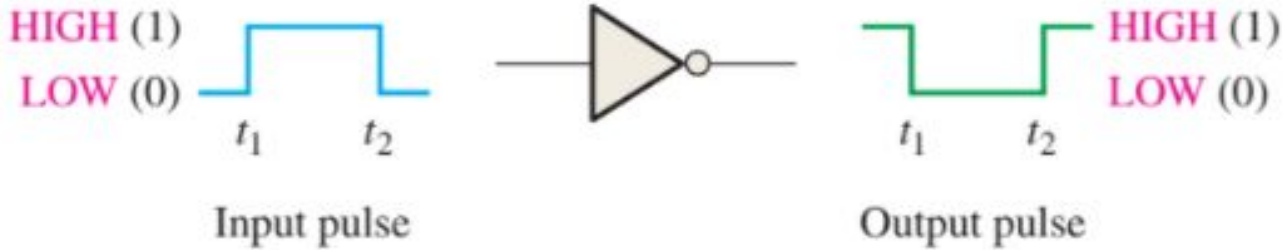


Complementation

TABLE 3–1

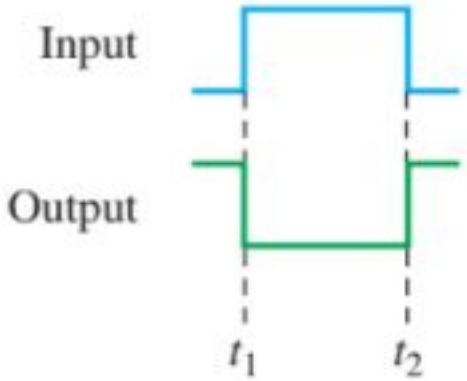
Inverter truth table.

Input	Output
LOW (0)	HIGH (1)
HIGH (1)	LOW (0)



Inverter Timing Diagram

A timing diagram shows how two or more waveforms relate in time.



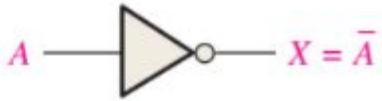


FIGURE 3–6 The inverter complements an input variable.

AND Gate

A	B	
0	0	0
1	0	0
0	1	0
1	1	1

AND Gate = Boolean Multiplication

AND Gate

(a) Develop the truth table for a 3-input AND gate.

(b) Determine the total number of possible input combinations for a 4-input AND gate.

AND Gate

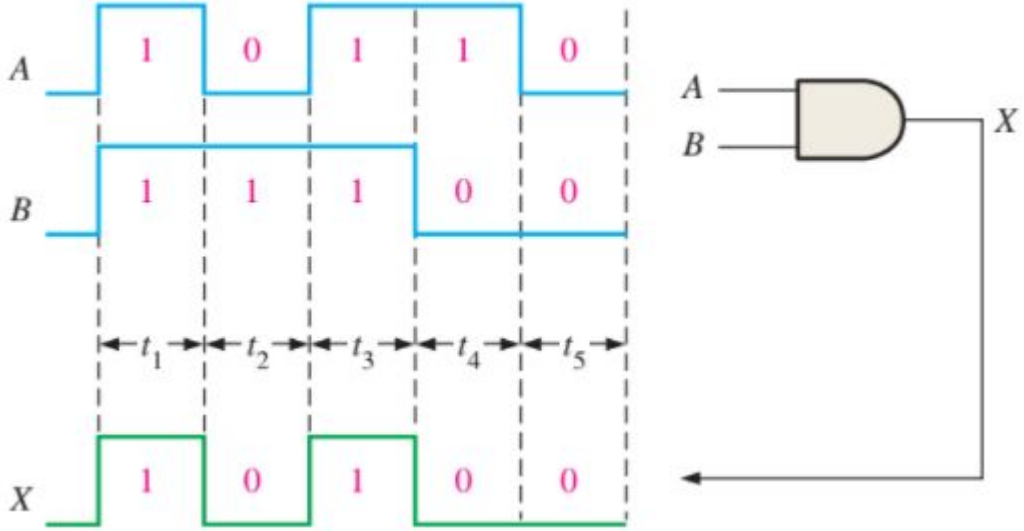
(a) Develop the truth table for a 3-input AND gate.

(b) Determine the total number of possible input combinations for a 4-input AND gate.

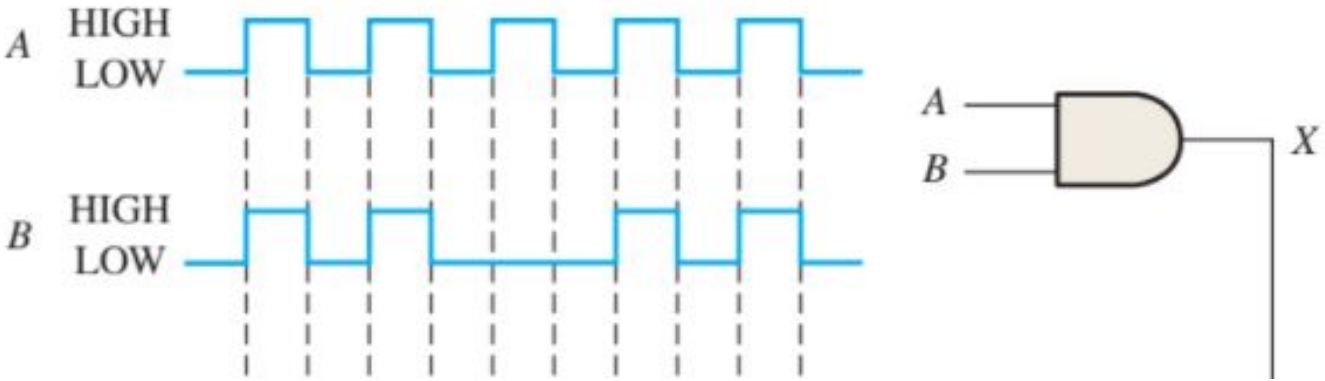
TABLE 3–3

Inputs			Output
A	*B*	*C*	*X*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

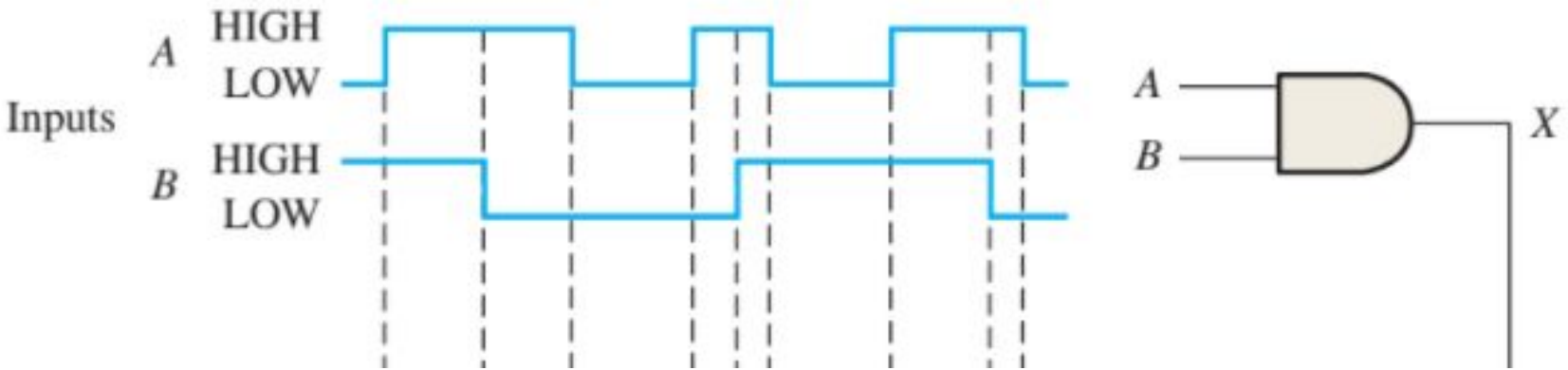
AND Gate Timing Diagram



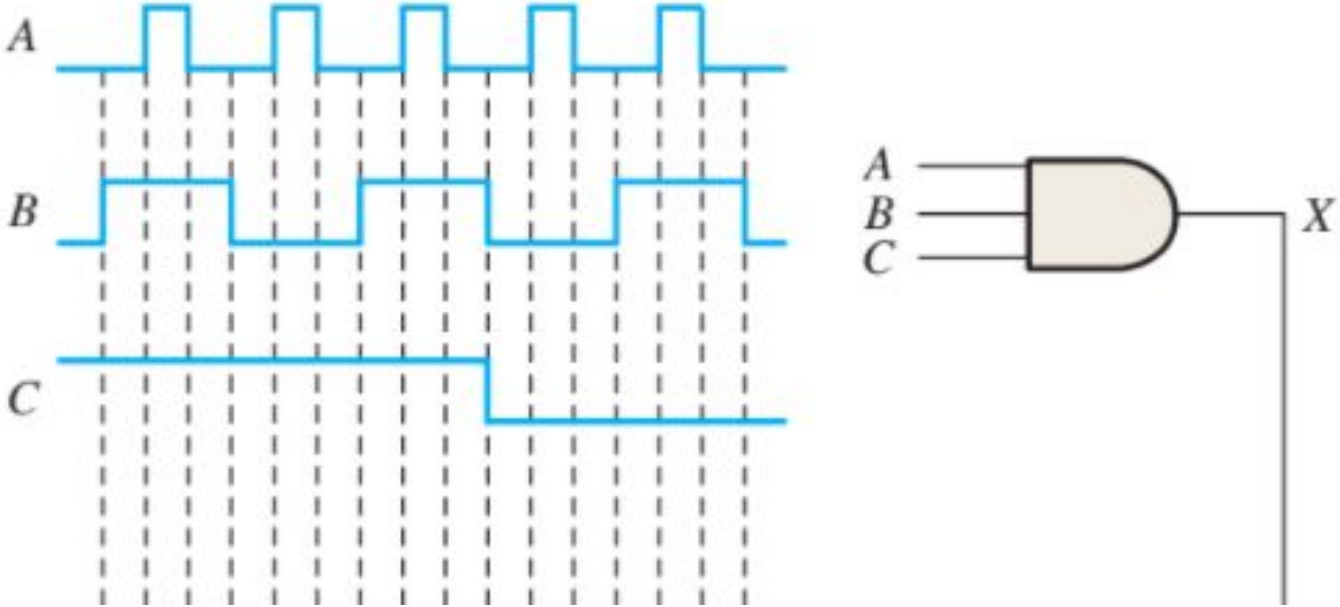
AND Gate Timing Diagram



AND Gate Timing Diagram



AND Gate Timing Diagram



AND Gate

Boolean multiplication is the same as the AND function.

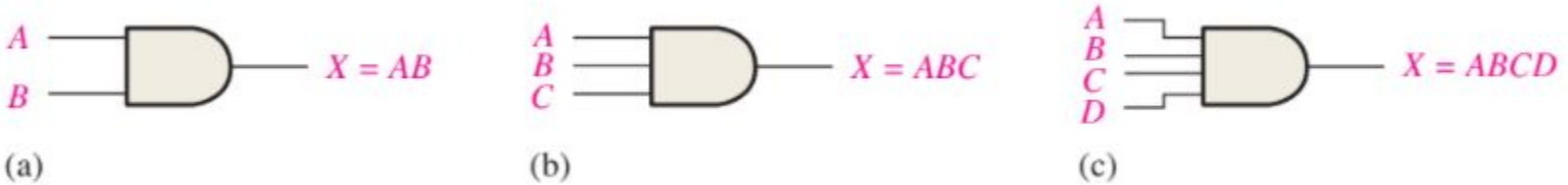


FIGURE 3–15 Boolean expressions for AND gates with two, three, and four inputs.

AND Gate Application

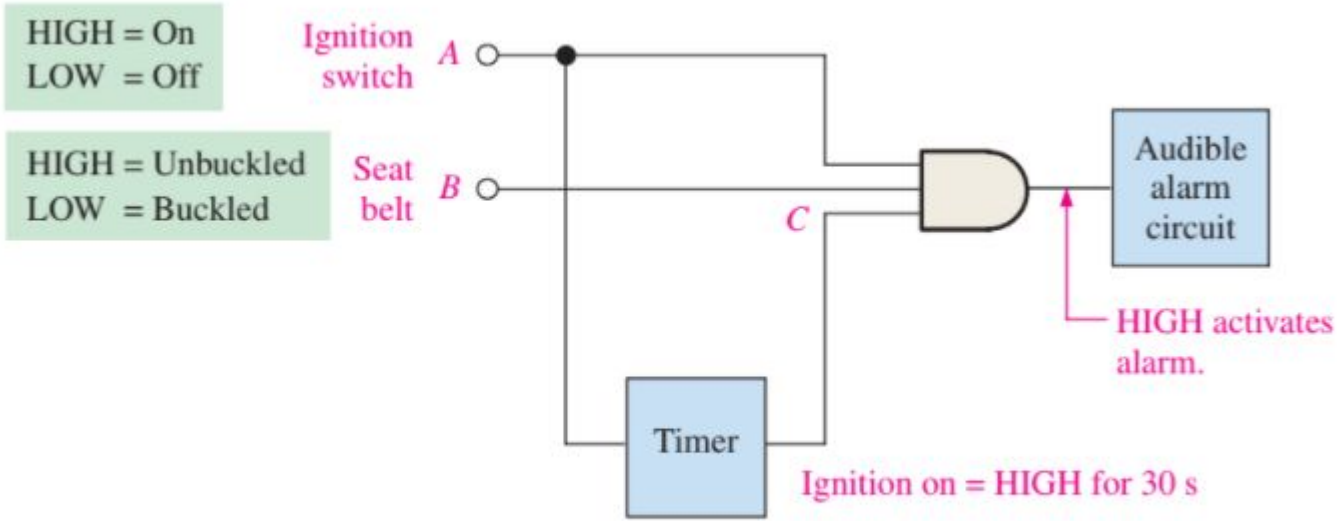


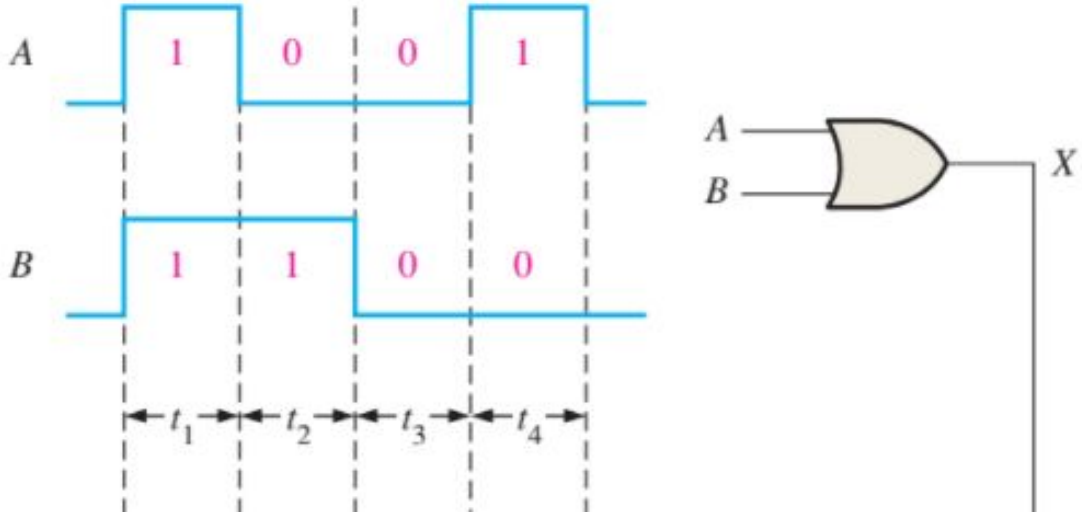
FIGURE 3–17 A simple seat belt alarm circuit using an AND gate.

OR Gate

OR Gate = Boolean Addition

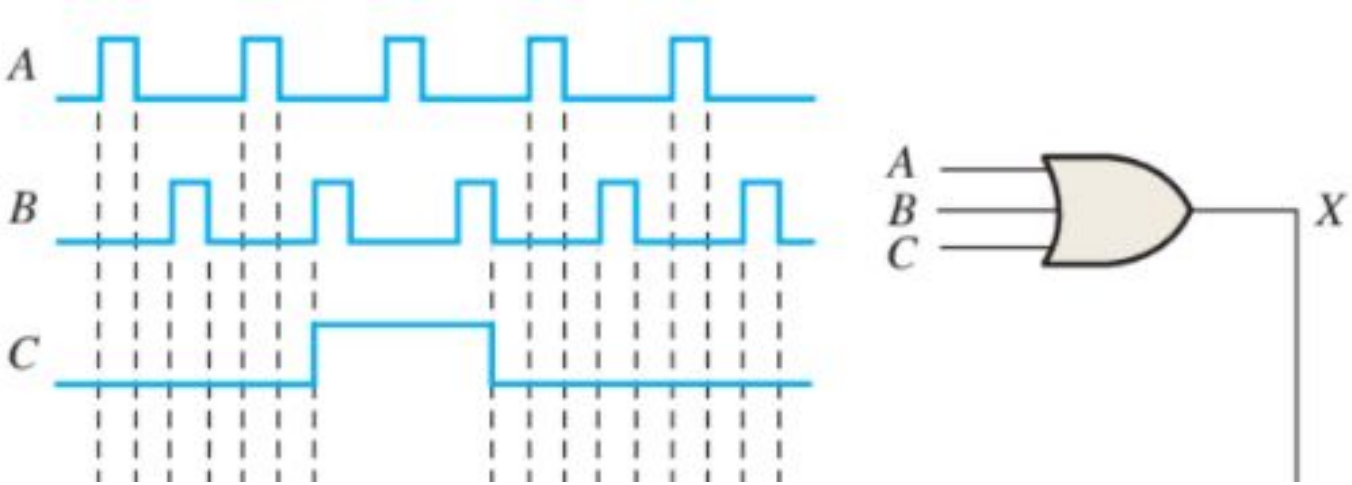
INPUT		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	1

OR Gate Timing Diagram



OR Gate Timing Diagram

OR Gate Timing Diagram



OR Gate

Boolean addition is the same as the OR function.

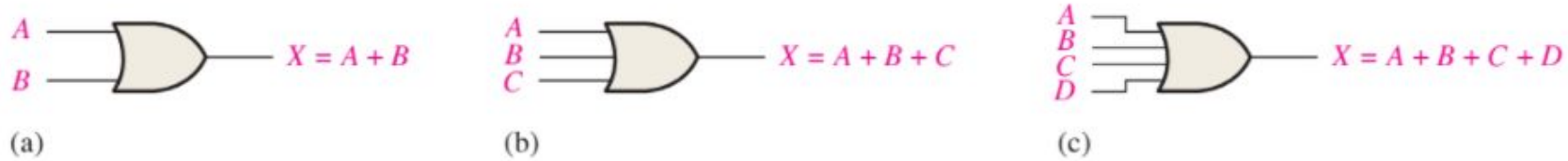


FIGURE 3–24 Boolean expressions for OR gates with two, three, and four inputs.

OR Gate Application

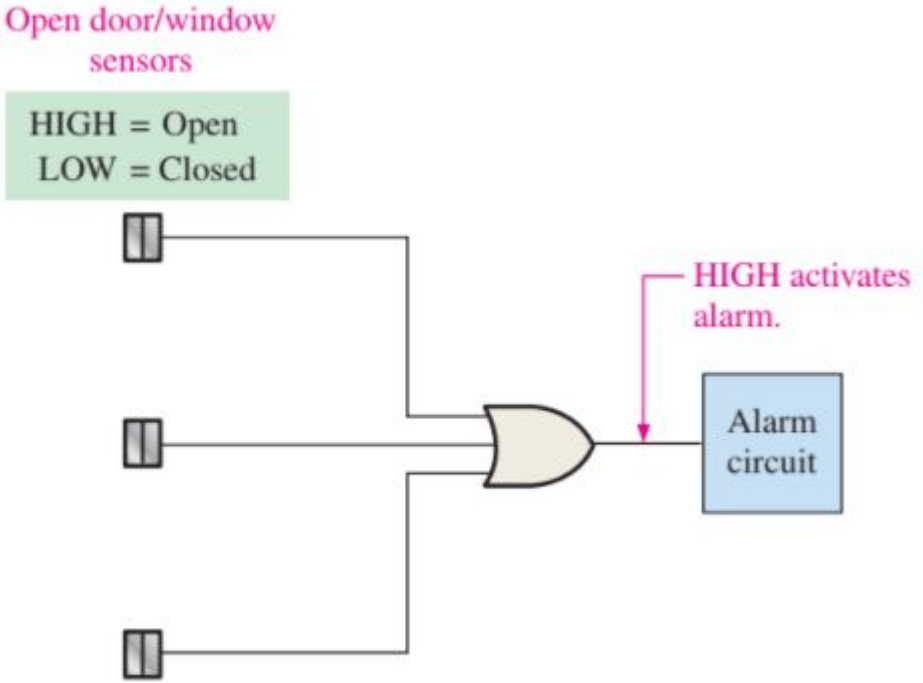


FIGURE 3–25 A simplified intrusion detection system using an OR gate.

NAND Gate

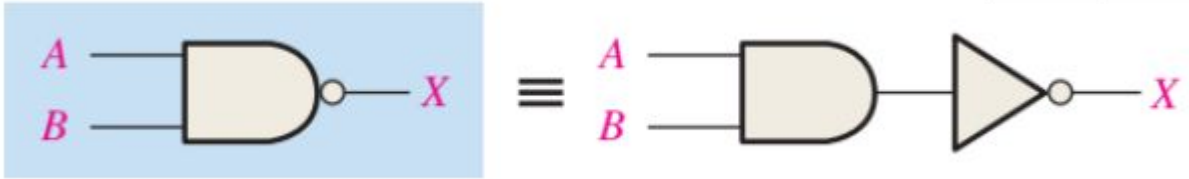
NAND = Not AND

Also known as Universal Gate

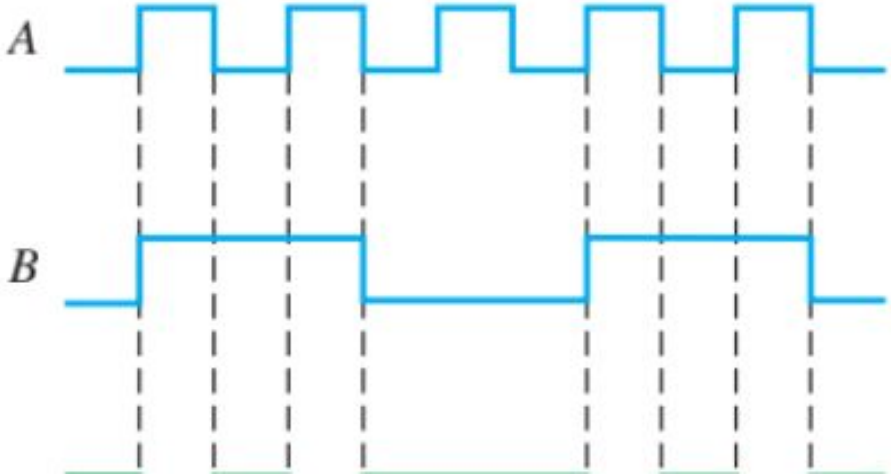
TABLE 3–7

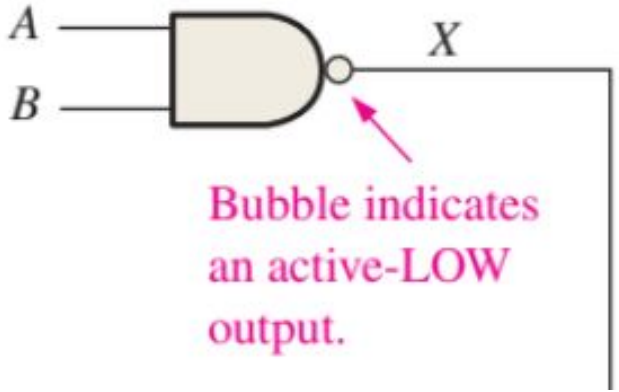
Truth table for a 2-input NAND gate.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	1
1	0	1
1	1	0

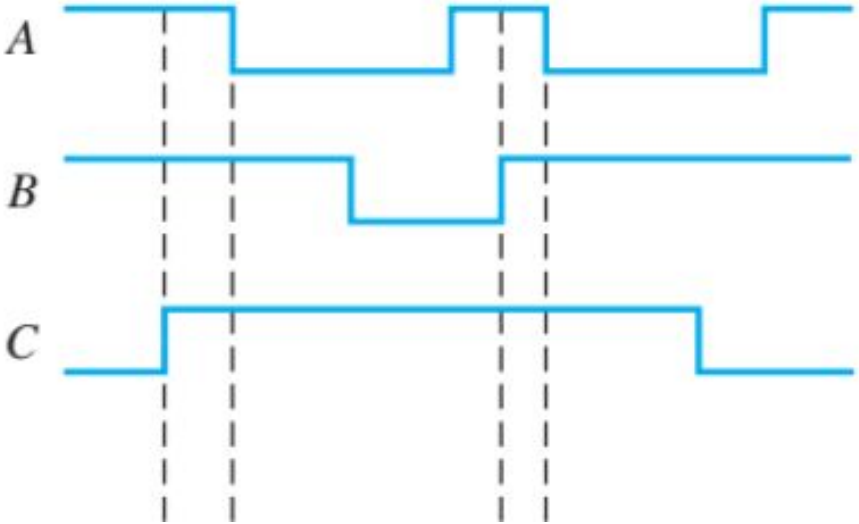


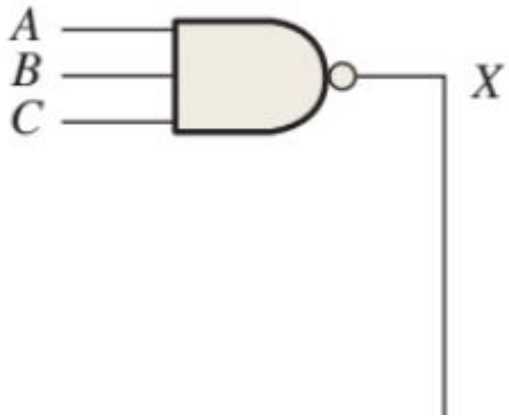
NAND Gate Timing Diagram



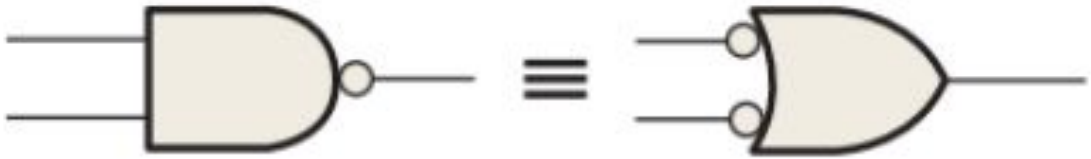


NAND Gate Timing Diagram



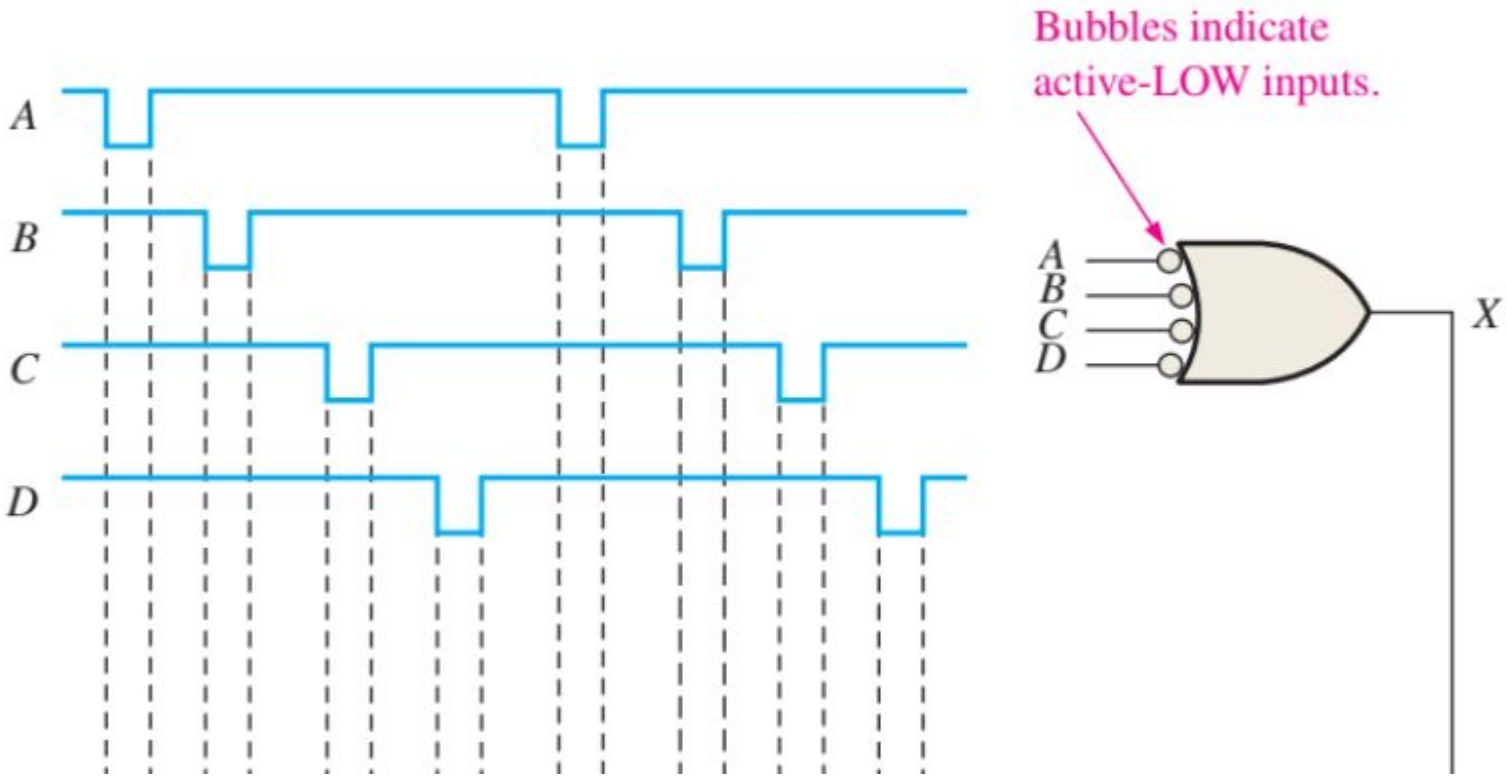


NAND Gate



NAND ≡ Negative-OR

NAND Gate



NAND Gate

$$X = \overline{AB}$$

TABLE 3–8

A	B	$\overline{AB} = X$
0	0	$\overline{0 \cdot 0} = \overline{0} = 1$
0	1	$\overline{0 \cdot 1} = \overline{0} = 1$
1	0	$\overline{1 \cdot 0} = \overline{0} = 1$
1	1	$\overline{1 \cdot 1} = \overline{1} = 0$

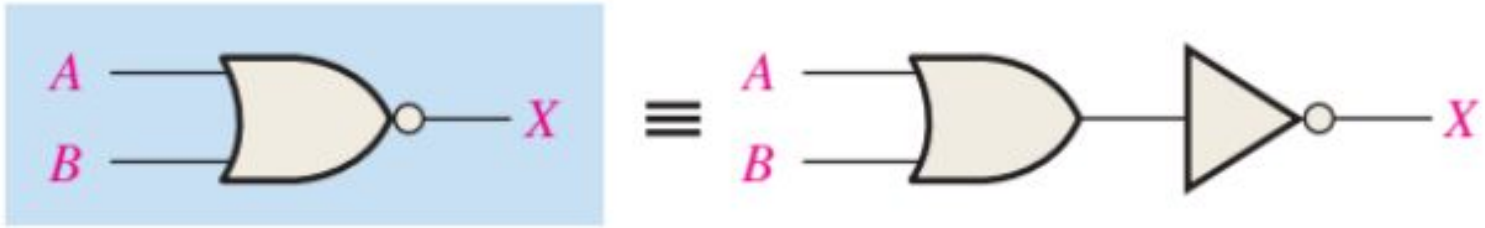
NOR Gate

NOR = Not OR

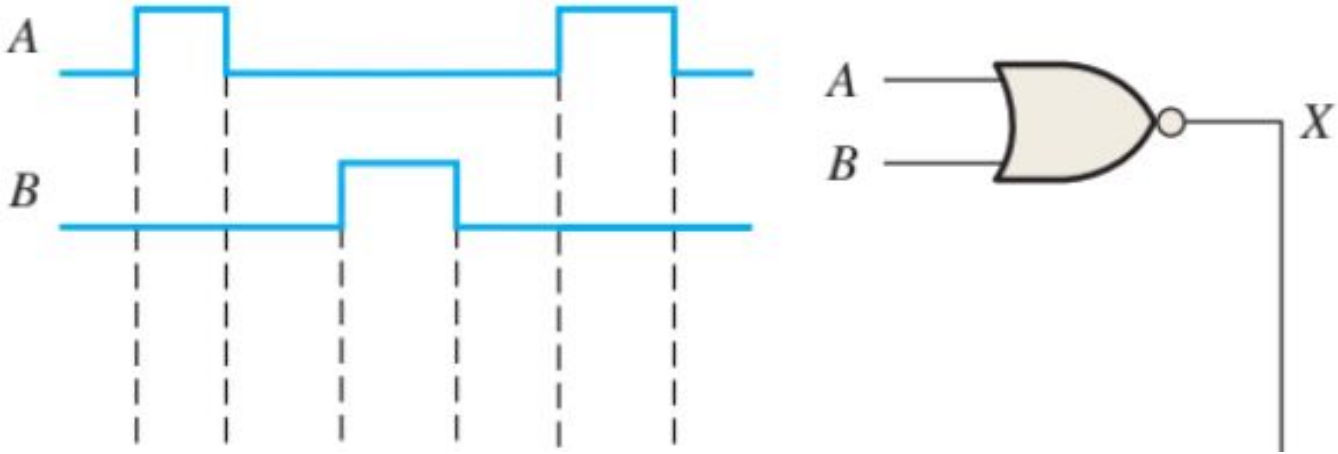
TABLE 3–9

Truth table for a 2-input NOR gate.

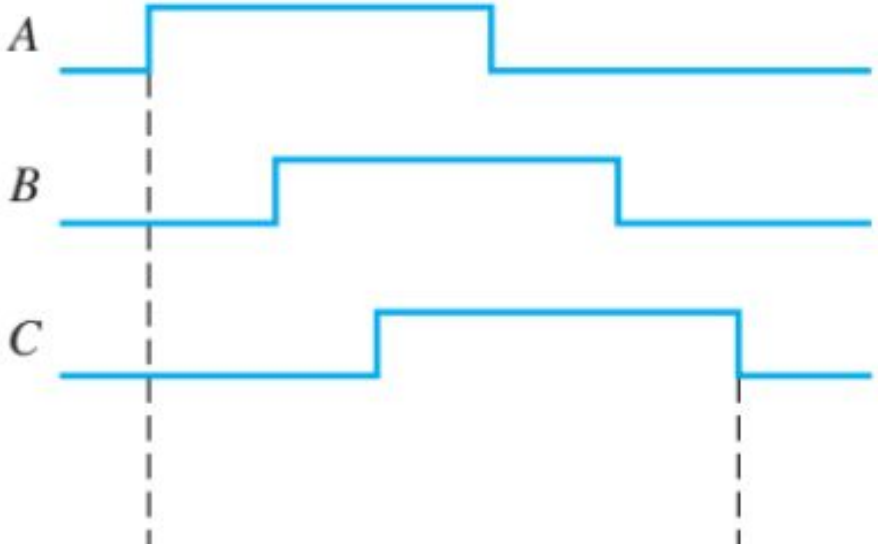
Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	0

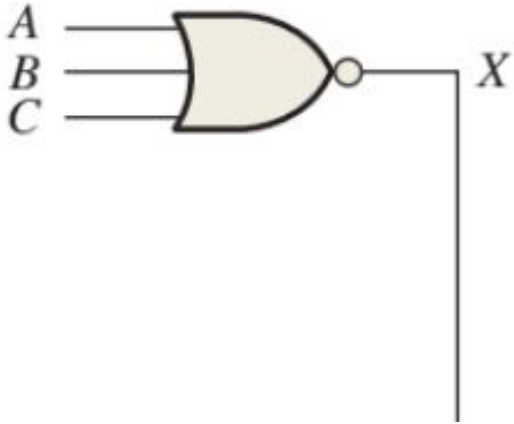


NOR Gate Timing Diagram

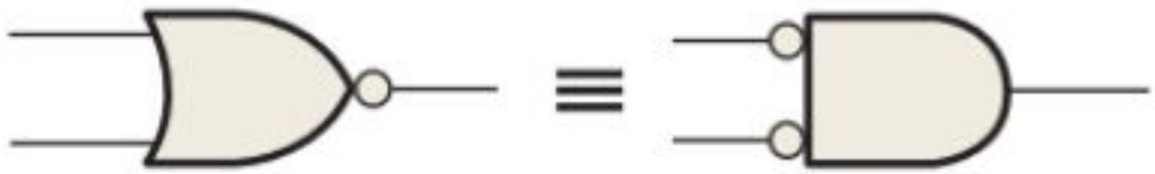


NOR Gate Timing Diagram



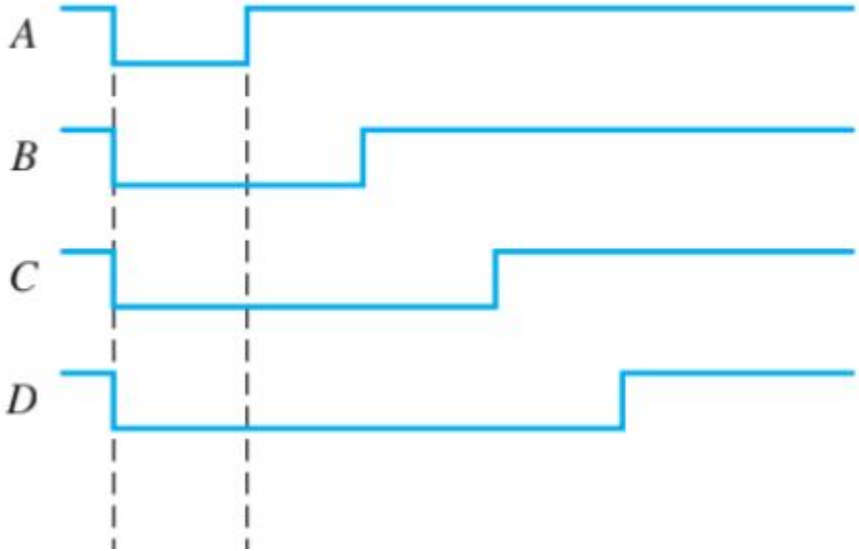


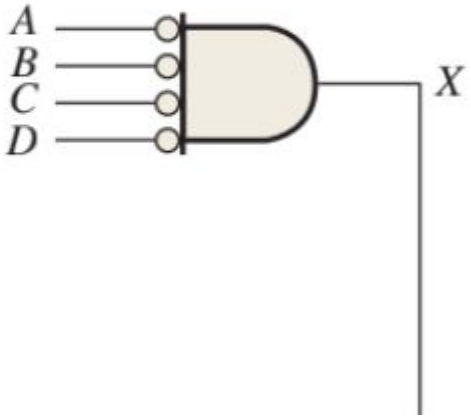
NOR Gate



NOR ≡ Negative-AND

NOR Gate Timing Diagram





NOR Gate

$$X = \overline{A + B}$$

TABLE 3–10

A	B	$\overline{A + B} = X$
0	0	$\overline{0 + 0} = \overline{0} = 1$
0	1	$\overline{0 + 1} = \overline{1} = 0$
1	0	$\overline{1 + 0} = \overline{1} = 0$
1	1	$\overline{1 + 1} = \overline{1} = 0$

Exclusive OR Gate

Exclusive or XOR Gate

Performs modulo-2 addition

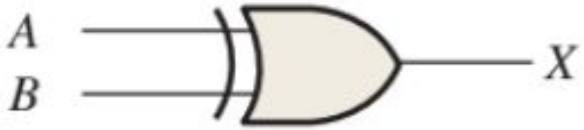
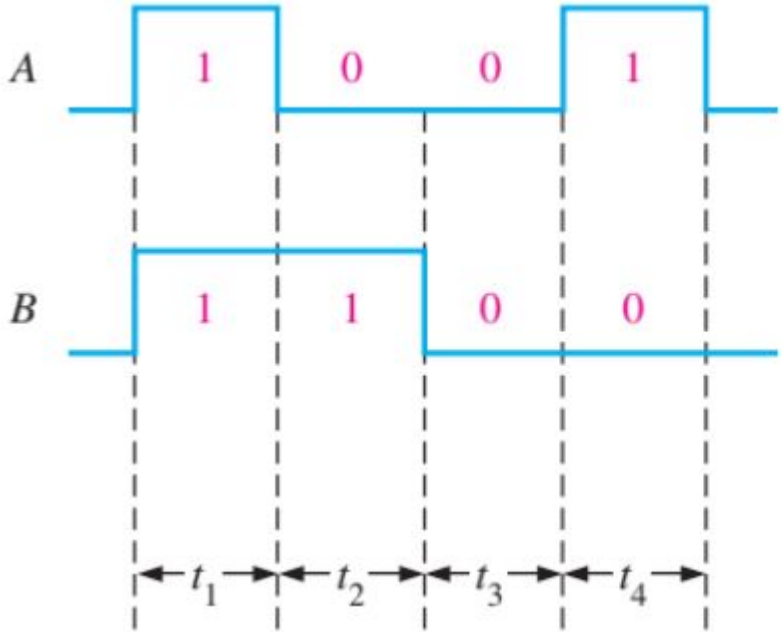


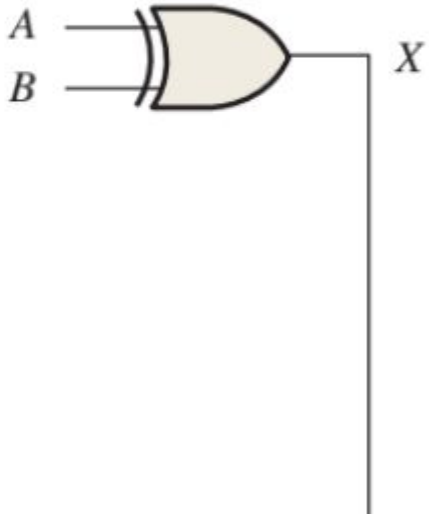
TABLE 3–11

Truth table for an exclusive-OR gate.

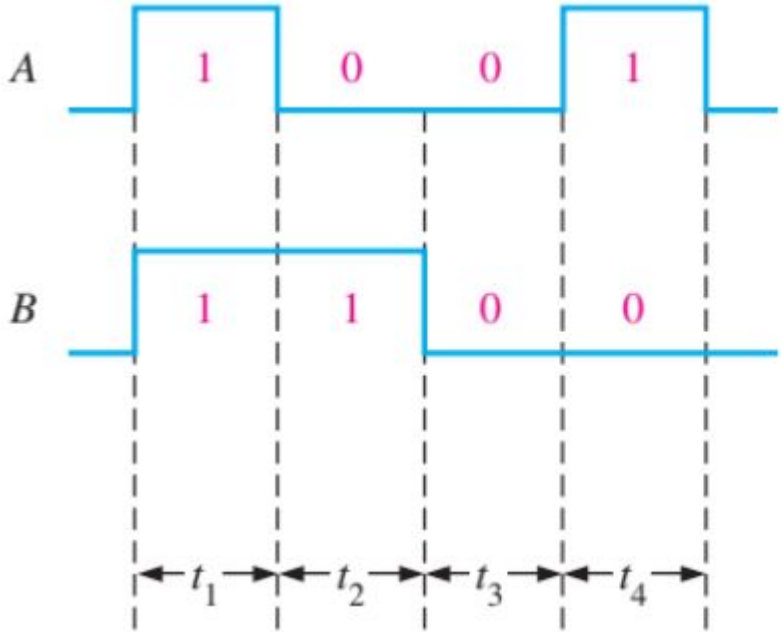
Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	0

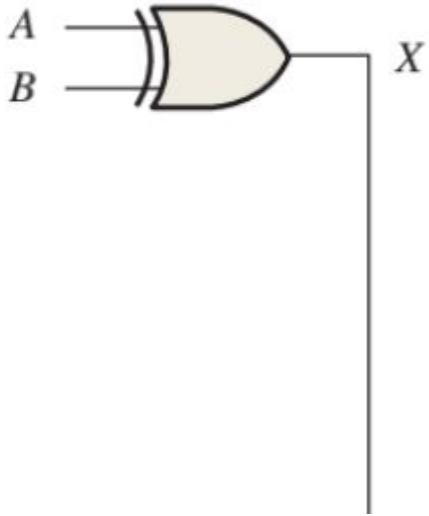
Exclusive OR Gate Timing Diagram





Exclusive OR Gate Timing Diagram



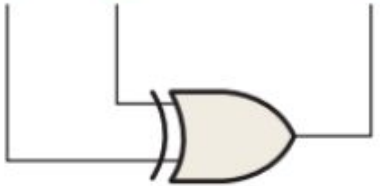


XOR Application

TABLE 3–13

An XOR gate used to add two bits.

Input Bits		Output (Sum)	
A	*B*	Σ	
0	0	0	
0	1	1	
1	0	1	
1	1	0	(without the 1 carry bit)



Exclusive NOR Gate

Exclusive NOT OR or XNOR Gate

Performs modulo-2 addition

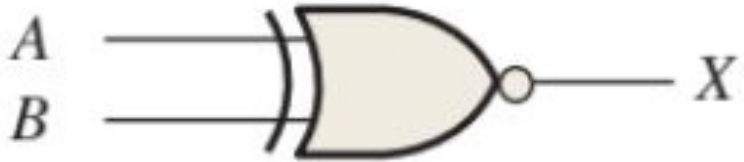
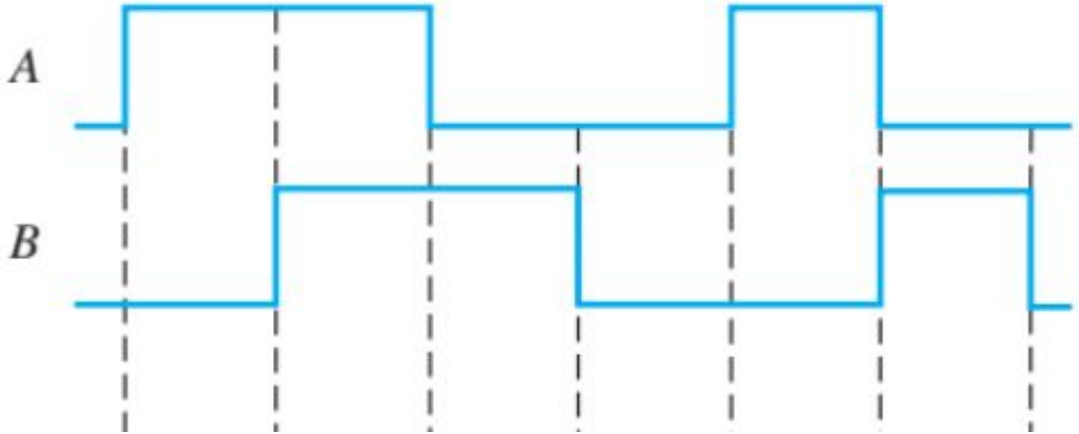


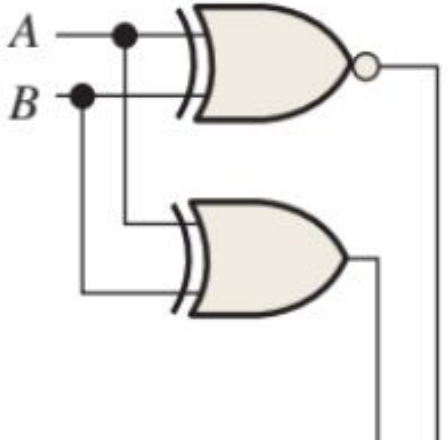
TABLE 3–12

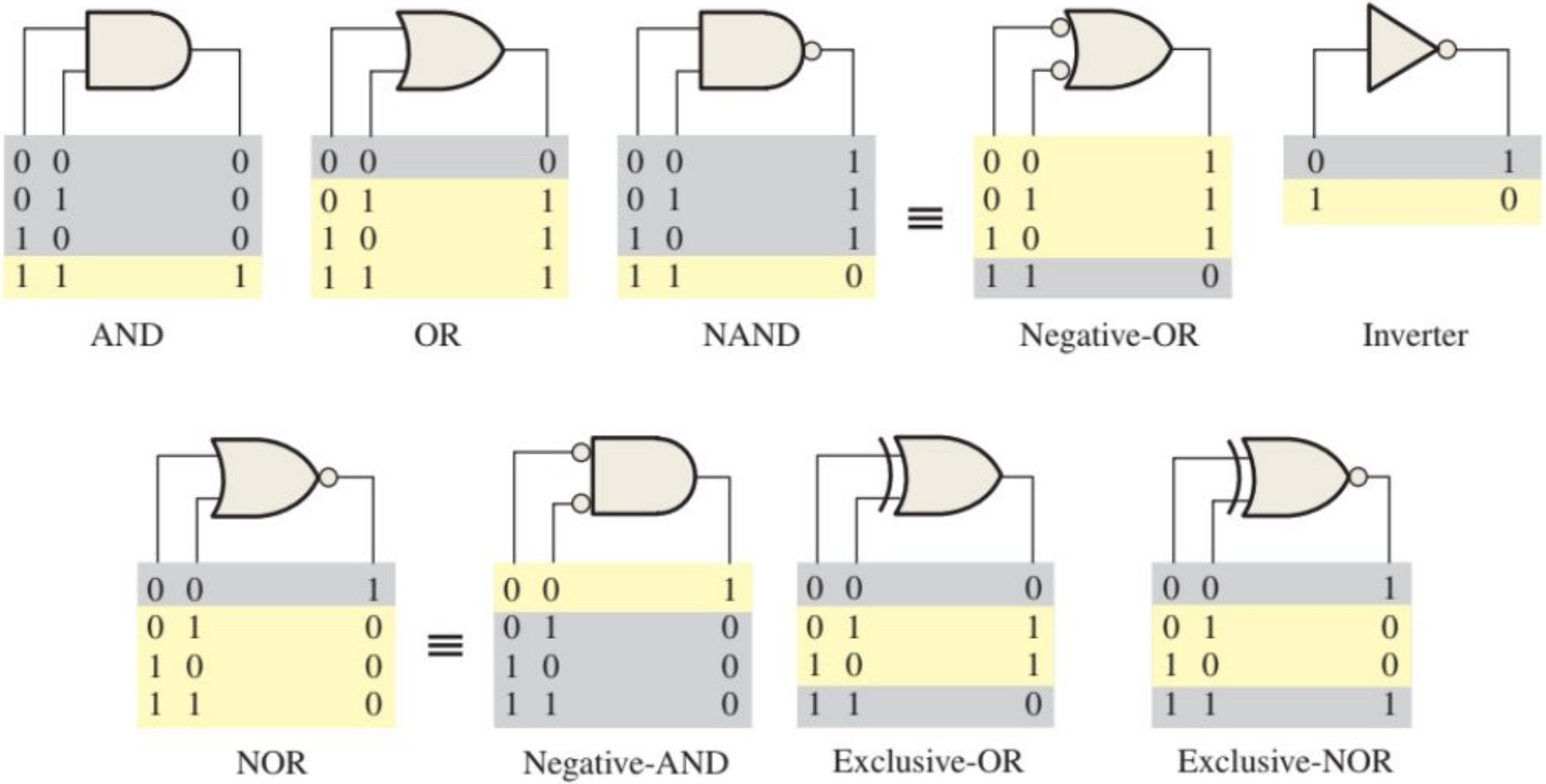
Truth table for an exclusive-NOR gate.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	0
1	0	0
1	1	1

XNOR Gate Timing Diagram







Note: Active states are shown in yellow.

FIGURE 3–75