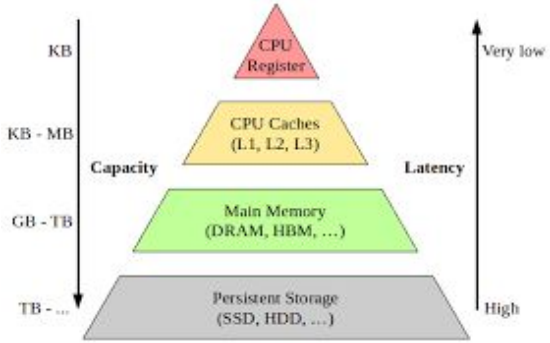


Shift Registers

Chapter 8

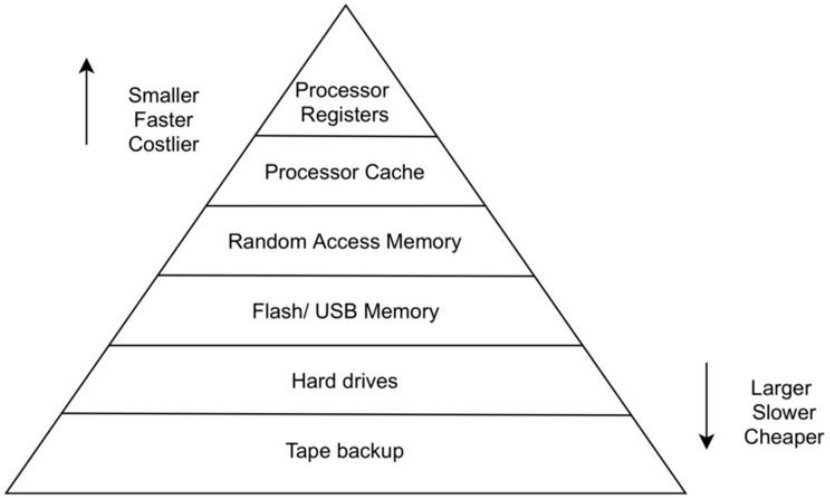
Sumaiyah Zahid

Registers

The smallest and fastest memory

It is used solely for storing and shifting data (1s and 0s)

A register can consist of one or more flip-flops used to store and shift data.



Registers

The storage capacity of a register is the total number of bits (1s and 0s) of digital data it can retain.

Each stage (flip-flop) in a shift register represents one bit of storage capacity; therefore, the number of stages in a register determines its storage capacity.

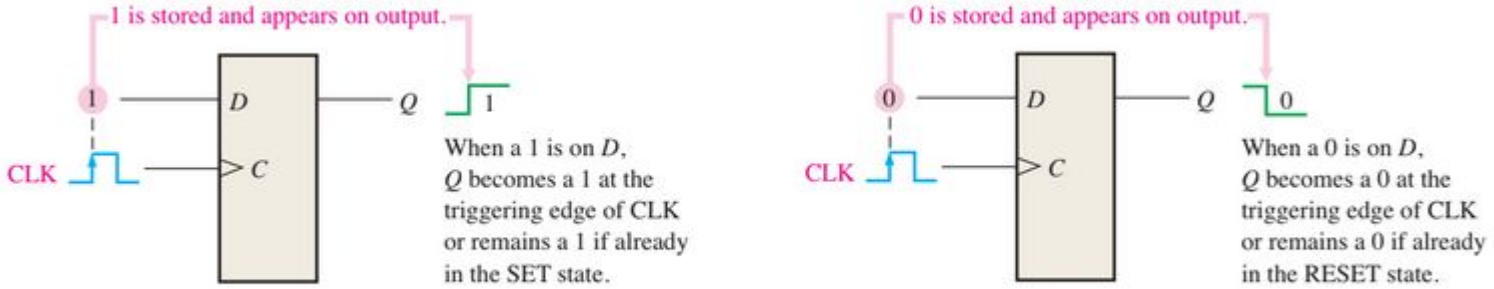


FIGURE 8–1 The flip-flop as a storage element.

Shift Registers

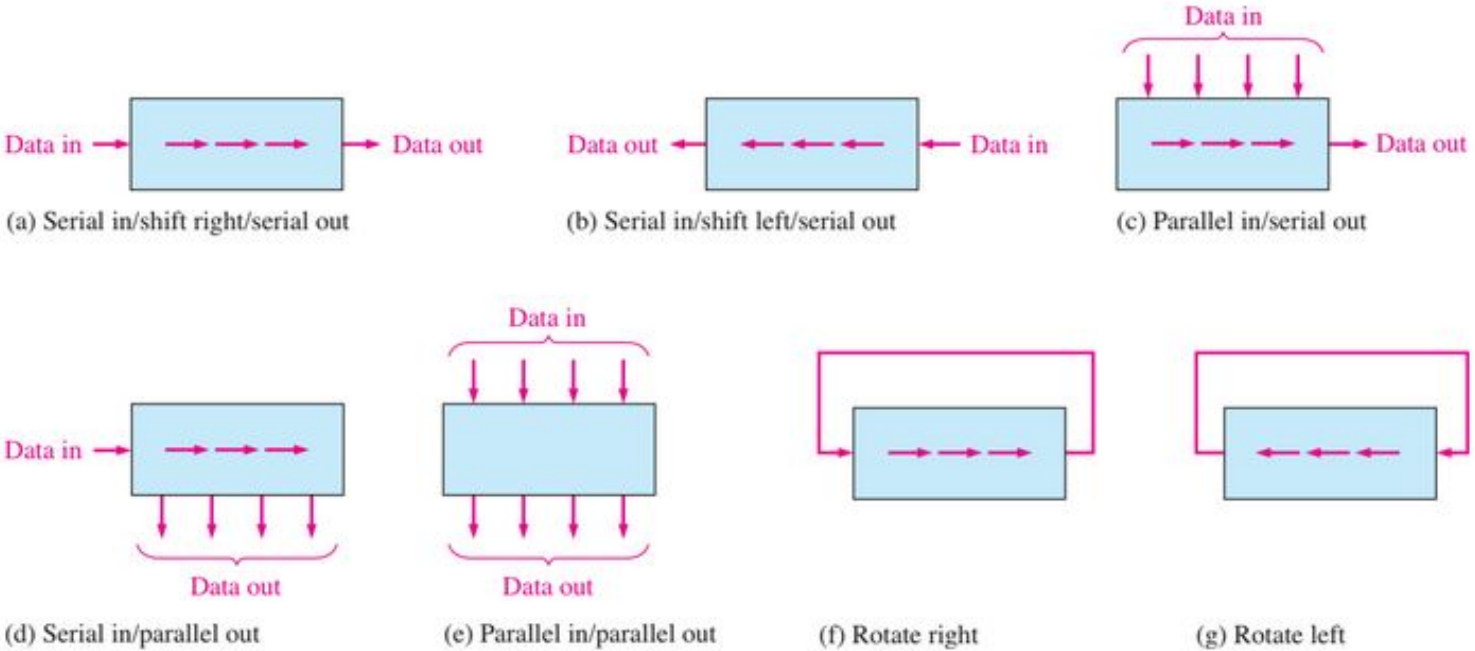


FIGURE 8–2 Basic data movement in shift registers. (Four bits are used for illustration. The bits move in the direction of the arrows.)

Serial In/Serial Out Shift Registers

FIGURE 8–5 Logic symbol for an 8-bit serial in/serial out shift register.

4-bit Register implemented with 4 D flip-flops.

With four stages, this register can store up to four bits of data.

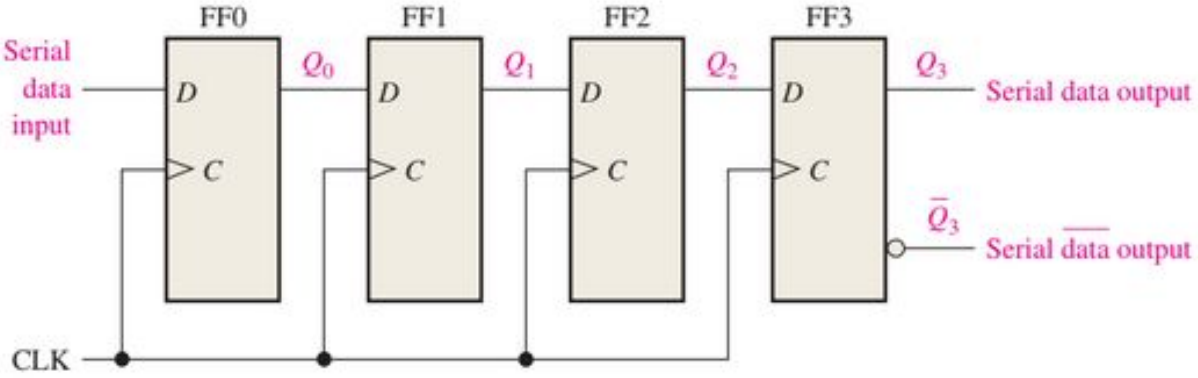


FIGURE 8–3 Serial in/serial out shift register.

Serial In/Serial Out Shift Registers

For serial data, one bit at a time is transferred.

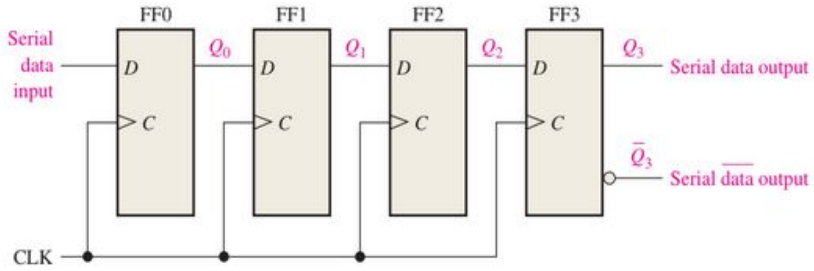


FIGURE 8–3 Serial in/serial out shift register.

TABLE 8–1

Shifting a 4-bit code into the shift register in Figure 8–3. Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	0	0	0	0
1	**0**	0	0	0
2	**1**	**0**	0	0
3	**0**	**1**	**0**	0
4	**1**	**0**	**1**	**0**

Serial In/Serial Out Shift Registers

For serial data, one bit at a time is transferred.

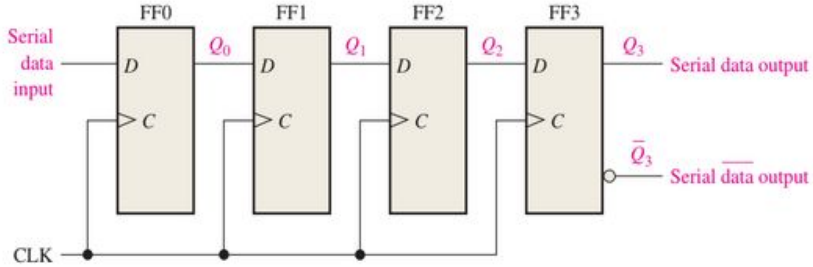


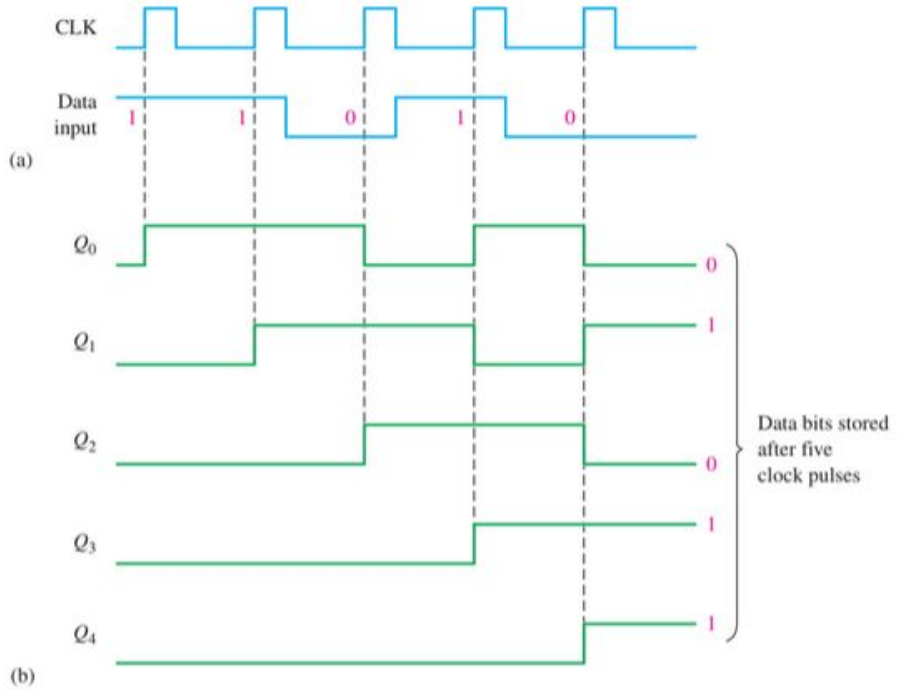
FIGURE 8–3 Serial in/serial out shift register.

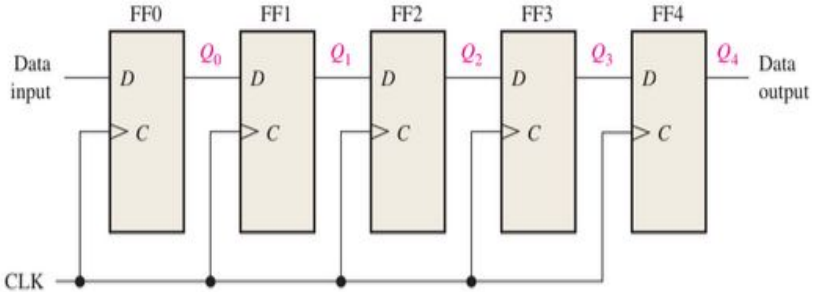
TABLE 8–2

Shifting a 4-bit code out of the shift register in Figure 8–3. Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	**1**	**0**	**1**	**0**
5	0	**1**	**0**	**1**
6	0	0	**1**	**0**
7	0	0	0	**1**
8	0	0	0	0

Serial In/Serial Out Shift Registers





Serial In/Parallel Out Shift Registers

Data bits are entered serially least-significant bit first

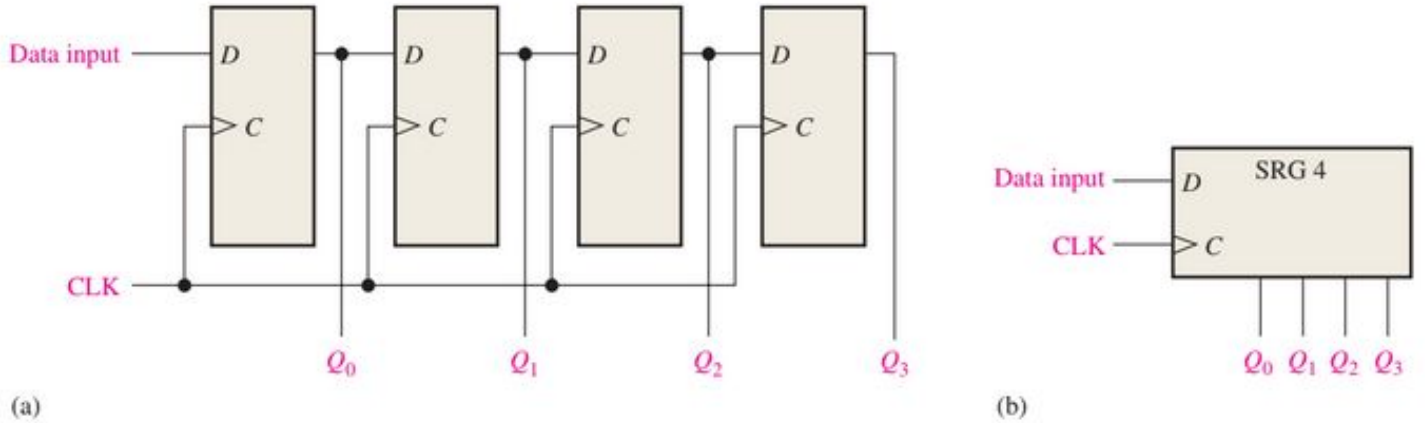
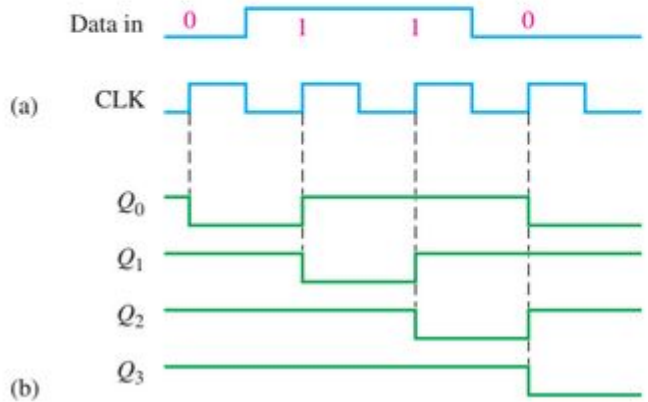


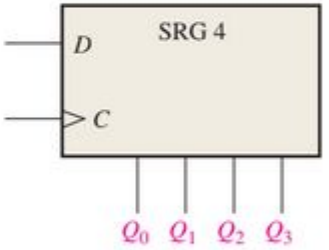
FIGURE 8–6 A serial in/parallel out shift register.

Serial In/Parallel Out Shift Registers

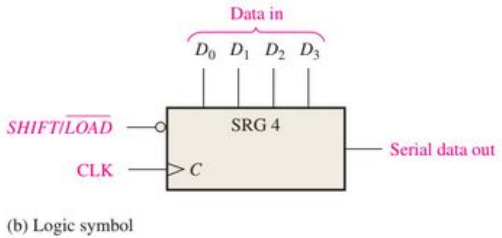
EXAMPLE 8–2

Show the states of the 4-bit register (SRG 4) for the data input and clock waveforms in Figure 8–7(a). The register initially contains all 1s.



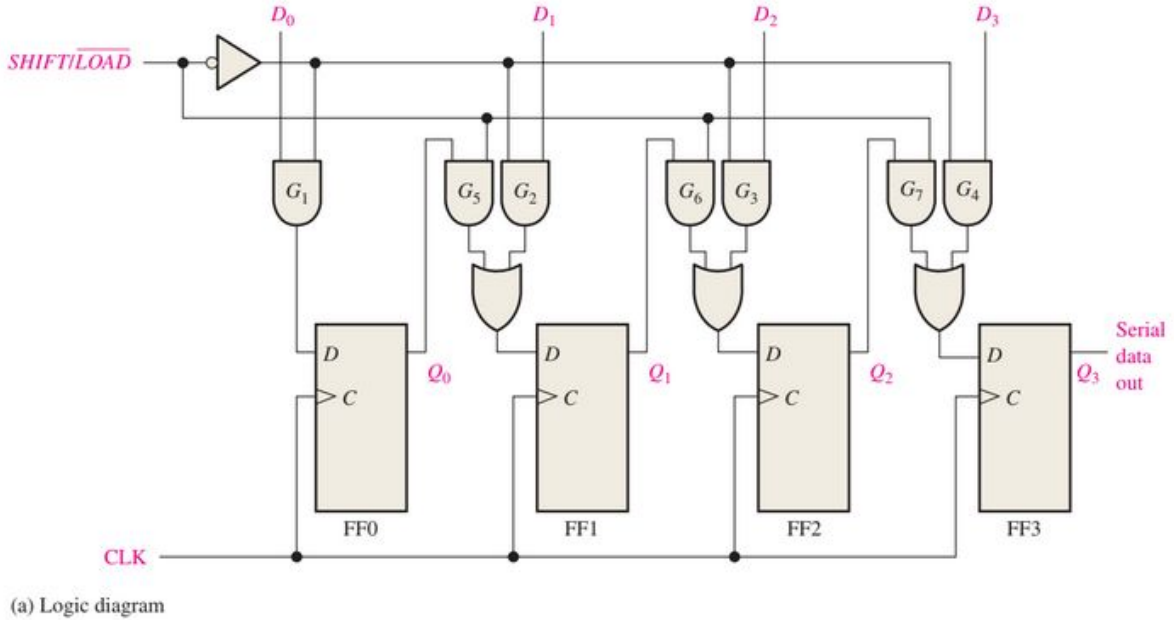


Parallel In/Serial Out Shift Registers



(b) Logic symbol

For parallel data, multiple bits are transfe
time



(a) Logic diagram

Parallel In/Serial Out Shift Registers

EXAMPLE 8–3

Show the data-output waveform for a 4-bit register with the parallel input data and the clock and *SHIFT*/$\overline{LOAD}$ waveforms given in Figure 8–11(a). Refer to Figure 8–10(a) for the logic diagram.

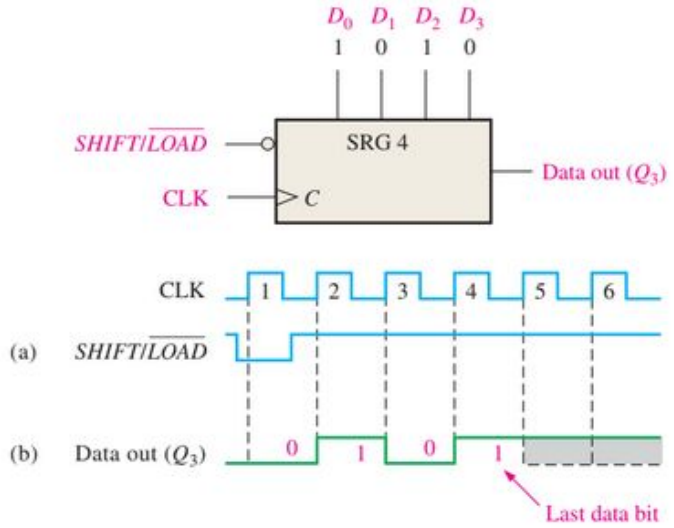


FIGURE 8–11

Parallel In/Parallel Out Shift Registers

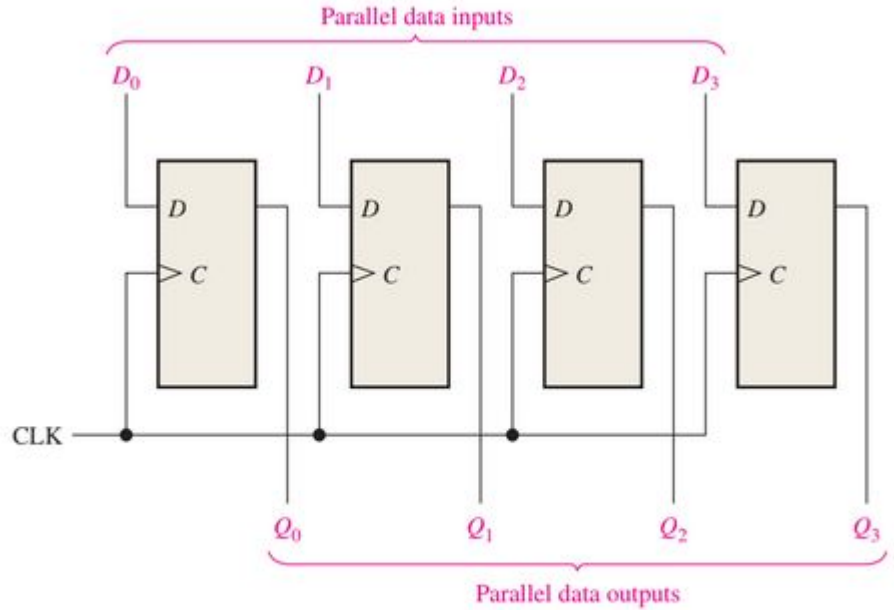


FIGURE 8–14 A parallel in/parallel out register.

Home Tasks

1. Develop the logic diagram for the shift registers using J-K flip-flops to replace the D flip-flops.

2. How many clock pulses are required to enter a byte of data serially into an 8-bit shift register?

3. The bit sequence 1101 is serially entered (least-significant bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?

4. How can a serial in/parallel out register be used as a serial in/serial out register?

5. Explain the function of the SHIFT/LOAD input.

6. Is the parallel load operation in Parallel in Serial Out shift register synchronous or asynchro

TBR

Bidirectional Shift Registers,

Shift Register Counters,

Shift Register Applications