

National University of Computer & Emerging Sciences, Kurachi



Spring-2017 CS-Department MidTerm ?

	30° March 2017, 1:00 am - 2:00am
Course Conse (8 20)	
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instructions.

Read each question completely before answering it. There are 2 questions and 2 pages.

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In case of any ambiguity, you may make assumption. But your assumption should not contradict any statement in the question paper.

Section No:

All the answers must be solved according to the sequence given in the question paper.

Time: 60 minutes.

Max Marks: 60 points

Ougstion 1:015 Marks)

1. What is the purpose of inverted page table? What are its advantages over page table? (3 Marks)

(2 Marks)

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2. Give an example where multilevel queues for scheduling of processes are beneficial. 3. How many memory accesses are required to access a data if 3-level paging scheme is used, assuming TLB miss? (3 Marks)

4. How is internal fragmentation affected by having large fixed partitions? (3 Marks)

3. What is meant by external fragmentation of memory? Give a possible solution for it. Which type of fragmentation occurs in paging and in segmentation? (4Marks)

Question 2:(45 Marks)

1. Processes p1 and p2 are swapped out at time instance 3 and swapped in at time instance 6. Process p1 has compile time binding and process p2 has execution time binding. Will the processes p1 and p2 be located t the same location or they may be located at different locations when they will be swapped back into main nemory. (4 Marks)

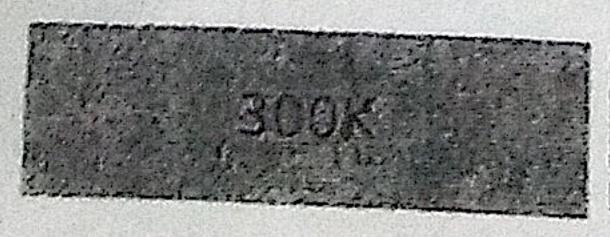
Calculate the effective memory access time for a TLB hit ratio of 95%, if 20nanoseconds are required to arch the TLB and the memory access time is 150nanoseconds. (2 Marks)

You are given the available memory holes 50K, 200K, 300K, and 10K. Processes P1, P2, P3 and P4 with naround time 3, 4, 2 and 5 respectively arrive in first come first serve order demand storage of 100k, ok, 95k and 270k respectively. At what time instant request of all jobs will be satisfied using best fit degy? (6 Marks)

w your working and draw allocated Memory blocks after completion of each process till request of all esses will be satisfied)









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4. For the given processes with the respective arrival and CPU barst time, give the Guard shart and calculates the furnaround time and the respective arrival and CPU barst time, give the Guard shart and calculates the turnaround time and the average waiting time for each of the following CVU scheduling policies 1709 MARRIAN

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1. Round-Robin(RR) with time quant

Processes	CPU Burst	CPU Bures		
p0	Durst	Arrival time	Printing Gran Only for property subscholing, etc.	
p1	10			
p2	9	0		
	7	2	0	
p3	8	4	4	
		6	2	

5. For the following segment table, find the physical addresses corresponding to the given logical addresses given as segment a contemporary of the contemporary of th given as segment, offset pairs:

1. 2.200

2.3,150

3. 0,520

Segment No.	Base address	Length(Bytes)
0	300	500
	1000	200
	1400	300
	2000	250

6. Consider a simple paging scheme with the following parameters: 2/32 total number of pages; page size -2^12 Bytes; 2^20 total number of frames. (16 Marks)

- 1. Calculate size of virtual address space and physical address space in bytes.
- 2. How many bits are there in a logical address?
- 3. How many bits are there in a physical address?
- 4. How many entries are there in the page table?
- 5. What will be the total page table size if each entry takes 4bytes?
- 6. What percentage of process P1 address space is covered by TLB(32 entries), if process P1 will fix in 500 pages?