CPE 110408423
VLSI Design
Chapter 0: Fundamentals of VLSI Design

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Course Administration

- Instructor: Bassam Jamil
- Instructor's e-mail: bassam@hu.edu.jo
- Office Hours: Posted on my office door

- Textbook:

Required: *CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition, Neil H. E. Weste, and David Money Harris, Pearson Publication, Inc., 2011.*

Optional:Digital Integrated Circuits: A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Prentice-Hall Publication, Inc., 2002.

Sedra & Smith, Microelectronic Circuits Oxford University Press, 5th Edition.

Slides : pdf on the course web page (Moodle System)

Course Content

- Course goals
  - The ability to analyze and design of digital integrated circuits families.
  - The ability to model datapath subsystems.
  - Acquire a basic knowledge to analyze design and circuit optimization of digital building blocks with respect to different quality metrics: cost, speed, power dissipation, and reliability.
  - The ability to learn fabrication and layout process, invertors design, clocks and power distribution and memory design.
  - The ability to work in groups to do design problems in the assignments and the projects.

- Course prerequisites

  Digital Integrated Circuits (0408422) Digital Electronics and Integrated Circuits (110408327).

Course Structure

- Design focused class:
  - Various homework assignments throughout the semester
- Lectures:

Ch0. Introduction

Ch11. Datapath Subsystems

Ch12. Array Subsystems

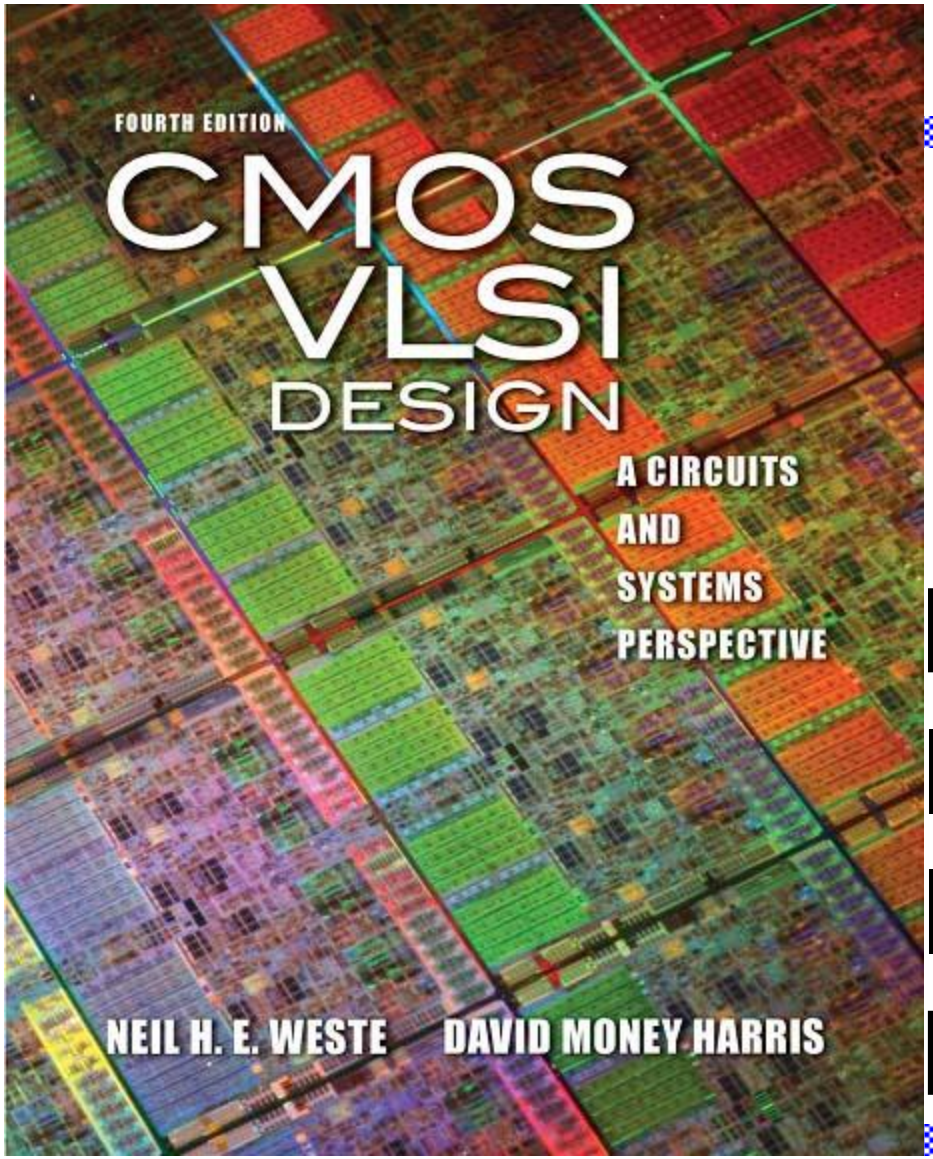
Ch13. Special-Purpose Subsystems **(optional)**

Ch14. Design Methodology Tools

Ch15. Testing, Debugging, and Verification

Grading Information

- Grade determinates
  - Midterm Exam ~30
  - Project ~20%
  - Final Exam ~50%
- Let me know about any exam conflicts ASAP



Lecture 0: Introduction: Intel Processors

Introduction

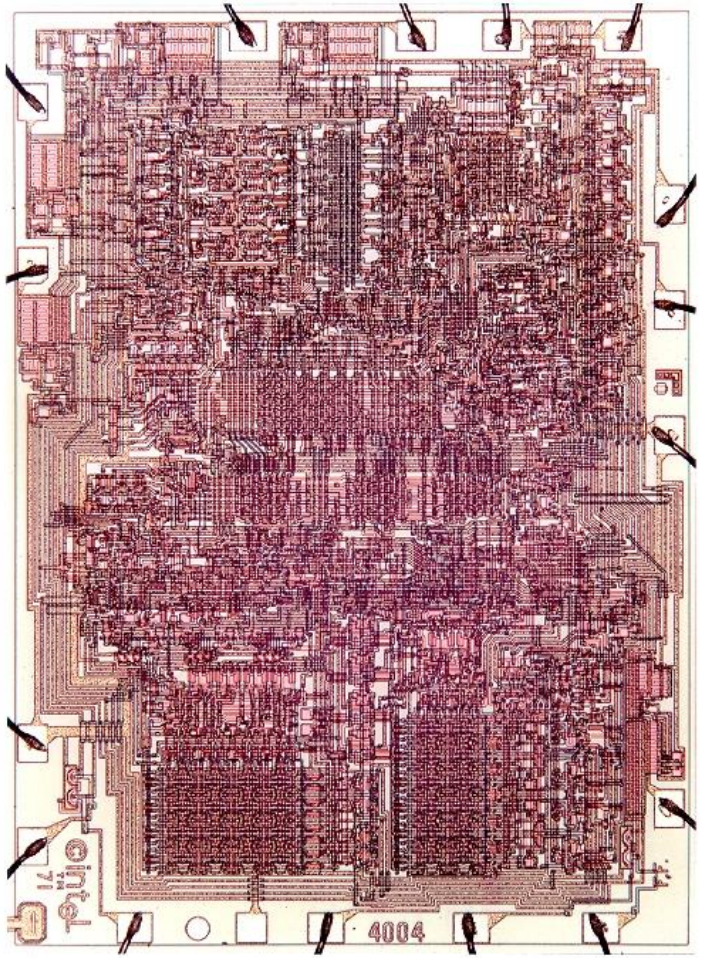
- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI): bucketloads!
- *Complementary Metal Oxide Semiconductor*
  - Fast, cheap, low power transistors
- Today: How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication
- Rest of the course: How to build a good CMOS chip

Outline

- Evolution of Intel Microprocessors
  - Scaling from 4004 to Core i7
  - Courtesy of Intel Museum

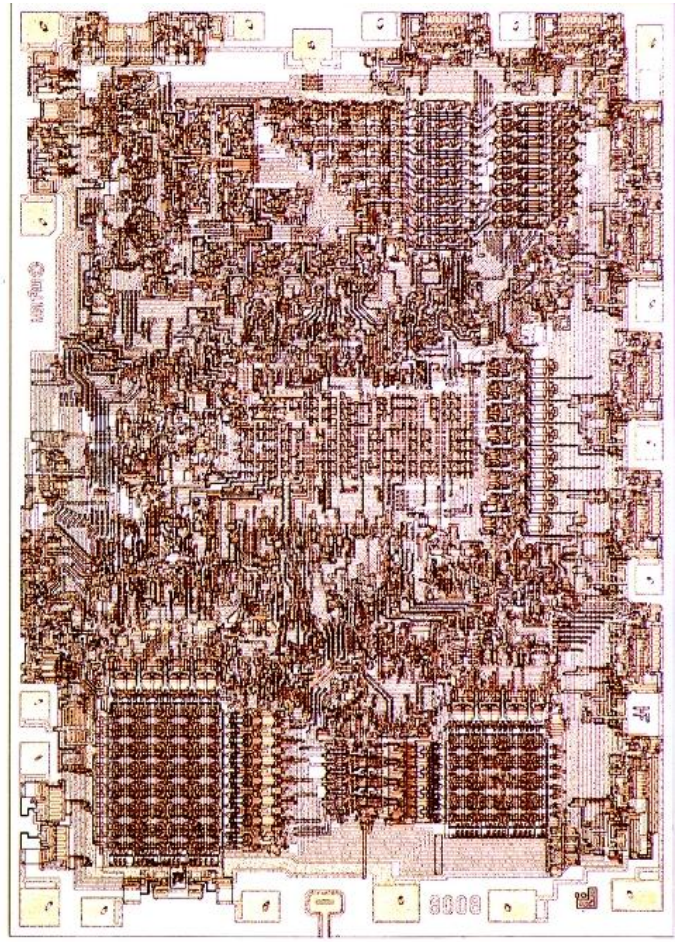
4004

- **First microprocessor** (1971)
  - For Busicom calculator
- Characteristics
  - 10 μm process
  - 2300 transistors
  - 400 – 800 kHz
  - 4-bit word size
  - 16-pin DIP package
- Masks hand cut from Rubylith
  - Drawn with color pencils
  - 1 metal, 1 poly (jumpers)
  - Diagonal lines (!)



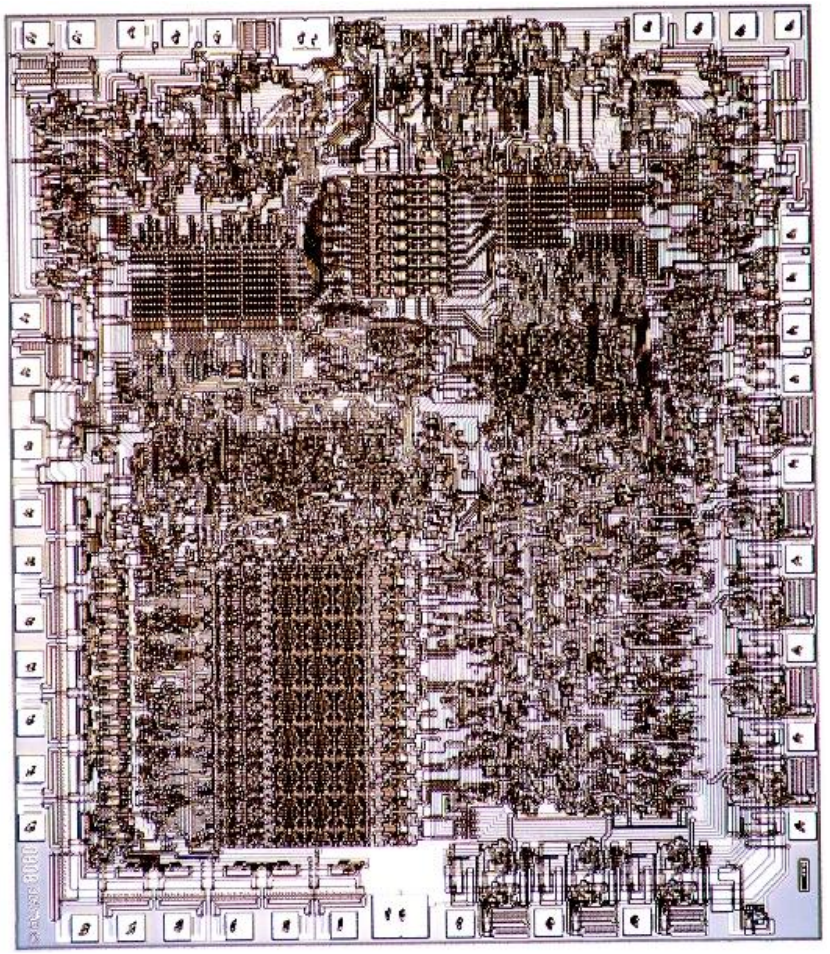
8008

- **8-bit follow-on** (1972)
  - Dumb terminals
- Characteristics
  - 10 μm process
  - 3500 transistors
  - 500 – 800 kHz
  - 8-bit word size
  - 18-pin DIP package
- Note 8-bit datapaths
  - Individual transistors visible



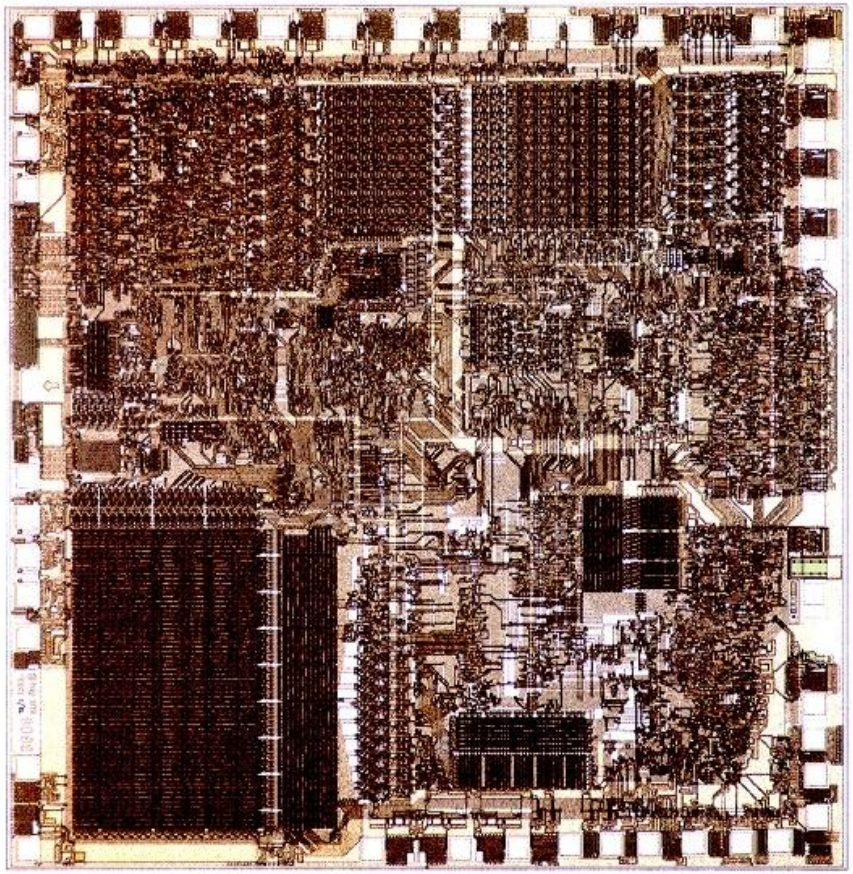
8080

- **16-bit address bus** (1974)
  - Used in Altair computer
    - (early hobbyist PC)
- Characteristics
  - 6 μm process
  - 4500 transistors
  - 2 MHz
  - 8-bit word size
  - 40-pin DIP package



8086 / 8088

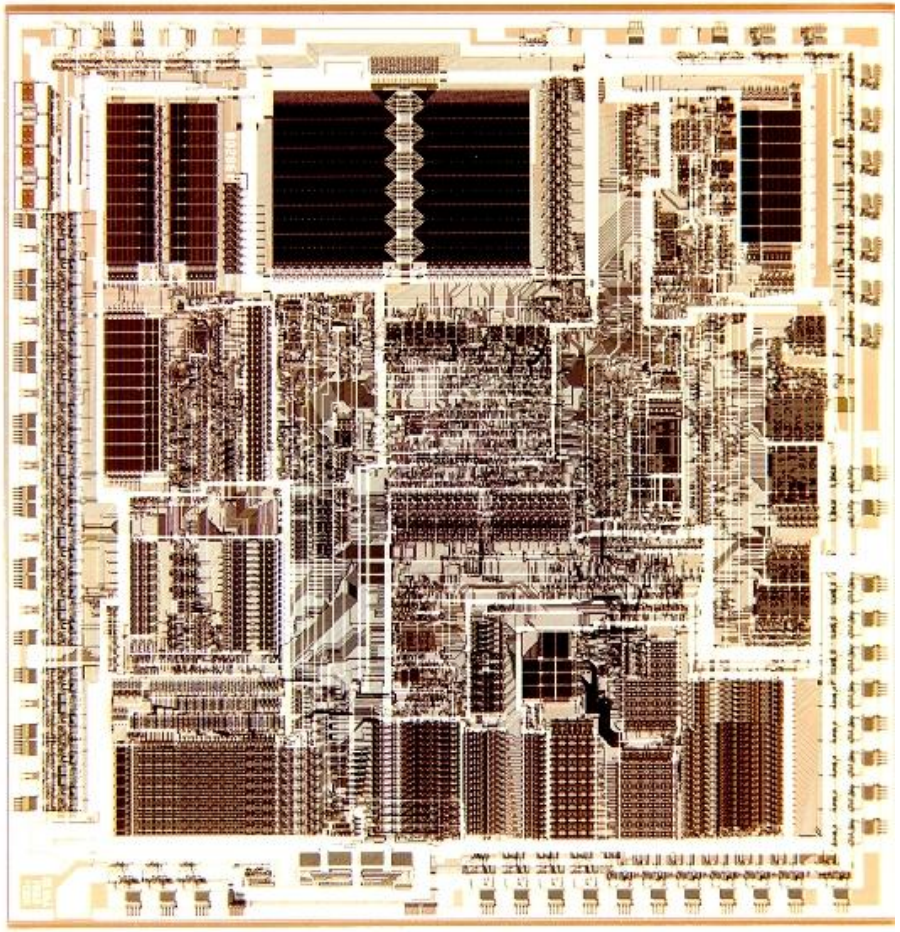
- **16-bit processor** (1978-9)
  - IBM PC and PC XT
  - Revolutionary products
  - Introduced x86 ISA
- Characteristics
  - 3 μm process
  - 29k transistors
  - 5-10 MHz
  - 16-bit word size
  - 40-pin DIP package
- Microcode ROM



80286

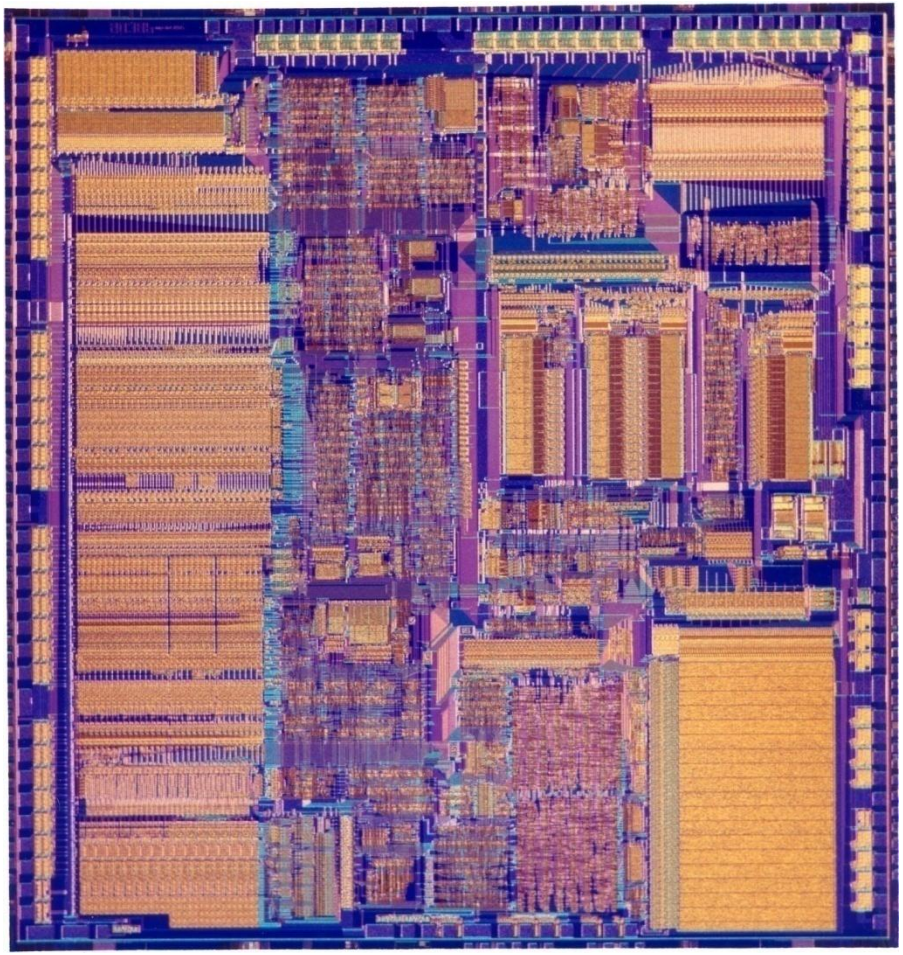
- **Virtual memory** (1982)
  - IBM PC AT
- Characteristics
  - 1.5 μm process
  - 134k transistors
  - 6-12 MHz
  - 16-bit word size
  - 68-pin PGA
- Regular datapaths and ROMs

  Bitslices clearly visible



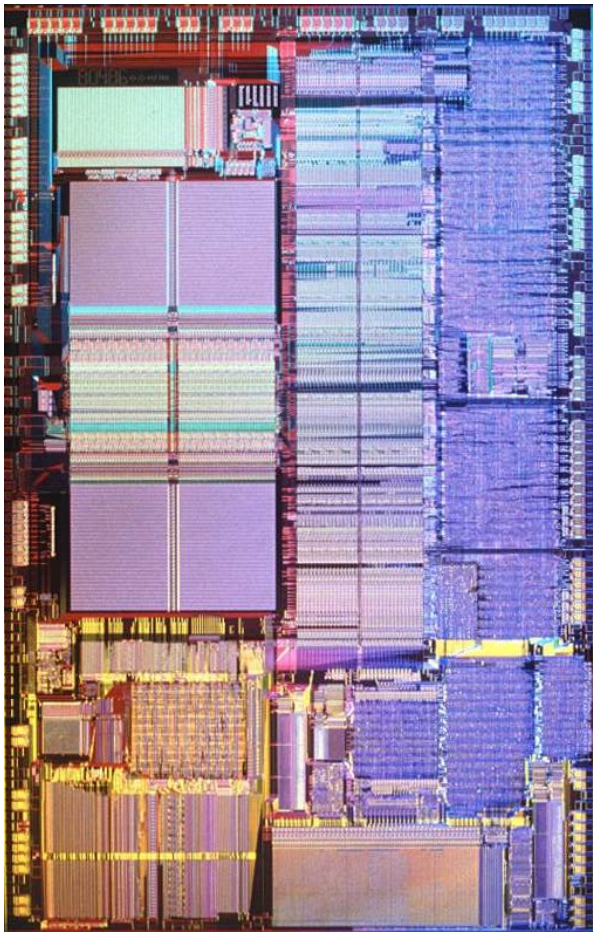
80386

- **32-bit processor (1985)**
  - **Modern x86 ISA**
- Characteristics
  - 1.5-1 μm process
  - 275k transistors
  - 16-33 MHz
  - 32-bit word size
  - 100-pin PGA
- 32-bit datapath, microcode ROM, synthesized control



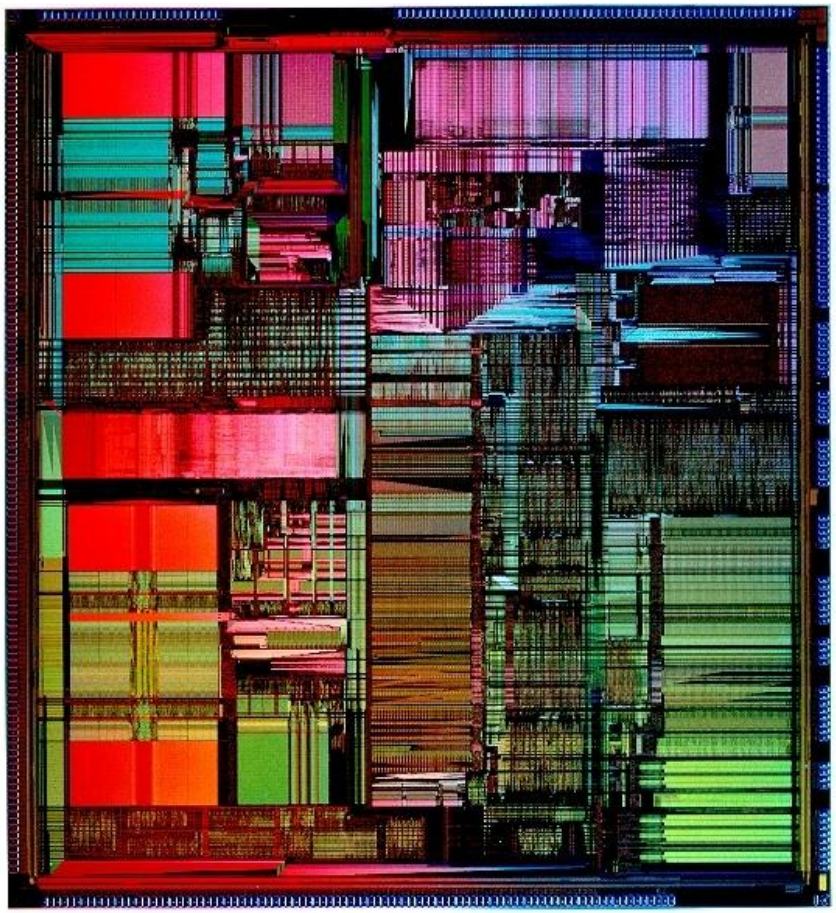
80486

- **Pipelining (1989)**
  - **Floating point unit**
  - 8 KB cache
- Characteristics
  - 1-0.6 μm process
  - 1.2M transistors
  - 25-100 MHz
  - 32-bit word size
  - 168-pin PGA
- Cache, Integer datapath, FPU, microcode, synthesized control



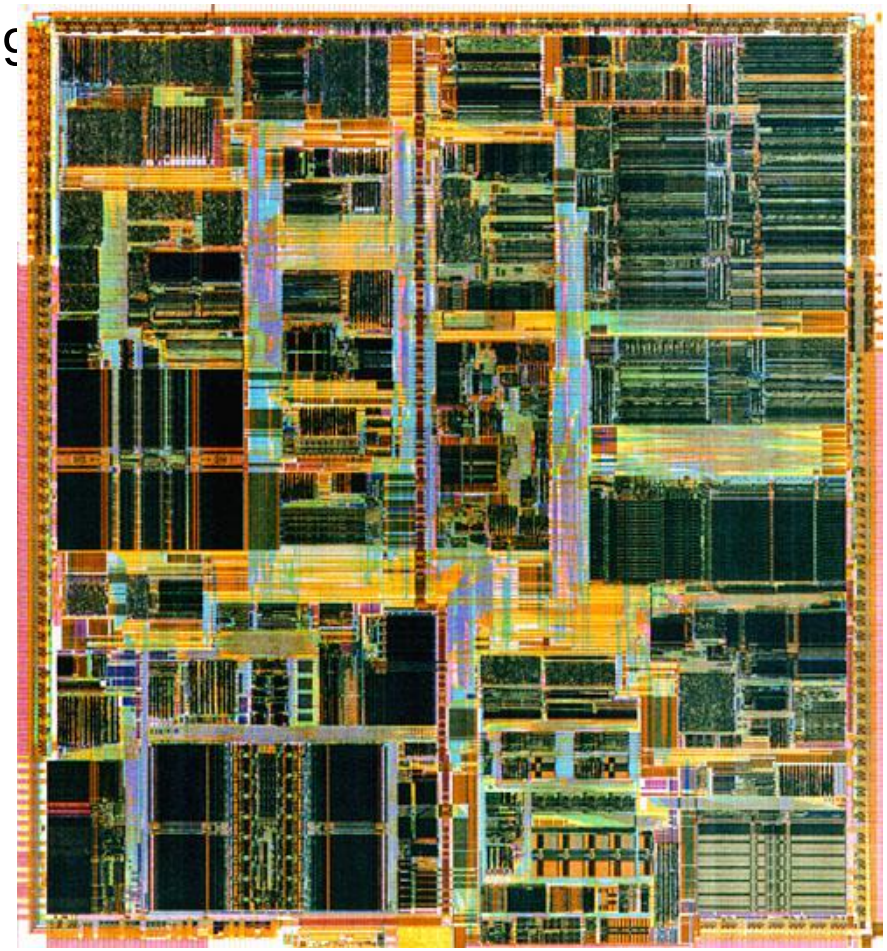
Pentium

- **Superscalar** (1993)
  - 2 instructions per cycle
  - Separate 8KB I$ & D$
- Characteristics
  - 0.8-0.35 μm process
  - 3.2M transistors
  - 60-300 MHz
  - 32-bit word size
  - 296-pin PGA
- Caches, datapath, FPU, control



Pentium Pro / II / III

- **Dynamic execution** (1995-9
  - 3 micro-ops / cycle
  - Out of order execution
  - 16-32 KB I$ & D$
  - Multimedia instructions
  - PIII adds 256+ KB L2$
- Characteristics
  - 0.6-0.18 μm process
  - 5.5M-28M transistors
  - 166-1000 MHz
  - 32-bit word size
  - MCM / SECC

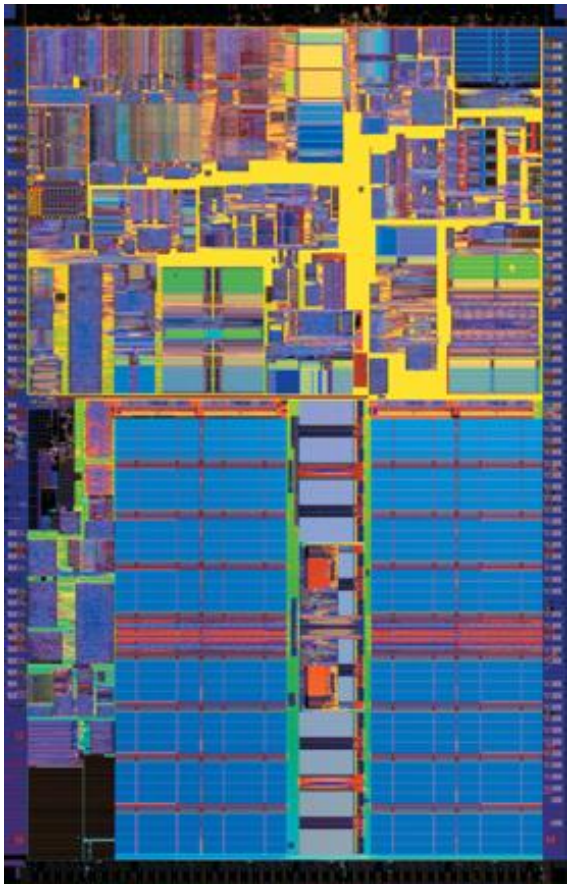


Pentium 4

- **Deep pipeline** (2001)
  - Very fast clock
  - 256-1024 KB L2$
- Characteristics
  - 180 – 65 nm process
  - 42-125M transistors
  - 1.4-3.4 GHz
  - Up to 160 W
  - 32/64-bit word size
  - 478-pin PGA
- Units start to become invisible on this scale

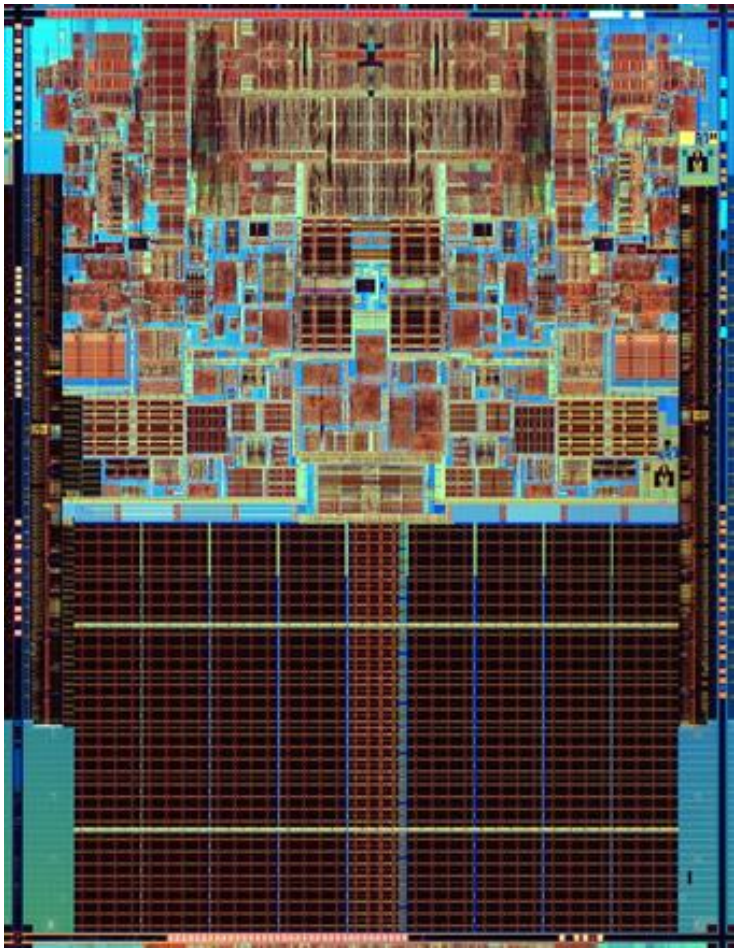
Pentium M

- Pentium III derivative
  - **Better power efficiency**
  - 1-2 MB L2$
- Characteristics
  - 130 – 90 nm process
  - 140M transistors
  - 0.9-2.3 GHz
  - 6-25 W
  - 32-bit word size
  - 478-pin PGA
- **Cache dominates chip area**



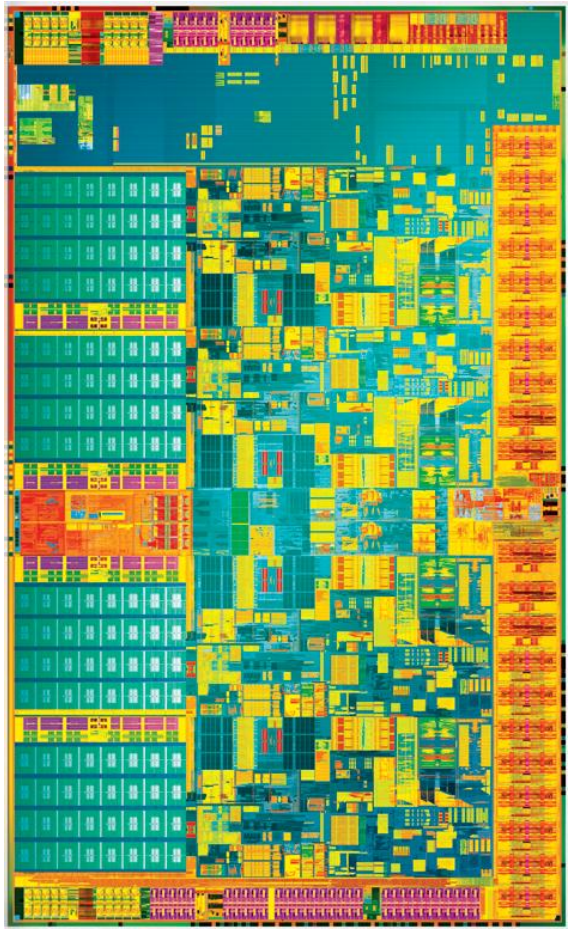
Core2 Duo

- **Dual core** (2006)
  - **1-2 MB L2$ / core**
- Characteristics
  - 65-45 nm process
  - 291M transistors
  - 1.6-3+ GHz
  - 65 W
  - 32/64 bit word size
  - 775 pin LGA
- Much better performance/power efficiency



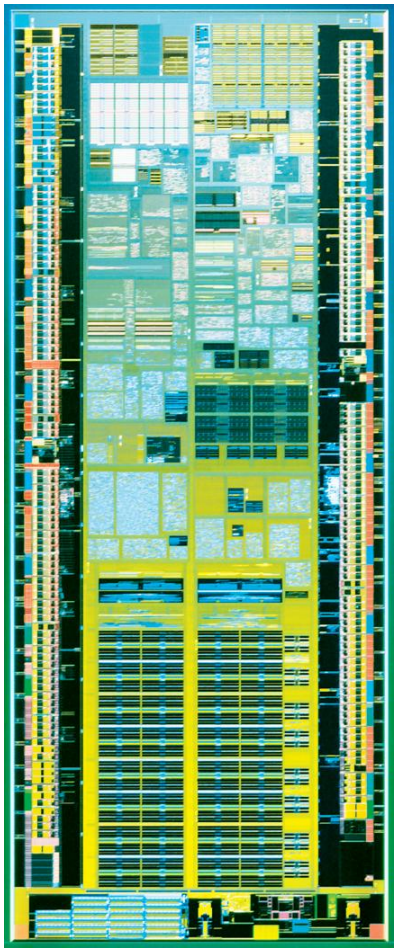
Core i7

- **Quad core (& more)**
  - Refinement of Core architecture
  - 2 MB L3$ / core
- Characteristics
  - 45-32 nm process
  - 731M transistors
  - 2.66-3.33+ GHz
  - Up to 130 W
  - 32/64 bit word size
  - 1366-pin LGA
  - Multithreading
- On-die memory controller



Atom

- **Low power CPU for netbooks**
  - Pentium-style architecture
  - 512KB+ L2$
- Characteristics
  - 45-32 nm process
  - 47M transistors
  - 0.8-1.8+ GHz
  - 1.4-13 W
  - 32/64-bit word size
  - 441-pin FCBGA
- Low voltage (0.7 – 1.1 V) operation
  - Excellent performance/power



Summary

- 10^4 increase in transistor count, clock frequency over 3 decades!

Processor	Year	Feature Size (μm)	Transistors	Frequency (MHz)	Word Size	Power (W)	Cache (L1 / L2 / L3)	Package
4004	1971	10	2.3k	0.75	4	0.5	none	16-pin DIP
8008	1972	10	3.5k	0.5–0.8	8	0.5	none	18-pin DIP
8080	1974	6	6k	2	8	0.5	none	40-pin DIP
8086	1978	3	29k	5–10	16	2	none	40-pin DIP
80286	1982	1.5	134k	6–12	16	3	none	68-pin PGA
Intel386	1985	1.5–1.0	275k	16–25	32	1–1.5	none	100-pin PGA
Intel486	1989	1–0.6	1.2M	25–100	32	0.3–2.5	8K	168-pin PGA
Pentium	1993	0.8–0.35	3.2–4.5M	60–300	32	8–17	16K	296-pin PGA
Pentium Pro	1995	0.6–0.35	5.5M	166–200	32	29–47	16K / 256K+	387-pin MCM PGA
Pentium II	1997	0.35–0.25	7.5M	233–450	32	17–43	32K / 256K+	242-pin SECC
Pentium III	1999	0.25–0.18	9.5–28M	450–1000	32	14–44	32K / 512K	330-pin SECC2
Pentium 4	2000	180–65 nm	42–178M	1400–3800	32/64	21–115	20K+ / 256K+	478-pin PGA
Pentium M	2003	130–90 nm	77–140M	1300–2130	32	5–27	64K / 1M	479-pin FCBGA
Core	2006	65 nm	152M	1000–1860	32	6–31	64K / 2M	479-pin FCBGA
Core 2 Duo	2006	65–45 nm	167–410M	1060–3160	32/64	10–65	64K / 4M+	775-pin LGA
Core i7	2008	45 nm	731M	2660–3330	32/64	45–130	64K / 256K / 8M	1366-pin LGA
Atom	2008	45 nm	47M	800–1860	32/64	1.4–13	56K / 512K+	441-pin FCBGA