CPE 110408423
VLSI Design
Chapter 13: Special-Purpose Subsystems

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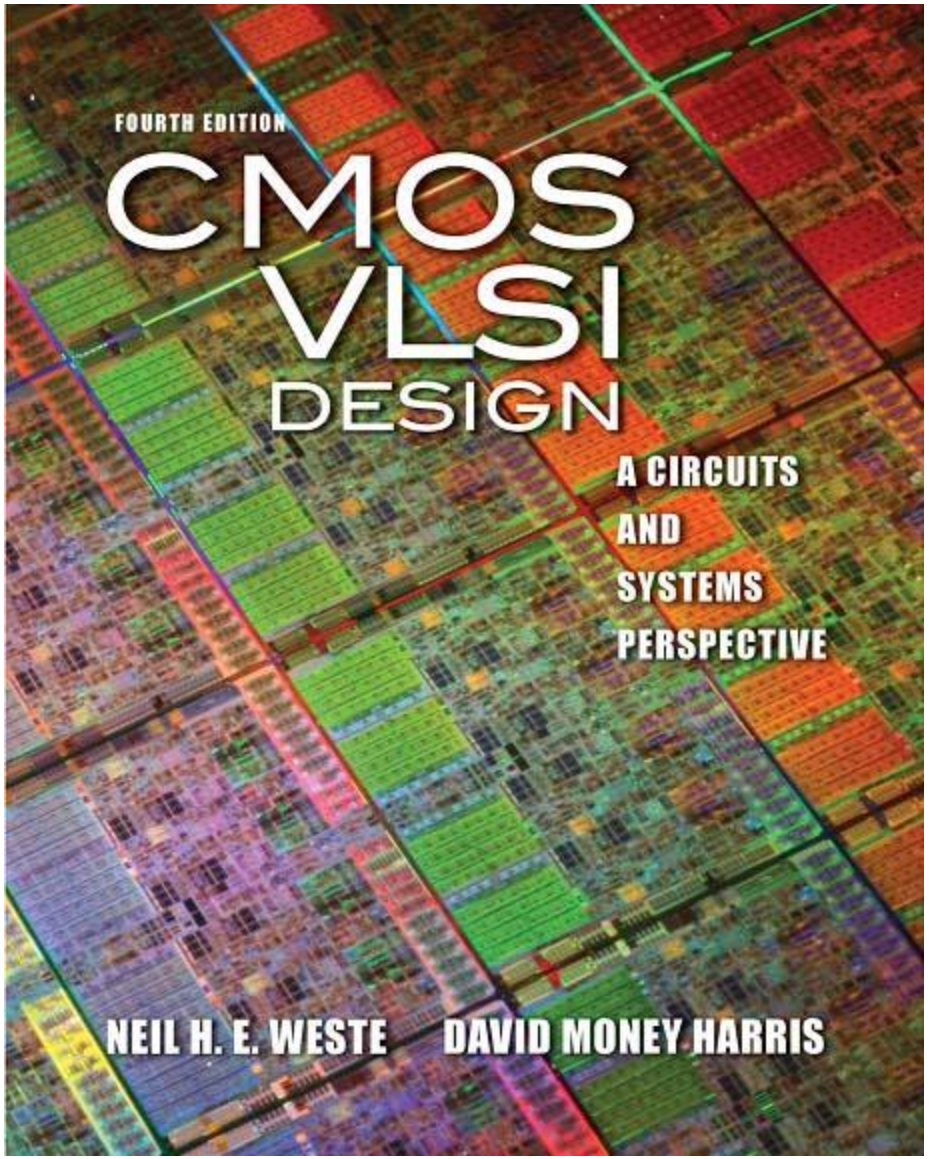


Lecture 5: Packaging, Power, & Clock

13.1 Outline

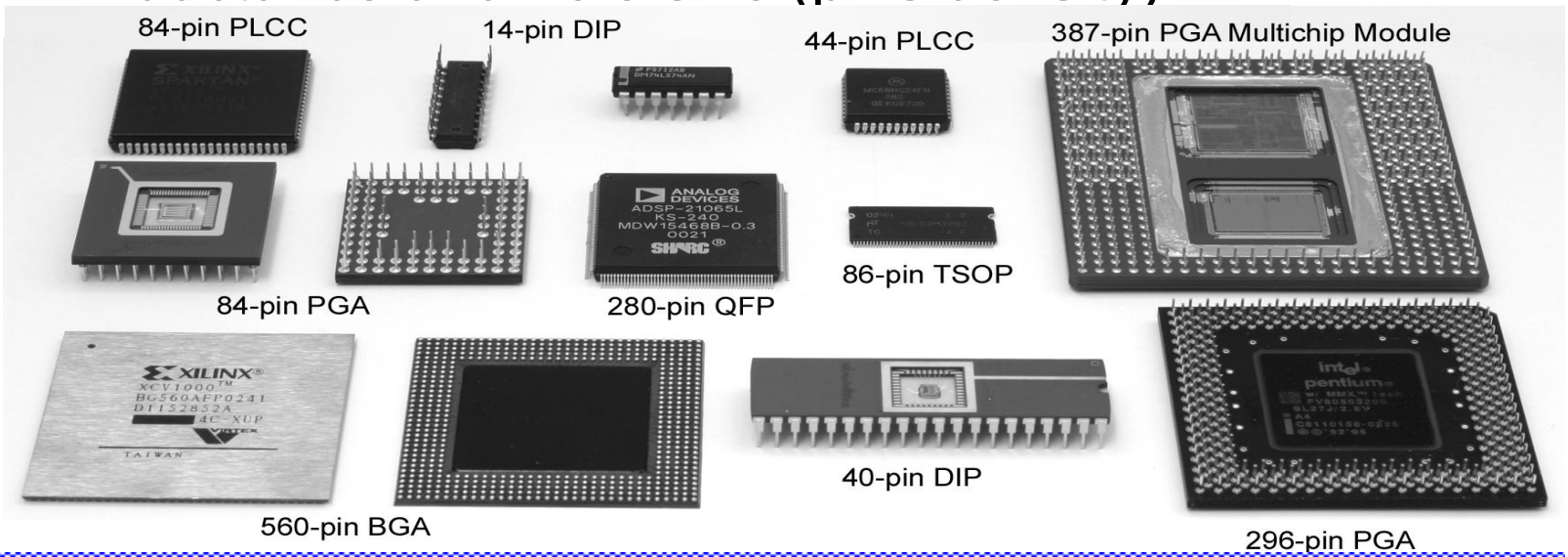
- Packaging and cooling
- Power Distribution
- Clock Distribution
- We will limit our discussion to:
  - Package types
  - Heat
  - Power Distribution:
  - 1. Power Supply drop:
    - IR drop
    - I di/dt
  - 2. Bypass capacitor
    - I = c dv/dt

13.2 Packaging and Cooling

- Package functions
  - Electrical connection of signals and power from chip to board
    - Little delay or distortion
  - Mechanical connection of chip to board
    - Removes heat produced on chip
    - Protects chip from mechanical damage
    - Compatible with thermal expansion
  - Inexpensive to manufacture and test

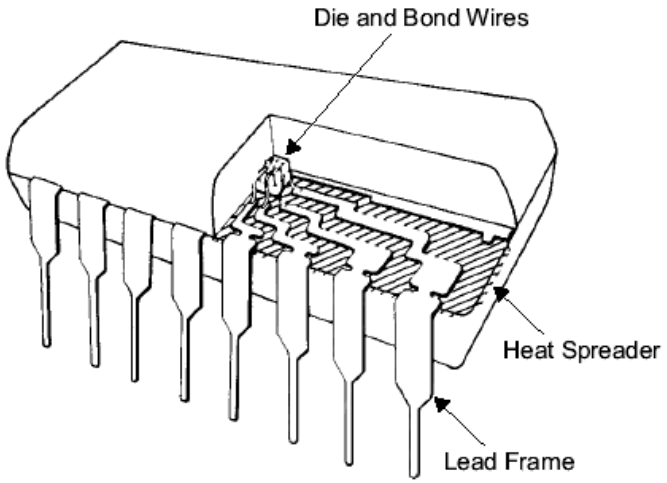
Package Types

- *Through-hole* pass through holes in a printed circuit board and are soldered from below.
- *Surface mount (SMT) packages* are soldered to the surface of a printed circuit board to alleviate pin inductance and hole size (pins density).



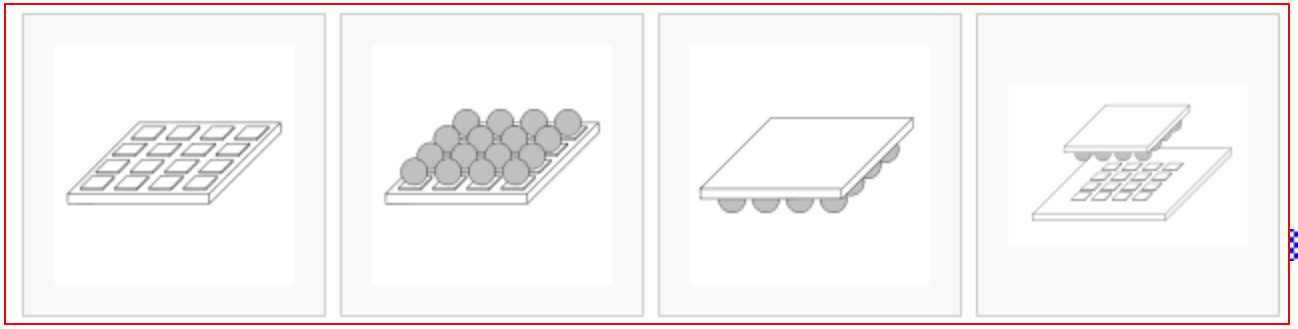
Chip-to-Package Bonding

- Traditionally, chip is surrounded by *pad frame*
  - Metal pads on 100 – 200 μm pitch (hundreds I/O)
  - Gold *bond wires* attach pads to package
  - *Lead frame* distributes signals in package
  - Metal *heat spreader* helps with cooling



Advanced Packages

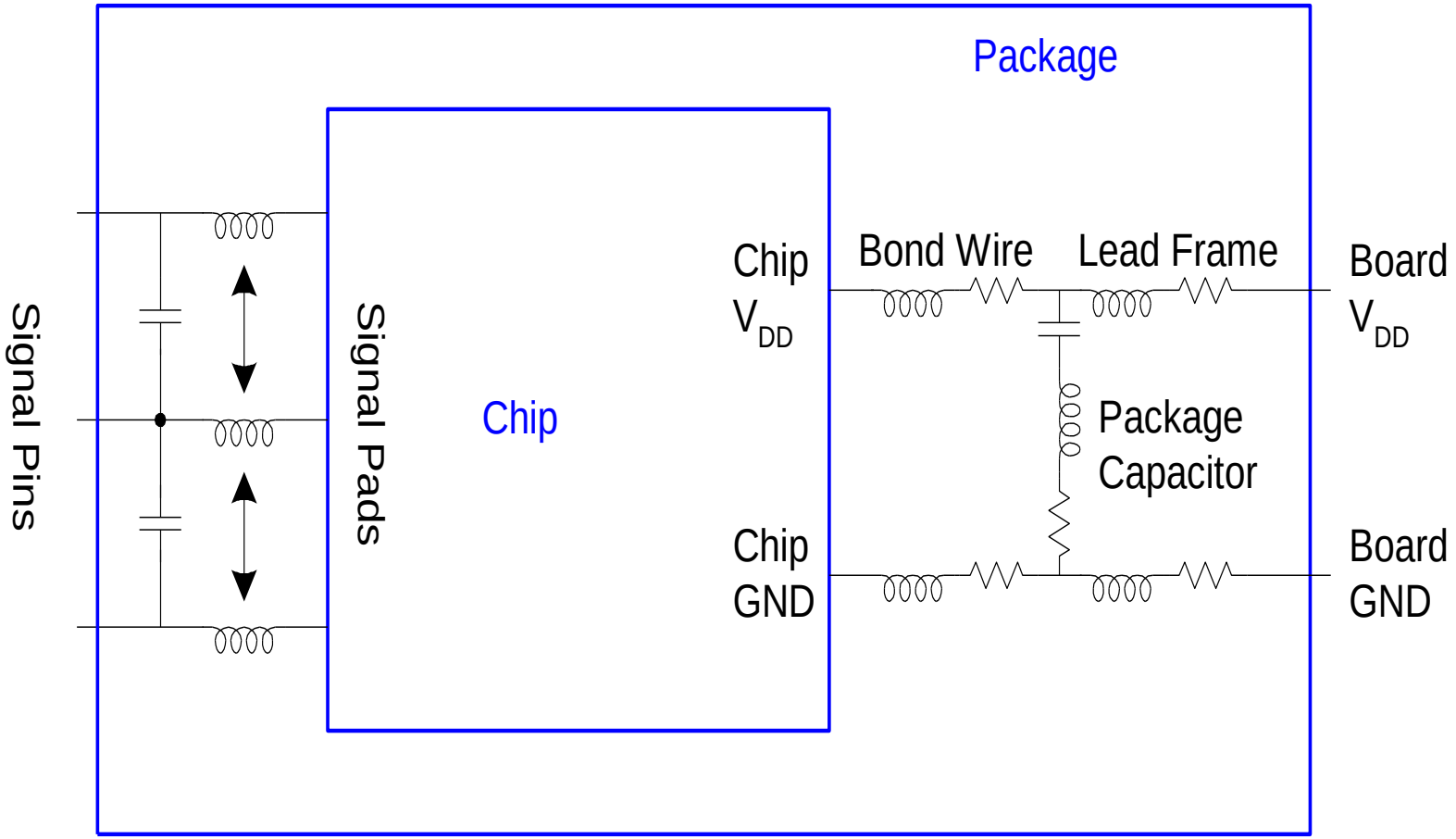
- Bond wires contribute parasitic inductance
- Fancy packages have many signal, power layers
  - Like tiny printed circuit boards
- *Flip-chip* places connections across surface of die rather than around periphery
  - Top level metal pads covered with solder balls
  - Chip flips upside down
  - Carefully aligned to package (done blind!)
  - Heated to melt balls
  - Also called *C4* (Controlled Collapse Chip Connection)



Package Parasitics

- Bond wires and lead frame contribute parasitic inductance to the signal traces.
- Inductive, capacitive coupling.
- Use many V_{DD}, GND in parallel
  - Inductance, I_{DD}

Package Parasitics



Heat Dissipation

- 60 W light bulb has surface area of 120 cm^2
- Itanium 2 die dissipates 130 W over 4 cm^2
  - Chips have **enormous power densities**
  - Cooling is a serious challenge
- Package spreads heat to larger surface area
  - Heat sinks may increase surface area further
  - Fans increase airflow rate over surface area
  - Liquid cooling used in extreme cases ($$$)

Thermal Resistance

- $\Delta T = \theta_{ja} P$
  - ΔT: temperature rise on chip
  - θ_{ja}: thermal resistance of chip junction to ambient (C/W)
  - P: power dissipation on chip
- Thermal resistances combine like resistors
  - Series and parallel
- $\theta_{ja} = \theta_{jp} + \theta_{pa}$
  - Series combination from the die to the package θ_{jp} and from package to the air θ_{pa}.

Heat Example

- Your chip has a heat sink with a thermal resistance to the package of 4.0° C/W.
- The resistance from chip to package is 1° C/W.
- The system box ambient temperature may reach 55° C.
- The chip temperature must not exceed 100° C.
- What is the maximum chip power dissipation?
- Solution:
  - $\theta_{ja} = \theta_{jp} + \theta_{pa} = (1 + 4) = 5$ C/W
  - $\Delta T = \theta_{ja} P$
  - (100-55 C) = 5 P
  - ➔ P=9W

Temperature Sensor

- Monitor die temperature and throttle performance if it gets too hot
  - **T**: absolute temp, **I_c** collector current, base emitter voltage **V_{BE}**

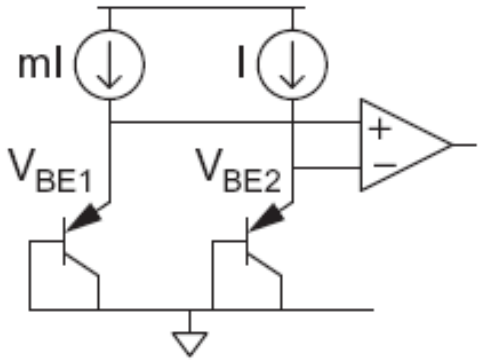
$$I_c = I_s e^{\frac{qV_{BE}}{kT}} \rightarrow V_{BE} = \frac{kT}{q} \ln \frac{I_c}{I_s}$$

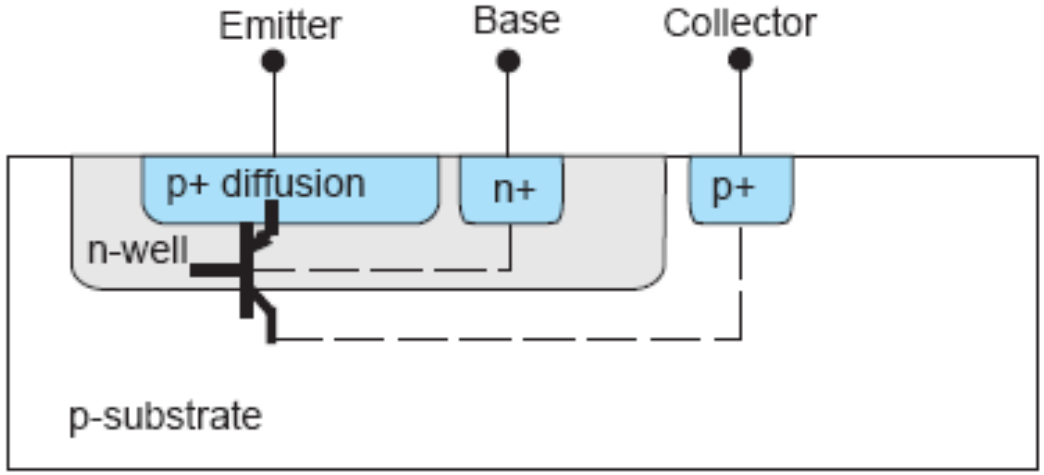
$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q}\left(\ln \frac{I_{c1}}{I_s} - \ln \frac{I_{c2}}{I_s} \right) = \frac{kT}{q}\left(\ln \frac{I_{c1}}{I_{c2}} \right) = \frac{kT}{q} \ln m$$

  - q: charge on electron, k: Boltzmann constant, Is: function of transistor geometry and processing.

Temperature Sensor

- Use a pair of pnp bipolar transistors
  - Vertical pnp available in CMOS





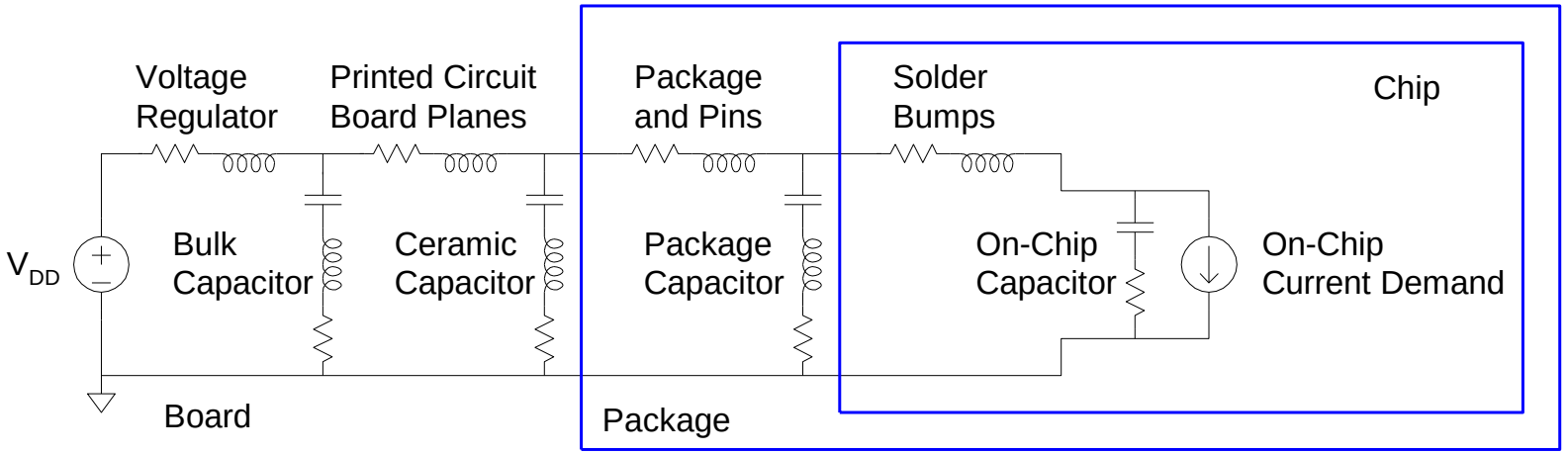
- **Voltage difference is proportional to absolute temp**
  - Measure with on-chip A/D converter

13.3 Power Distribution

- Power Distribution Network functions
  - Carry current from pads to transistors on chip
  - Maintain stable voltage with low noise
  - Provide average and peak power demands
  - Provide current return paths for signals
  - Avoid electromigration & self-heating wearout
  - Consume little chip area and wire
  - Easy to lay out

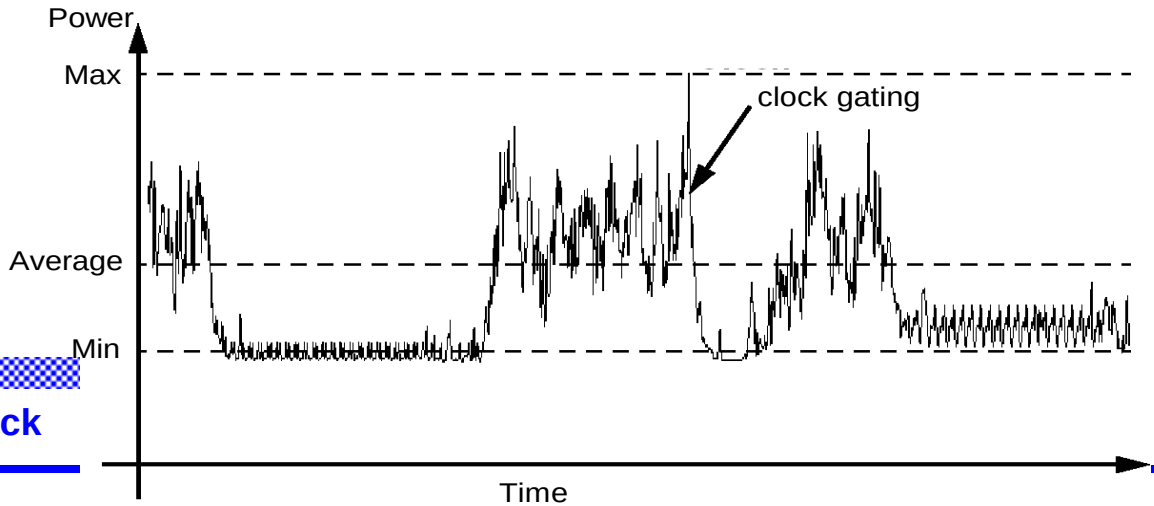
Power System Model

- Power comes from regulator on system board
  - Board and package add parasitic R and L
  - Bypass capacitors help stabilize supply voltage
  - But capacitors also have parasitic R and L
- Simulate system for time and frequency responses



Power Requirements

- $V_{DD} = V_{DDnominal} - V_{drop}$
- Want V_{droop} < +/- 10% of V_{DD}
- Sources of V_{drop}
  - IR drops (Caused by the resistance of distribution network)
  - L di/dt noise: caused by the inductance of the distribution network)
- I_{DD} changes on many time scales



IR Drop

- IR drop:
  - R: resistance of the power distribution network
  - I : is the draw current
  - Instantaneous drawing of current I causes voltage drop in the power supply equals to IR drop.
- IR Drop = I_{DD} $_{\text{Power Supply}}$ × Impedance $_{\text{Power Supply}}$
- A chip draws 24 W from a 1.2 V supply. The power supply impedance is 5 mΩ. What is the IR drop?
  - **I_{DD} = 24 W / 1.2 V = 20 A**
  - **IR drop = (20 A)(5 mΩ) = 100 mV**

L di/dt Noise

- The change in current flows through the inductance of the printed circuit board and package causes L di/dt
- The drop in the power supply due to drawing current
  - $V(t)_{\text{drop in power supply}} = L \times di / dt$
- A 1.2 V chip switches from an idle mode consuming 5W to a full-power mode consuming 53 W. The transition takes 10 clock cycles at 1 GHz. The supply inductance is 0.1 nH. What is the L di/dt droop?
- **$\Delta I = \Delta W/V = (53\ W - 5\ W)/(1.2\ V) = 40\ A$**
- **$\Delta t = 10$ cycles * (1 ns / cycle) = 10 ns**
- **L di/dt drop = (0.1 nH) * (40 A / 10 ns) = 0.4 V**

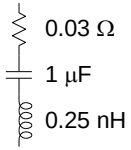
Bypass Capacitors

- Need low supply impedance at all frequencies
- Ideal capacitors have impedance decreasing with ω
- Real capacitors have parasitic R and L
  - Leads to resonant frequency of capacitor

$$Z = \frac{1}{j\omega C} + R + j\omega L$$

This impedance has a minimum of $Z = R$ at the self-resonant frequency of

$$f_{\text{resonant}} = \frac{\omega_{\text{resonant}}}{2\pi} = \frac{1}{2\pi\sqrt{LC}}$$



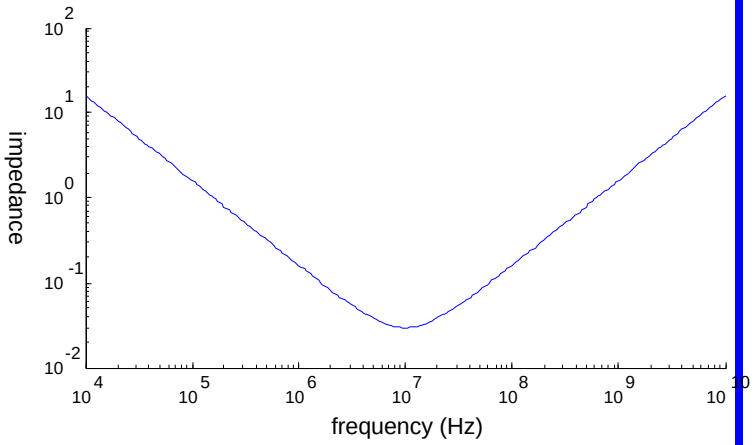


Figure 13.11 plots the magnitude of the impedance of a 1 μF capacitor with 0.25 nH of series inductance and 0.03 Ω of series resistance. The capacitor has low impedance near its resonant frequency of 10 MHz, but higher impedance elsewhere.

Bypass Capacitors

Example:

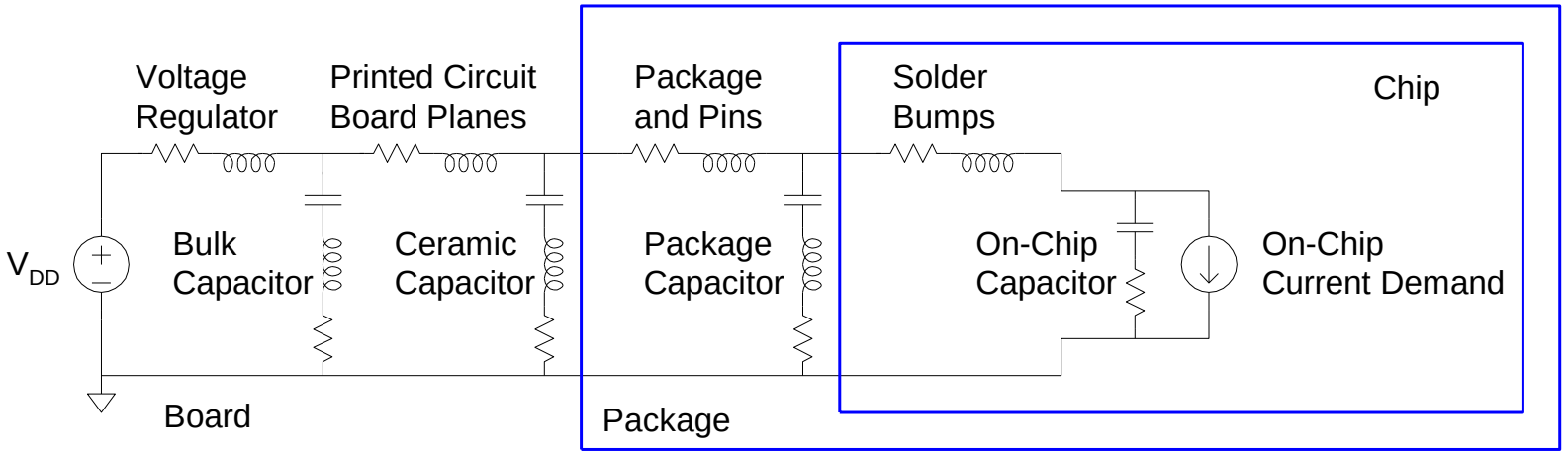
How much bypass capacitance is needed to supply a sudden current spike of 40 A for 1 ns with no more than a 200 mV supply droop?

SOLUTION: We solve

$$I = C\frac{\Delta V}{\Delta t} \Rightarrow C = \frac{(40\text{ A})(1\text{ ns})}{0.2\text{ V}} = 200\text{ nF}$$

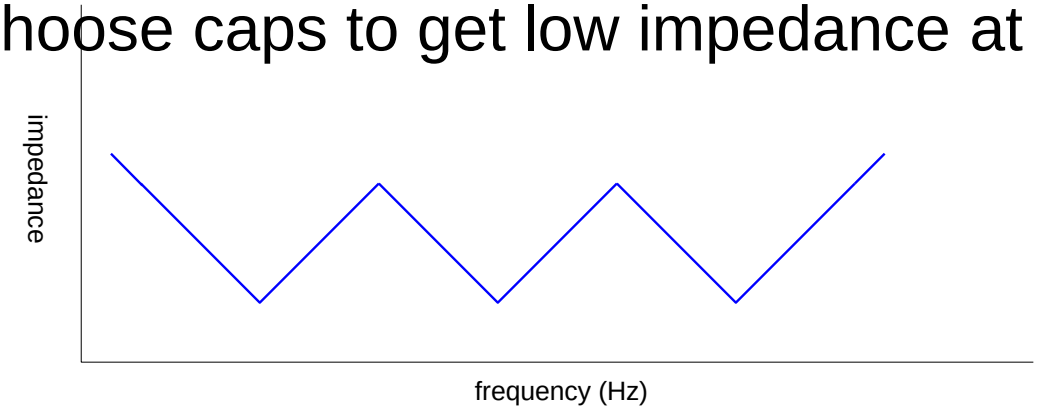
Power System Model

- Power comes from regulator on system board
  - Board and package add parasitic R and L
  - Bypass capacitors help stabilize supply voltage
  - But capacitors also have parasitic R and L
- Simulate system for time and frequency responses



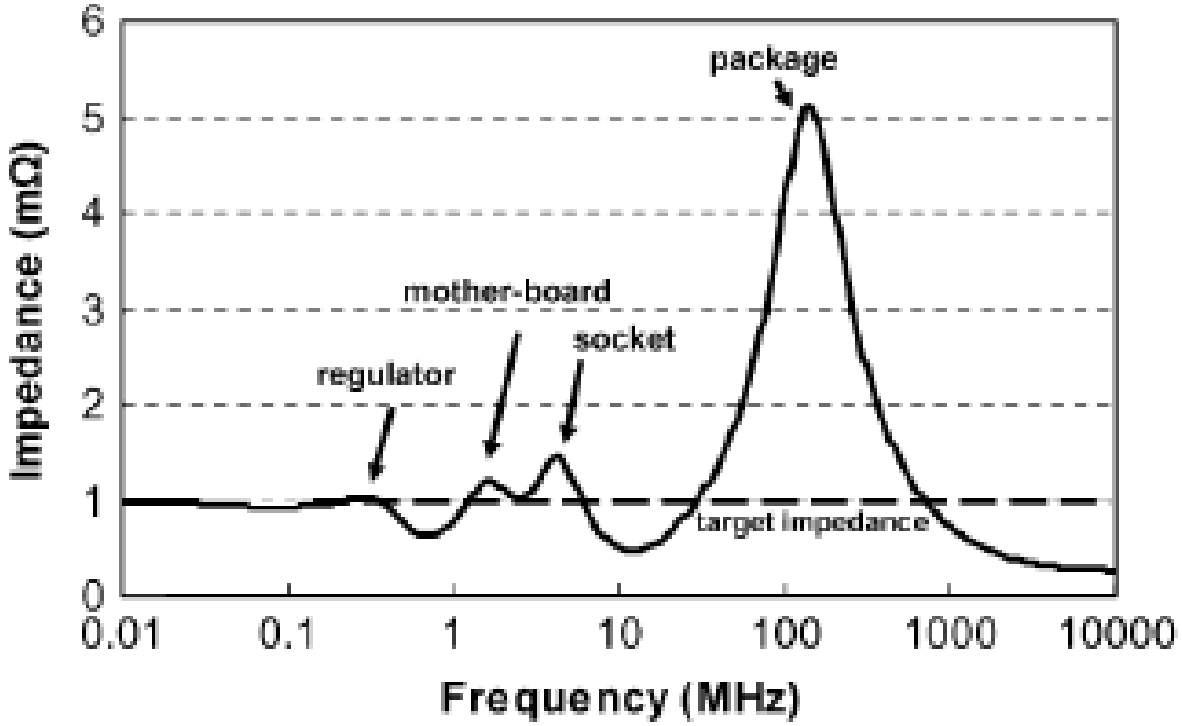
Frequency Response

- Multiple capacitors in parallel
  - Large capacitor near regulator has low impedance at low frequencies
  - But also has a low self-resonant frequency
  - Small capacitors near chip and on chip have low impedance at high frequencies
- Choose caps to get low impedance at all frequencies



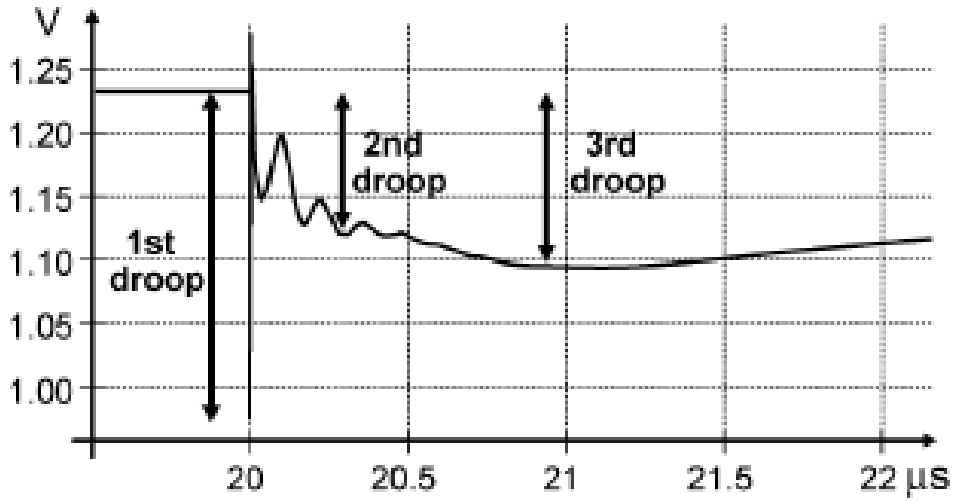
Example: Pentium 4

- Power supply impedance for Pentium 4
  - Spike near 100 MHz caused by package L



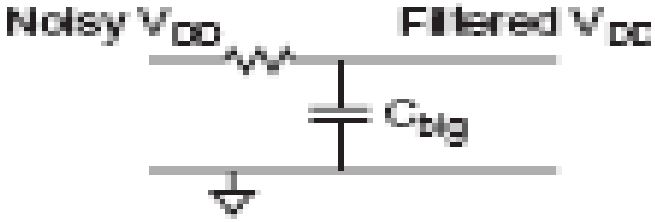
Example: Pentium 4

- Step response to sudden supply current chain
  - 1st droop: on-chip bypass caps
  - 2nd droop: package capacitance
  - 3rd droop: board capacitance



Power Supply Filtering

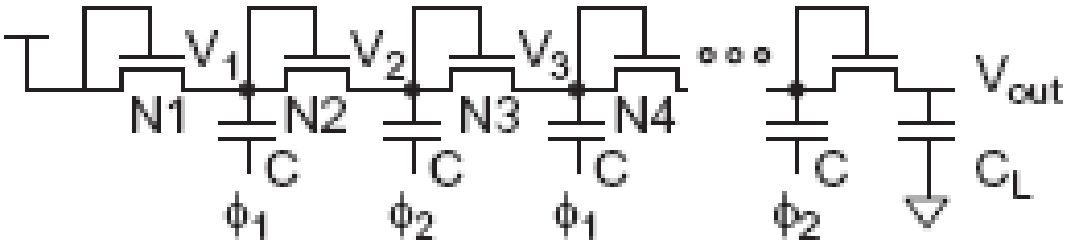
- Certain structures such as the phase-locked loop (PLL), clock buffers, and analog circuits are particularly sensitive to power supply noise.
- An RC power supply filter circuit that eliminates the high-frequency noise on the local supply.



- The resistance of this wire must be low enough to carry the current demand of the local circuitry without excessive IR drop, yet low enough to produce an RC time constant that will filter noise at frequencies of interest.

Charge Pumps

- Sometimes a different supply voltage is needed but little current is required
  - 20 V for Flash memory programming
  - Negative body bias for leakage control during sleep
- Generate the voltage on-chip with a charge pump



$$V_{out} = N\left[\frac{CV_{DD} - \frac{I_{out}}{f}}{C + C_s} - V_t\right]$$

Energy Scavenging

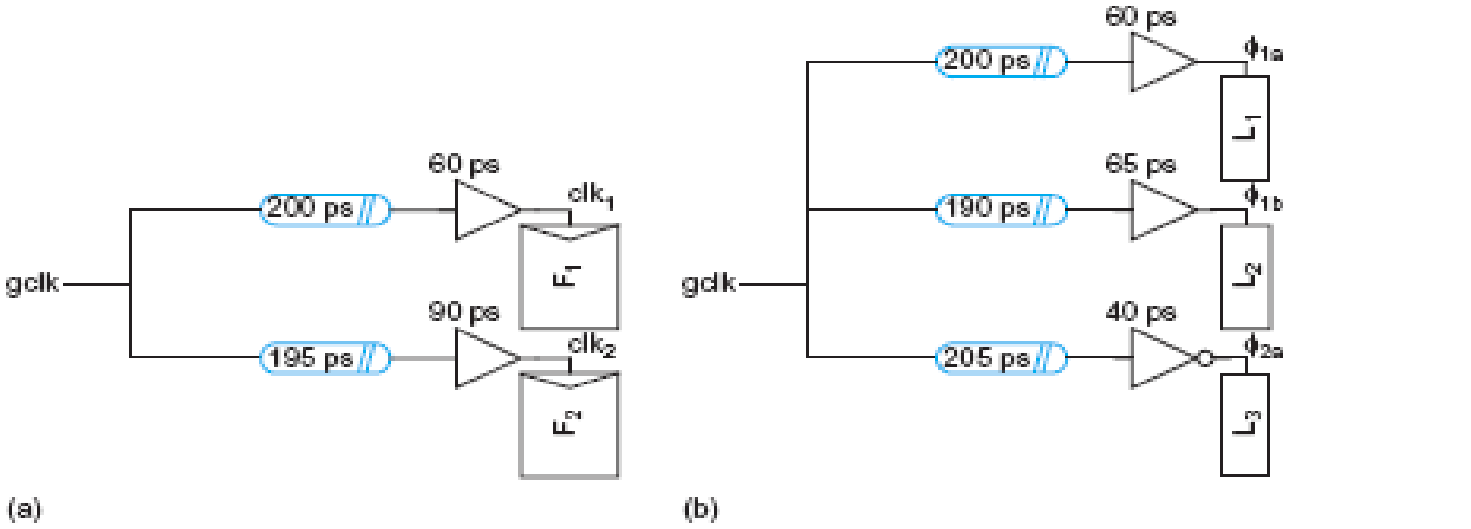
- Ultra-low power systems can scavenge their energy from the environment rather than needing batteries
  - Solar calculator (solar cells)
  - RFID tags (antenna)
  - Tire pressure monitors powered by vibrational energy of tires (piezoelectric generator)
- Thin film microbatteries deposited on the chip can store energy for times of peak demand

13.4 Clock Distribution

- On a small chip, the clock distribution network is just a wire
  - And possibly an inverter for clkb
- On practical chips, the RC delay of the wire resistance and gate load is very long
  - Variations in this delay cause clock to get to different elements at different times
  - This is called *clock skew*
- Most chips use repeaters to buffer the clock and equalize the delay
  - Reduces but doesn't eliminate skew

Clock Skew

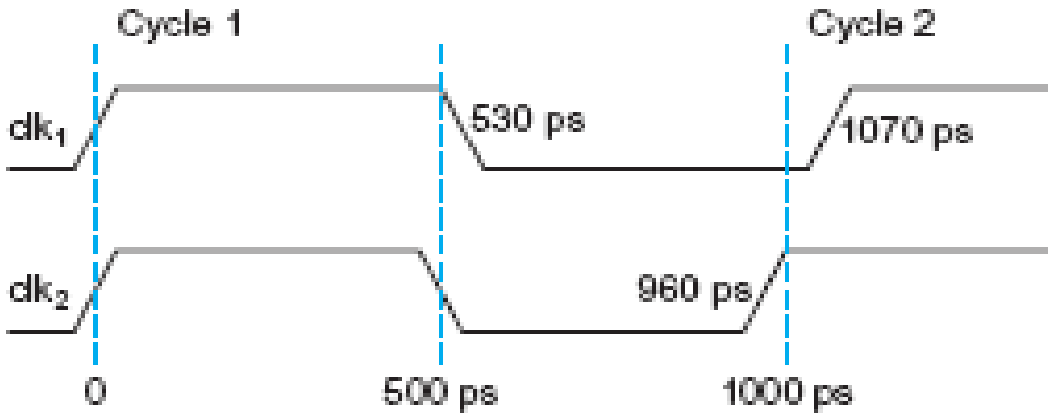
- Skew is the *difference between the nominal and actual inter-arrival time of a pair of physical clocks.*



  - (a) clock skew is 25 ps
  - (b) $t_{skew}^{\phi_{1a}\phi_{1b}} = 5$ ps; $t_{skew}^{\phi_{1a}\phi_{2a}} = 15$ ps; $t_{skew}^{\phi_{1b}\phi_{2a}} = 10$ ps

Clock Skew

- Clock skew can also be measured between different edges of the clock or between different cycles.

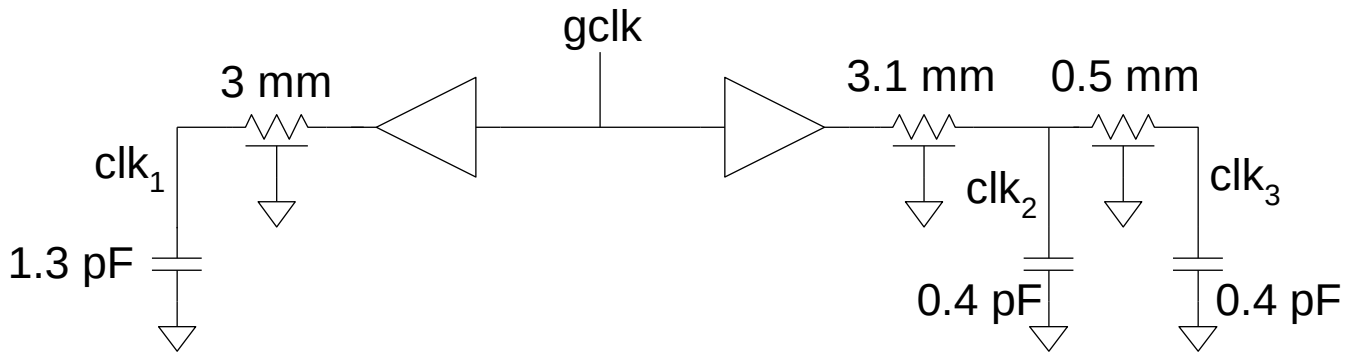


$$t_{skew}^{clk_1,clk_1}(r,r,0) = 0 \text{ ps}; \quad t_{skew}^{clk_1,clk_1}(r,f,0) = 30 \text{ ps}; \quad t_{skew}^{clk_1,clk_1}(r,r,1) = 70 \text{ ps}$$

$$t_{skew}^{clk_1,clk_2}(r,r,0) = 0 \text{ ps}; \quad t_{skew}^{clk_1,clk_2}(r,f,0) = 0 \text{ ps}; \quad t_{skew}^{clk_1,clk_2}(r,r,1) = 40 \text{ ps}$$

Example

- Skew comes from differences in gate and wire delay
  - With right buffer sizing, clk_1 and clk_2 could ideally arrive at the same time.
  - But power supply noise changes buffer delays
  - clk_2 and clk_3 will always see RC skew



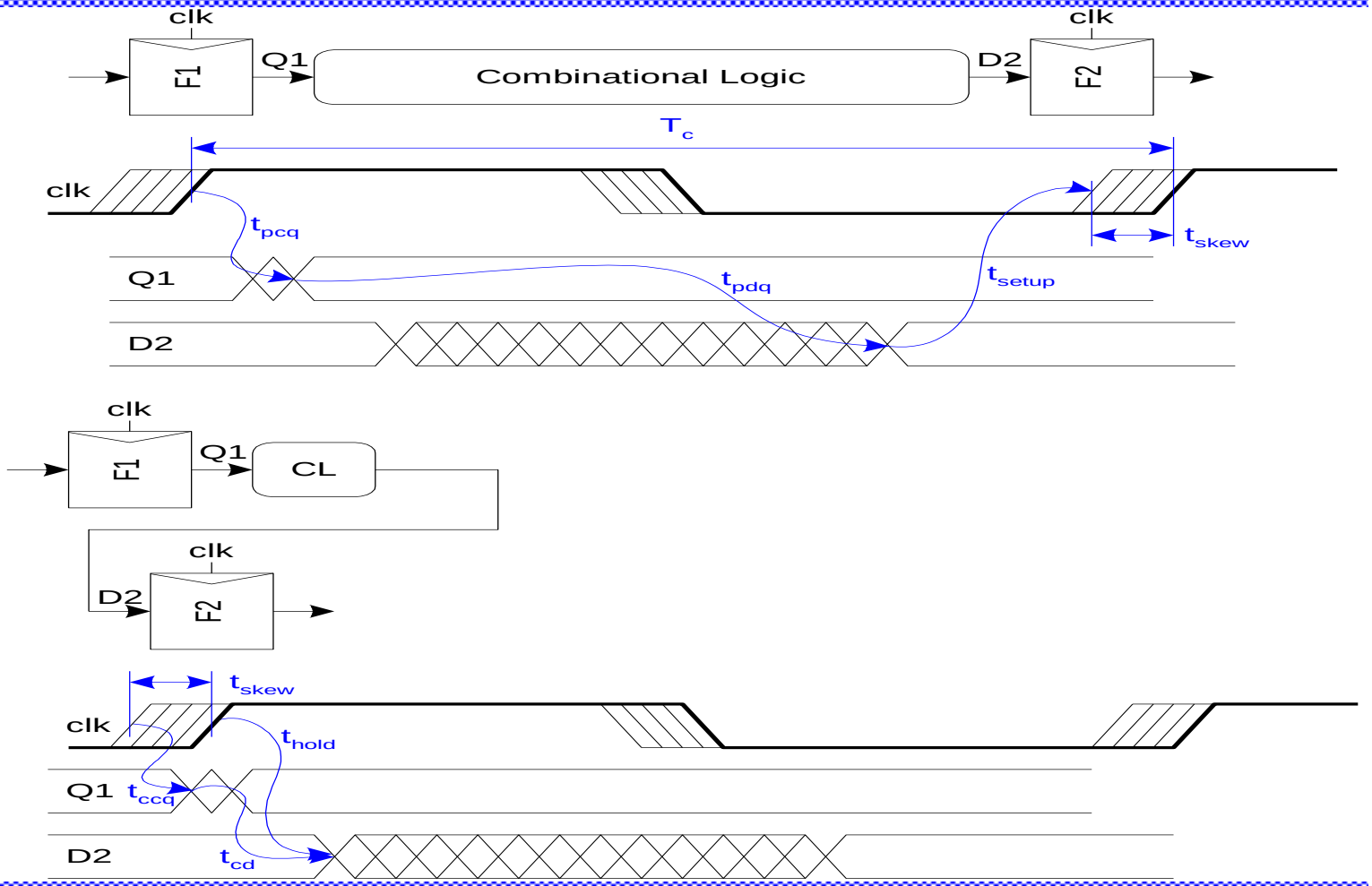
Review: Skew Impact (1)

- Ideally full cycle is available for work
- Skew adds sequencing overhead
- Increases hold time too

$$t_{pd} \leq T_c - \underbrace{\left(t_{pcq} + t_{\text{setup}} + t_{\text{skew}} \right)}_{\text{sequencing overhead}}$$

$$t_{cd} \geq t_{\text{hold}} - t_{ccq} + t_{\text{skew}}$$

Review: Skew Impact (2)



Solutions

- Reduce clock skew
  - Careful clock distribution network design
  - Plenty of metal wiring resources
- Analyze clock skew
  - Only budget actual, not worst case skews
  - Local vs. global skew budgets
- Tolerate clock skew
  - Choose circuit structures insensitive to skew

Global Clock Dist. Networks

- *Ad hoc*
- Grids
- H-tree
- Hybrid

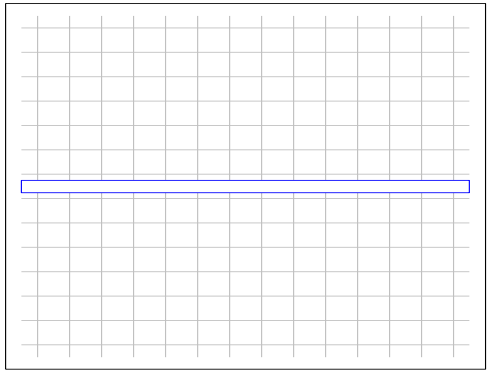
- Random skew (manufacture), drift (time-dependent environment variation : temperature), and jitter (high-frequency environment variation: power supply noise) from the clock distribution network are proportional to the delay through network because they are caused by process or environmental variations in the distribution elements. Designer should try to keep this distribution delay low.

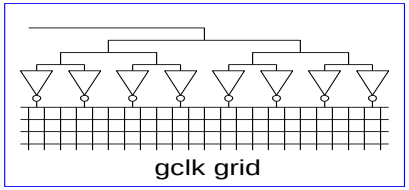
Clock Grids

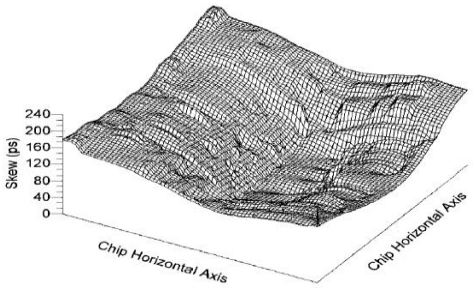
- Use grid on two or more levels to carry clock (mesh)
- Make wires wide to reduce RC delay
- Ensures low skew between nearby points
- But possibly large skew across die
- Grids can be routed early in the design without detailed knowledge of latch placement.
- However, grids do have significant systematic skew between the points closest to the drivers and the points farthest away. They also consume a large amount of metal resources and hence have a high switching capacitance and power consumption.

Alpha Clock Grids

Alpha 21064







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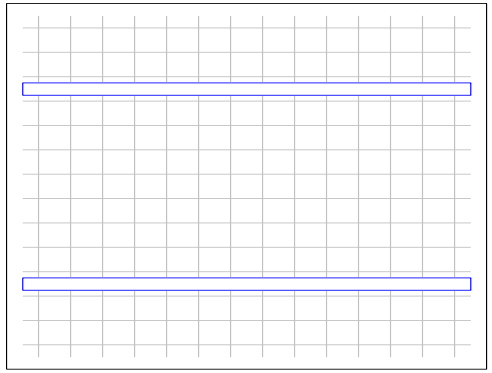

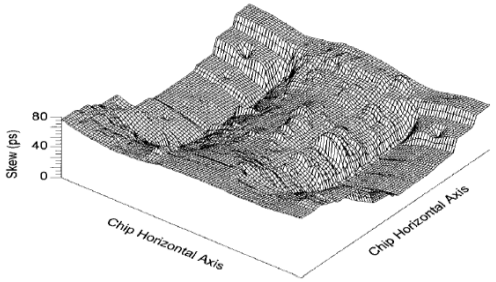

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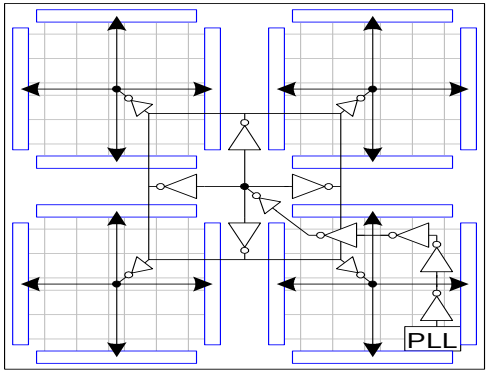

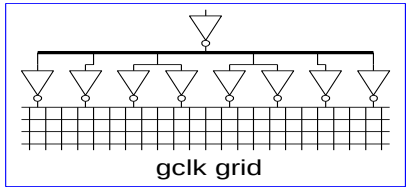

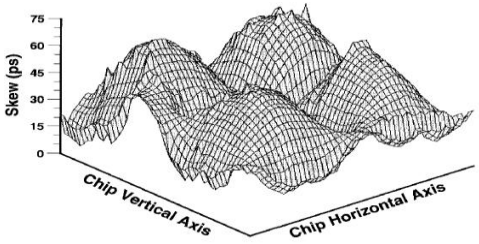

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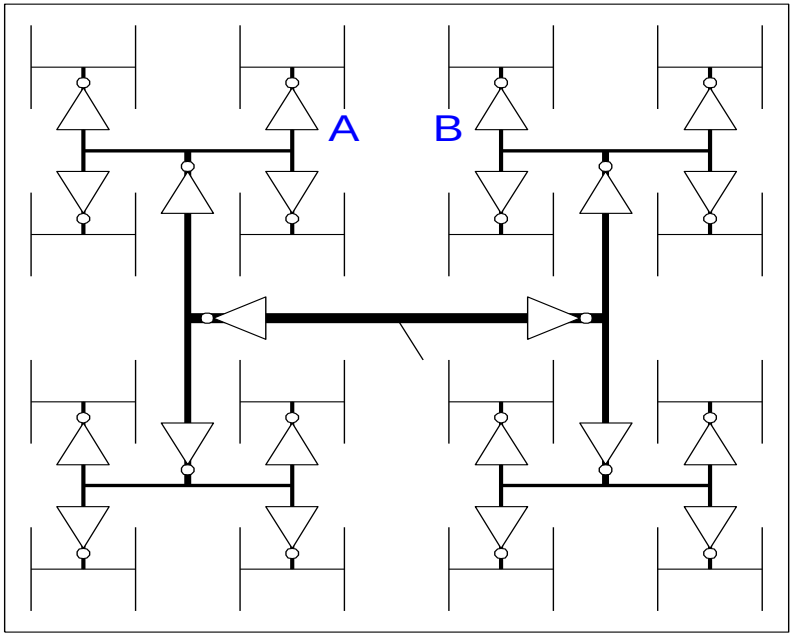
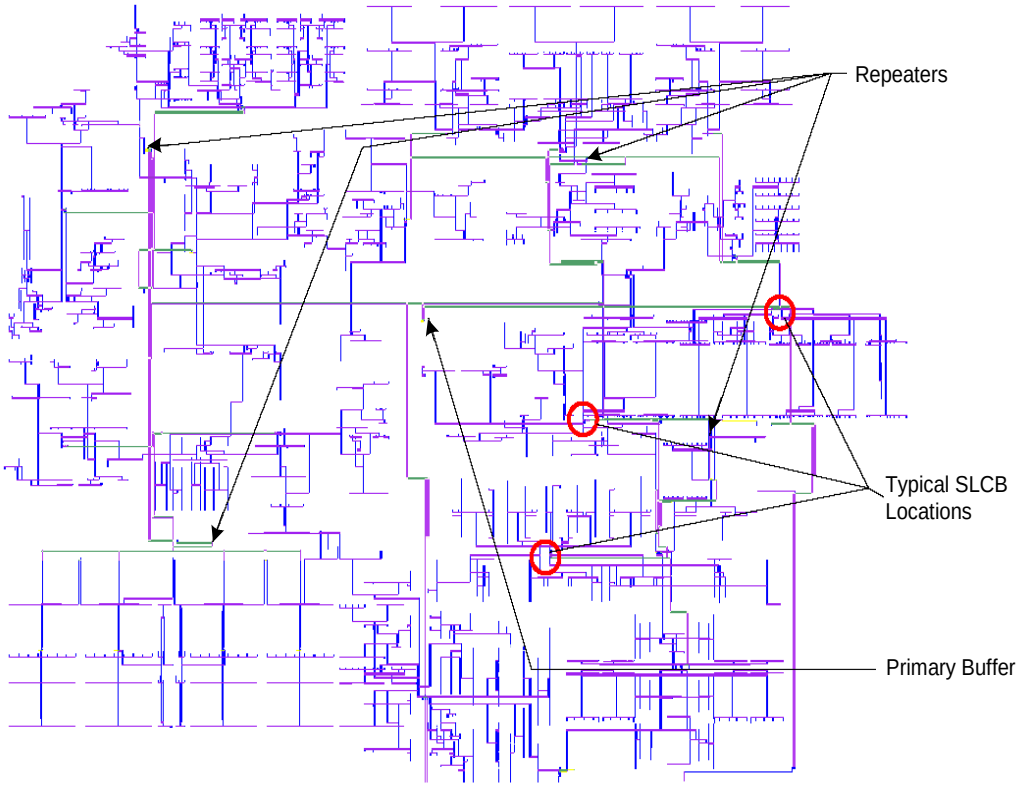
H-Trees

- Fractal structure has H-shape on each vertices
  - Gets clock arbitrarily close to any point
  - Matched delay along all paths
  - Buffers are added as repeaters
- Delay variations cause skew because load are not uniform.
- A and B might see big skew
- A drawback of H-trees is that they may have high random skew, drift, and jitter between two nearby points that are leaves of different legs of the tree.



Itanium 2 H-Tree

- Four levels of buffering:
  - Primary driver
  - Repeater
  - Second-level clock buffer
  - Gater
- Route around obstacles



Hybrid Networks

- Use H-tree to distribute clock to many points
- Tie these points together with a grid

- Ex: IBM Power4, PowerPC
  - H-tree drives 16-64 sector buffers
  - Buffers drive total of 1024 points
  - All points shorted together with grid