An-Najah National University
Faculty of Engineering
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Electrical and Computer Engineering
Department

جامعــة النجــاح الوطنيــة
كليـة الهندسـة و تكنولوجيا المعلومات
دائرة الهندسة الكهربائية والحاسوب

Due to 28/11/2022

HW1: (CLOs: VI)	Points:10

Complete the following VHDL design to implement a digital system that counts the number of bit transitions. This system can load an input data (10-bit) value when the **Load** input is asserted, and then compute the result on the positive edge of the input clock.

e.g.

Enable = 1 & Data = 1101011001 ==> 6 transitions

Enable = 0 ==> No change on the output count

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity Transition_Calculatoris
  port(   CLK, Load, Clear : in  std_logic;
          Data    : in  std_logic_vector(9 downto 0);
          Count   : out std_logic_vector(3 downto 0));
end Transition_Calculator;

architecture behavioral of Transition_Calculator is
```

Your design should include the following pins:

1. **CLK:** (positive edge trigger input clock)
2. **Load:** Synchronous **Active High** Load signals
3. **Clear:** Asynchronous **Active Low** Input (Clear the output)
4. **Count:** The output result which represents the number transitions in the loaded data.

Notes:

- Use behavioral description
- The calculation should be synchronous with the clock when the load signal is equal to 1. (*the number of transitions should be calculated in a single clock cycle at the rising edge*)

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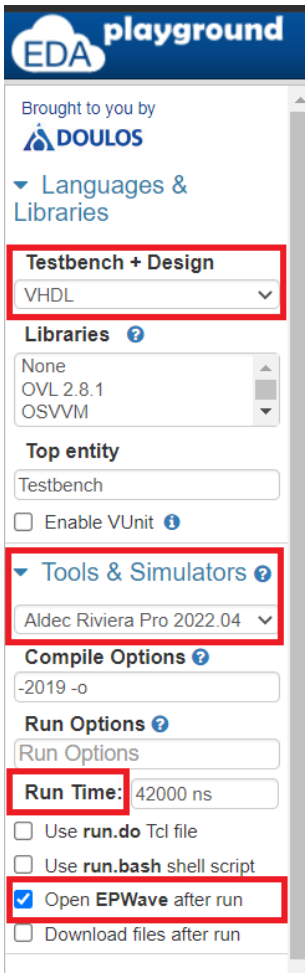
You have to submit two files:

1. A VHDL code to implement your Design.
2. A testbench file to simulate and test your design:
    a. You have to give a test case for the Asynchronous **Clear**,
    b. You have to cover all the possible cases for the input **Data** (1024 different cases)
        i. For each case you have to:
            1. Select a different value for the input **Data**
            2. Set the **Load** signal to **'1'**
            3. Wait for two clock cycles
    c. You have to give a test case to show that no change will occur when the **Load** signal is **'0'**.

Note: When you select the simulation tool to be "**Aldec Rivera Pro 2022.04**", do not forget to set the **Run Time** to be sufficient to cover the previous test cases.



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