Pipelined ARM

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PCSrc ID/EX WB EX/MEM Control WB MEM/WB WB M EX IF/ID Pipelined ARM Add Add Add result Shift Branch left 2 ALUSrc Instruction [28] Reg2Loc ► PC Address Read Read data 1 register 1 Read register 2 Registers Read data ALU ALU Instruction Read Address memory result data Data memory Write data Write data Instruction [31-0] Sign-MemRead extend Instruction ALU [31-21] control ALUOp Instruction [4-0]

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- The project for this course is implementing the pipelined version of ARM architecture
- So far in the semester, you have defined and tested all the sub-modules used in the pipelined ARM implementation: Fetch, IF/ID, Decode, Control Unit, ID/EX, Execute, EX/MEM, Data Memory, MEM/WB, and Write Back
- Now, you just have to instantiate all these modules and connect them inside your ARM module to create the pipeline

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Remember:

- Update your Fetch module to match the ARM implementation if you haven't already (details of this update are available as comments in the HW1-ARM file)
- Test your final ARM module to make sure that it executes the instructions correctly
- Even if you have implemented all the sub-modules correctly, you <u>may</u> notice some problems with the behaviour of the pipeline while testing the module and you <u>may</u> need to make some minor changes to fix these problems (What minor changes and are they even necessary? This time you're going to tell us)

INPUTS & OUTPUTS

The inputs and outputs of the ARM module are the same as the ones you defined for the ARM module in HW3:

ARM:

Input: clk(1 bit)

THANK YOU & GOOD LUCK!