Chittagong University of Engineering and Technology

Department of electrical and Electronic Engineering

Project Report

Course No: EEE 366

Course Name: Digital Electronics Sessional

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Remarks

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Level: 3

Term: 2

Section: A

Group: A1

Task-1: Use 4 bit Synchronous Up Down Counter With Load and Reset

Simulation Output:

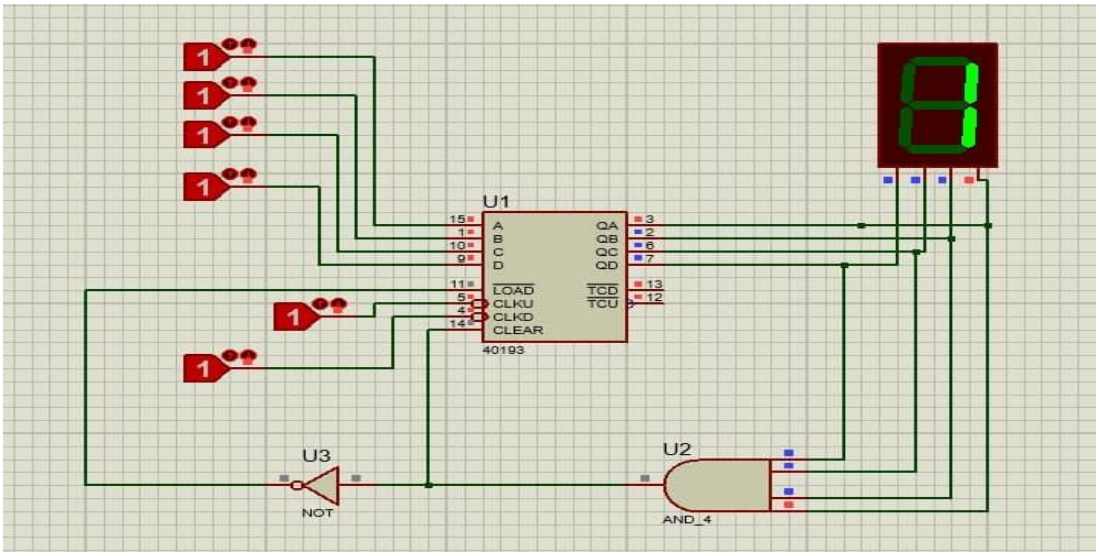

Fig.01. 4-bit synchronous up counter. This counted 0,1,2,3,4,…,14,15. Here output pins QA, QB, QC, QD got cleared after the output is 15(1111). I incremented the output by altering the logic state of CLOCK UP pin. CLOCK DOWN pin will be always in logic 1 state.

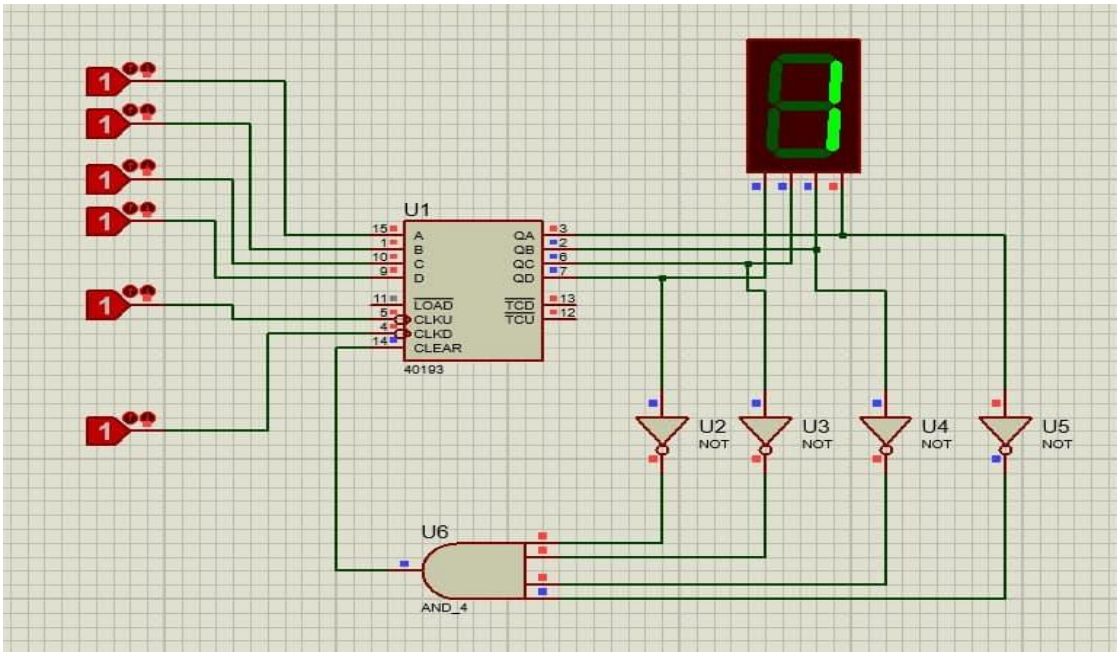

Fig.02. 4-bit synchronous down counter. This counted 15,14,…,3,2,1,0. I decremented the output by altering the logic state of CLOCK DOWN pin. CLOCK UP pin will always be in logic 1 state.

Task-2:

You will design 2 counter.

i. First one will count like the following sequence

ii. Second one will count in reverse direction

Last Digit of ID	Counting Sequence
0	0,3,4,5,0,3,4,5……..
1	0,1,4,5,6,0,1,4,5,6……..
2	0,1,2,5,6,7,0,1,2,5,6,7……
3	0,1,2,3,6,7,8,0,1,2,3,6,7,8……
4	……
5	……
6	……
7	……
8	……
9	0,1,2,3,4,5,6,7,8,9,12,13,14, 0,1,2,3,4,5,6,7,8,9,12,13,14,

Simulation Output:

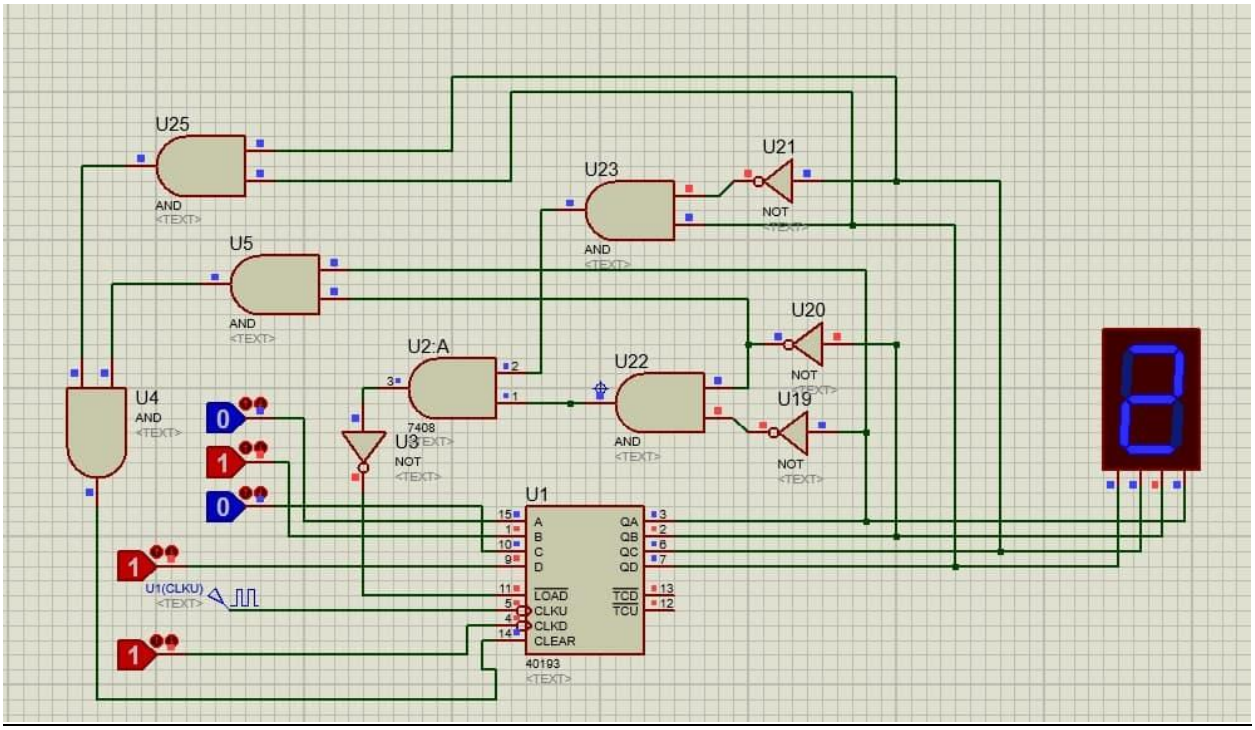

Fig.3. Up counter which counts 0,1,2,3,4,5,6,7,10,11,12 and then from 0 again. Here when outputs QD, QC, QB, QA turns into 8(1000 in binary), active low pin LOAD pin gets activated, then loads the input A, B, C, D into output. In my case, input is 10(1010 in binary). So after having 7 in output we will find 10,11,12 in output. When the output will turn into 13(1101 in binary) the clear pin will get activated and we will find 0 in output. Output will be incremented again

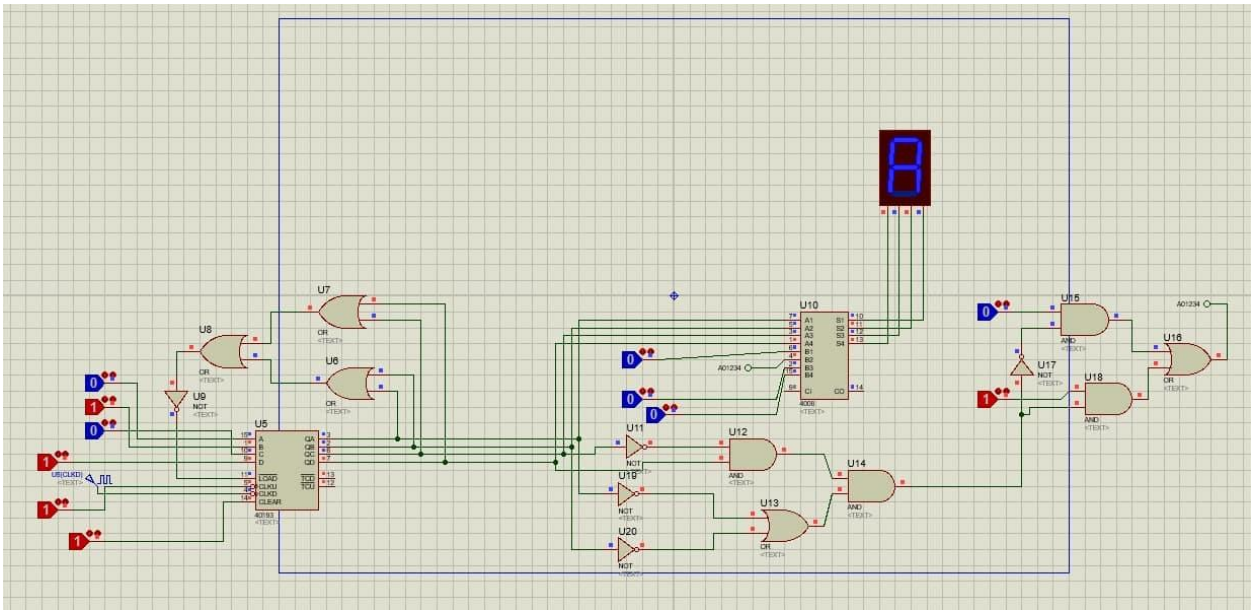

Fig.04. Down counter. Seven segment display is connected in 10,11,12,13 pins of 4008 IC. 4008 IC is adder circuit. 4 inputs are applied in A, B, C, D pins. 4008 IC adder circuit and 40193 IC of counter is used. After giving the output 0(0000), IC 40193 gives the output 10(A), which with the help of IC 4008 turns into 12(C) on display. Then IC 40193 gives output 9,8. Using K map a logic gate is designed to give output 1 for the input of 1010(10),1001(9),1000(8) and output 0 for 0000(0) to 0111(7) making the count down like 7,6,5,4,3,2,1 and then again 0.