COMPUTER ARCHITECTURE (CIE 439)

PROJECT1: ARM 1 SIMULATION

Description:

The following figure shows the ARM I architecture, and you are required to do the following:

1- Simulate this architecture in Logisim, System Verilog or any other hardware simulator.
2- Implement the hardware for this architecture. (**Bonus**)

The deadline for this project is 20 Dec. 2025.

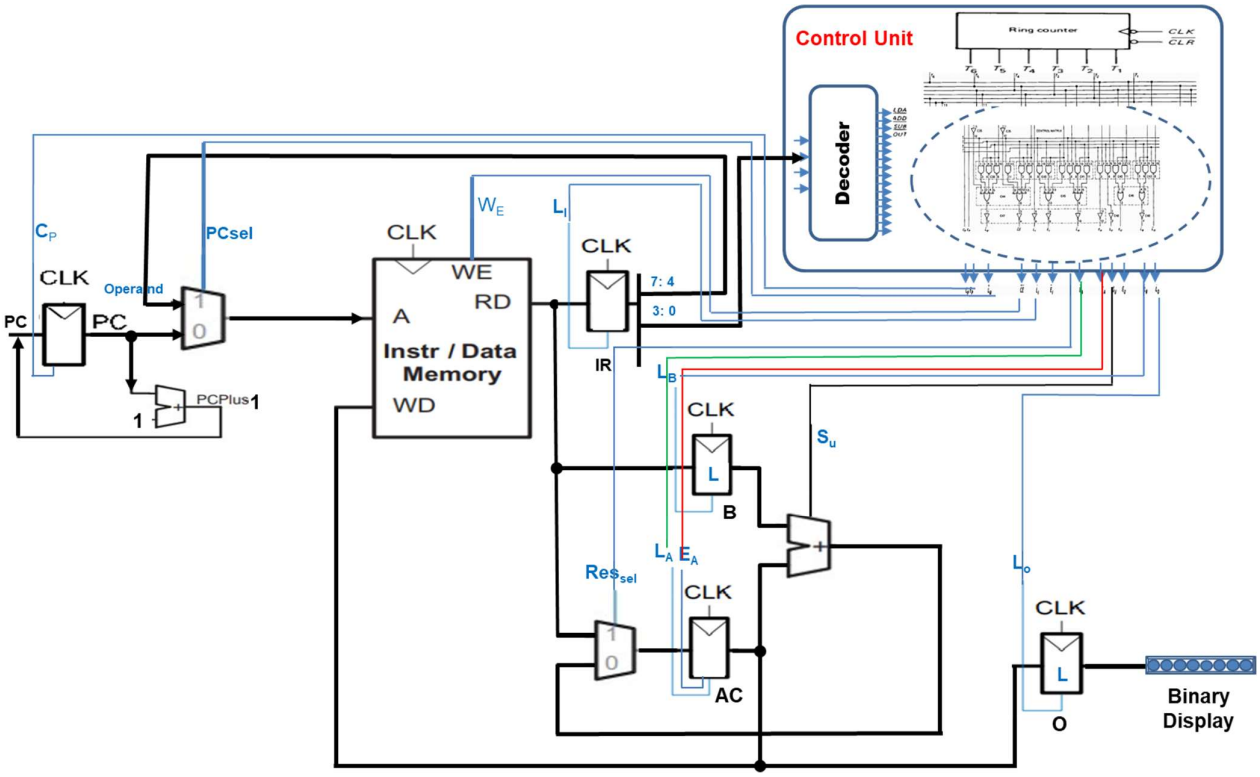

Figure 1: ARM I architecture

Deliverables:

1- Simulation file which contains the design of the ARM 1 architecture.
2- Report (*.pdf file) which shows your work on Simulator.
3- The video which demonstrates how your hardware operates.

PROJECT 2: PIPELINED ARM PROCESSOR

Description:

Implement the pipelined ARM processor using system Verilog. The block diagram of the processor is given in Fig. 2. The processor should support the following instructions:

- **Data processing instructions** where the second source can be either an immediate value or a source register, with no shifts. The data processing instructions must include ADD, SUB, AND, ORR, BIC, and EOR. The Arithmetic Logic Unit (ALU) must be extended to support all these instructions but try to minimize the number of logic gates in the ALU as much as you can.
- **The LDR and STR instructions** with positive immediate offset (offset mode).
- **Branch instruction**

Also, the processor must **handle** the following **hazards**:

- Read After Write (**RAW**) Hazard
- **LDR** Hazard
- **Control** Hazards due to Branch or PC write

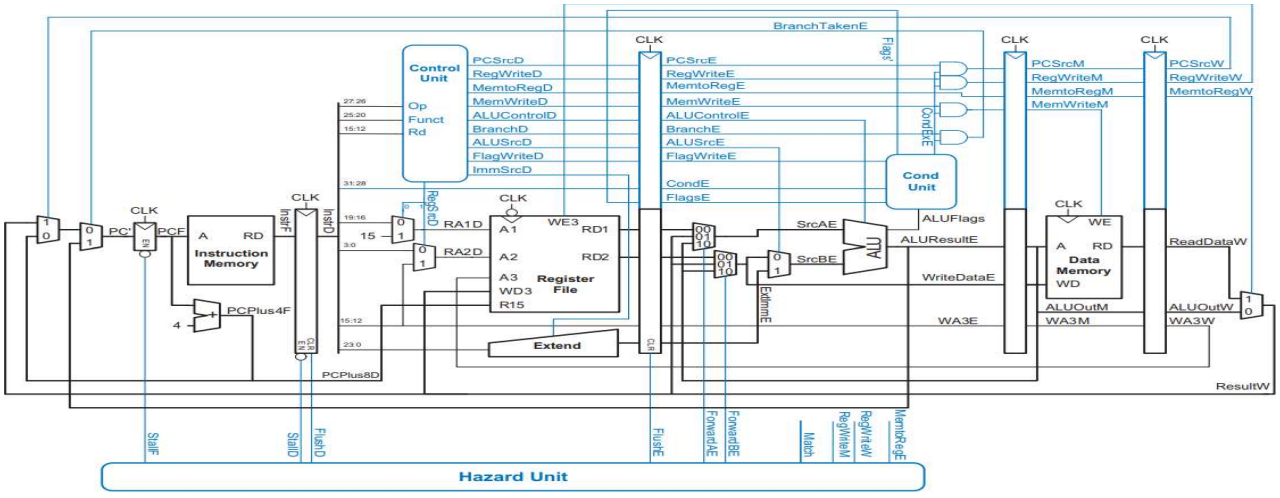

Figure 2: The pipelined ARM processor with control unit and Hazard unit

To test the functionality of the processor, a test assembly program must be written and stored in the instruction memory. This program must test all the above- mentioned instructions. Also, the program must show the ability of the processor to overcome all the above-mentioned hazards.

Deliverables:

1. The system Verilog files of all the modules.
2. The test program, which must be written in both ARM assembly and machine language.

Guidelines:

- The project must be done in groups. (**1-20 students per group**)
- The groups must be sent to the TAs **before 1-Dec-2025**
- Power point slides that show the overall design with the simulation results of all the possible test scenarios (well explained)
- During the evaluation, each group must bring a laptop to run the designed processor using ModelSim.

Deadline:

The **project discussion** will be held in the last week before the final exams **(week 14 || Week 15)**. The exact date will be announced on google classroom

Grading:

According to the grading system outlined in the **course syllabus**, the two projects will be graded out of total **20 marks for both projects**. Additionally, a **bonus** of **5 marks** will be awarded to students who successfully complete the hardware implementation for Project #1.

Best Wishes