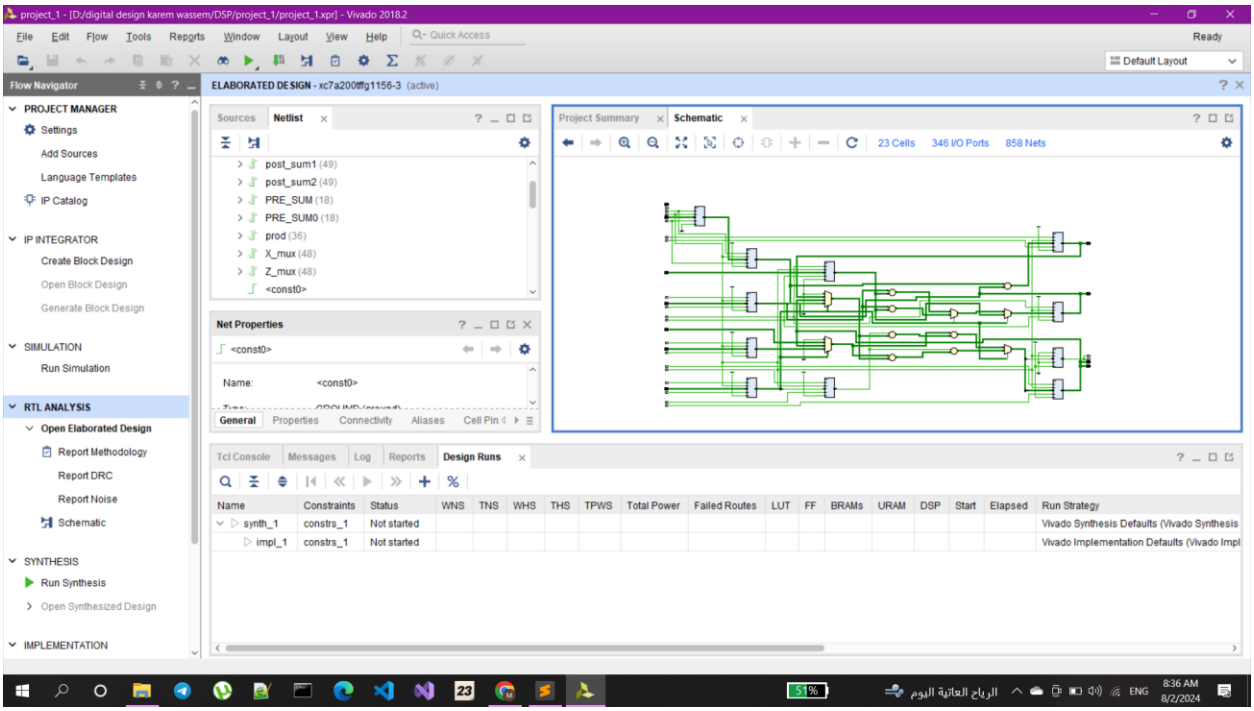
project_1 - [D:/digital design karem wassem/DSP/project_1/project_1.xpr] - Vivado 2018.2
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Open Block Design
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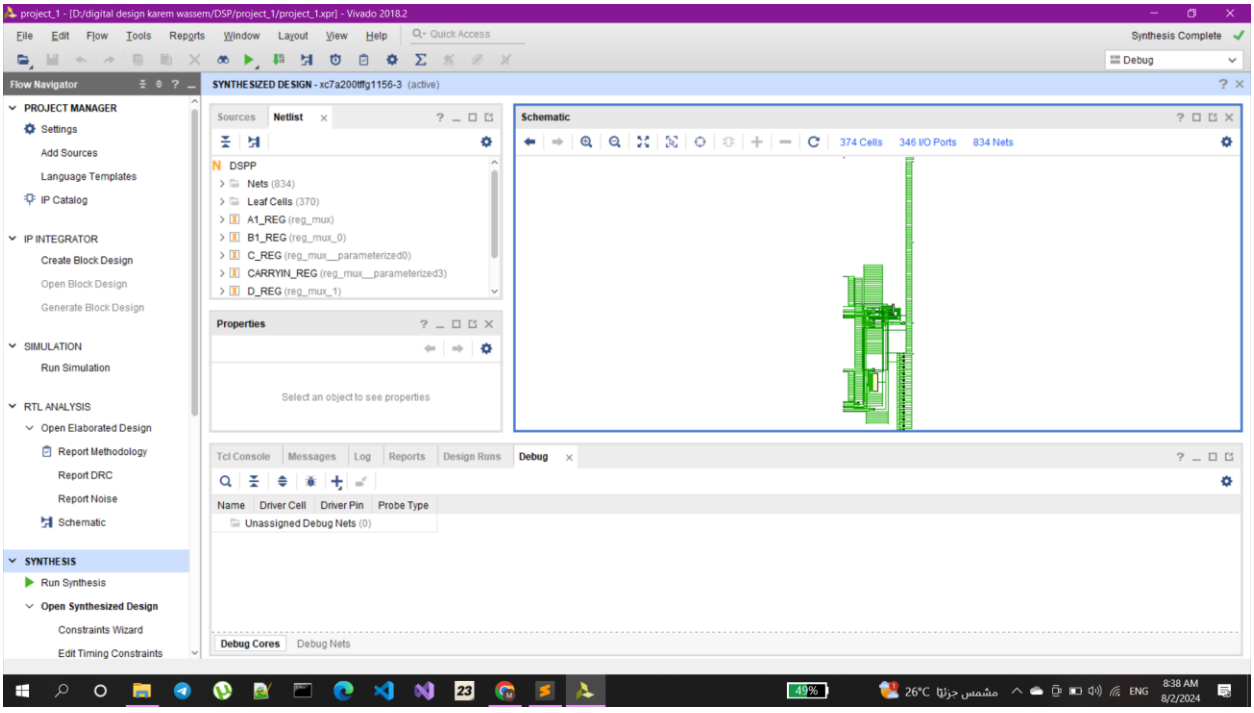
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
ELABORATED DESIGN - xc7a200tffg1156-3 (active)
Sources
Netlist
post_sum1 (49)
post_sum2 (49)
PRE_SUM (18)
PRE_SUM0 (18)
prod (36)
X_mux (48)
Z_mux (48)
<const0>
Net Properties
<const0>
Name: <const0>
General
Properties
Connectivity
Aliases
Cell Pin
Project Summary
Schematic
23 Cells
346 I/O Ports
858 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAMs
URAM
DSP
Start
Elapsed
Run Strategy
synth_1
constrs_1
Not started
Vivado Synthesis Defaults (Vivado Synthesis
impl_1
constrs_1
Not started
Vivado Implementation Defaults (Vivado Impl
51%
ENG
8:36 AM
8/2/2024


project_1 - [D:/digital design karem wassem/DSP/project_1/project_1.xpr] - Vivado 2018.2
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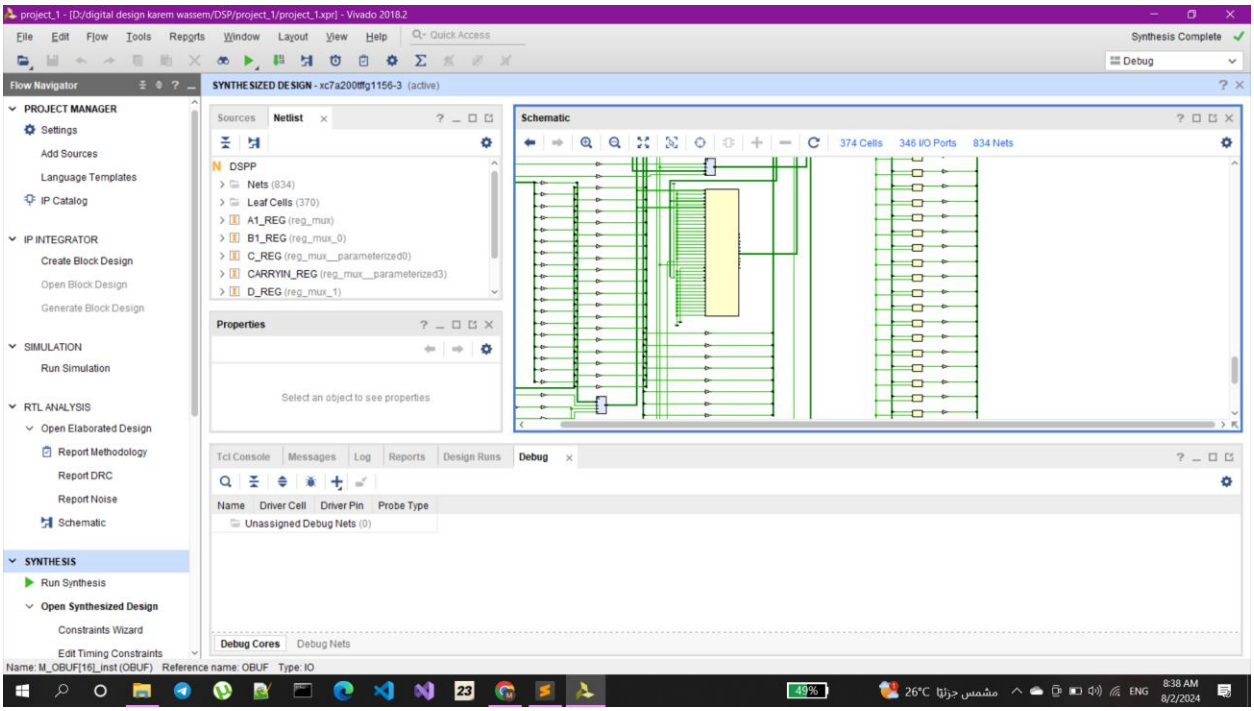
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
SYNTHESIZED DESIGN - xc7a200tffg1156-3 (active)
Sources
Netlist
DSPP
Nets (834)
Leaf Cells (370)
A1_REG (reg_mux)
B1_REG (reg_mux_0)
C_REG (reg_mux__parameterized0)
CARRYIN_REG (reg_mux__parameterized3)
D_REG (reg_mux_1)
Properties
Select an object to see properties
Schematic
374 Cells
346 I/O Ports
834 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Debug
Name
Driver Cell
Driver Pin
Probe Type
Unassigned Debug Nets (0)
Debug Cores
Debug Nets
49%
26°C
ENG
8:38 AM
8/2/2024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Quick Access
Synthesis Complete
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Create Block Design
Open Block Design
Generate Block Design
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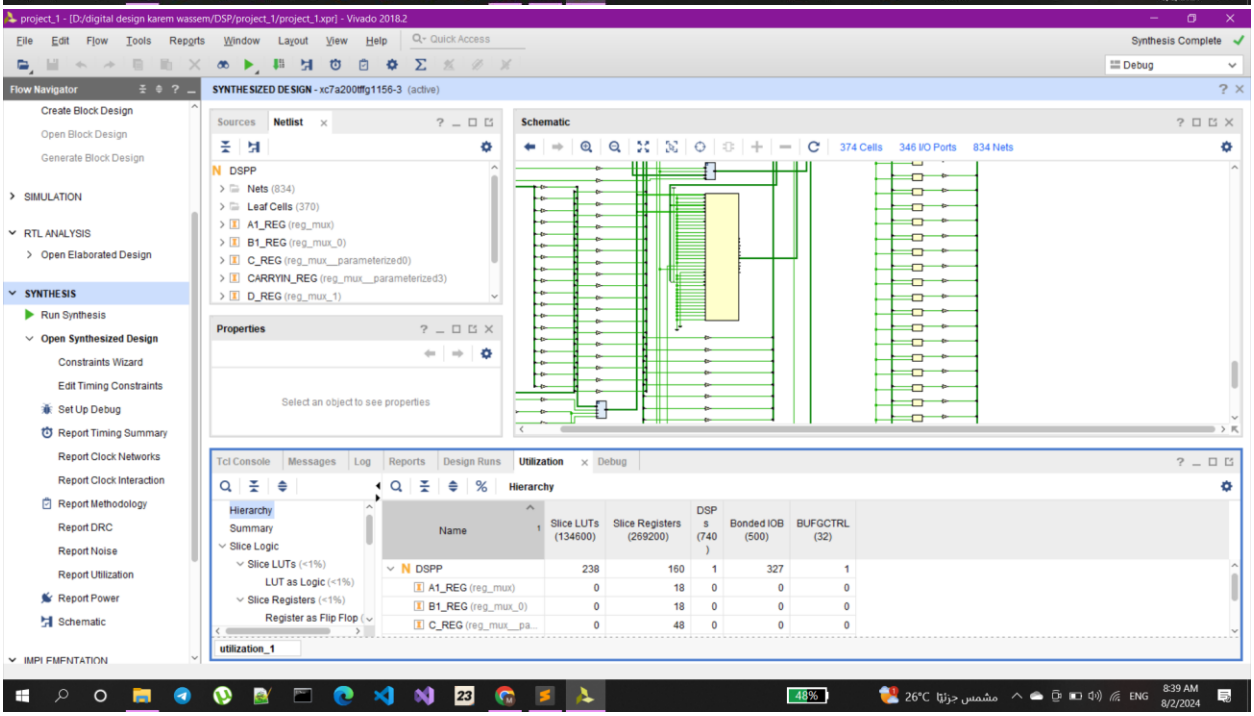
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
SYNTHESIZED DESIGN - xc7a200tffg1156-3 (active)
Sources
Netlist
DSPP
Nets (834)
Leaf Cells (370)
A1_REG (reg_mux)
B1_REG (reg_mux_0)
C_REG (reg_mux__parameterized0)
CARRYIN_REG (reg_mux__parameterized3)
D_REG (reg_mux_1)
Properties
Select an object to see properties
Schematic
374 Cells
346 I/O Ports
834 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Debug
Name
Driver Cell
Driver Pin
Probe Type
Unassigned Debug Nets (0)
Debug Cores
Debug Nets
Name: M_OBUF[16]_inst (OBUF) Reference name: OBUF Type: IO
49%
26°C
ENG
8:38 AM
8/2/2024


project_1 - [D:/digital design karem wassem/DSP/project_1/project_1.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
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Constraints Wizard
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Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
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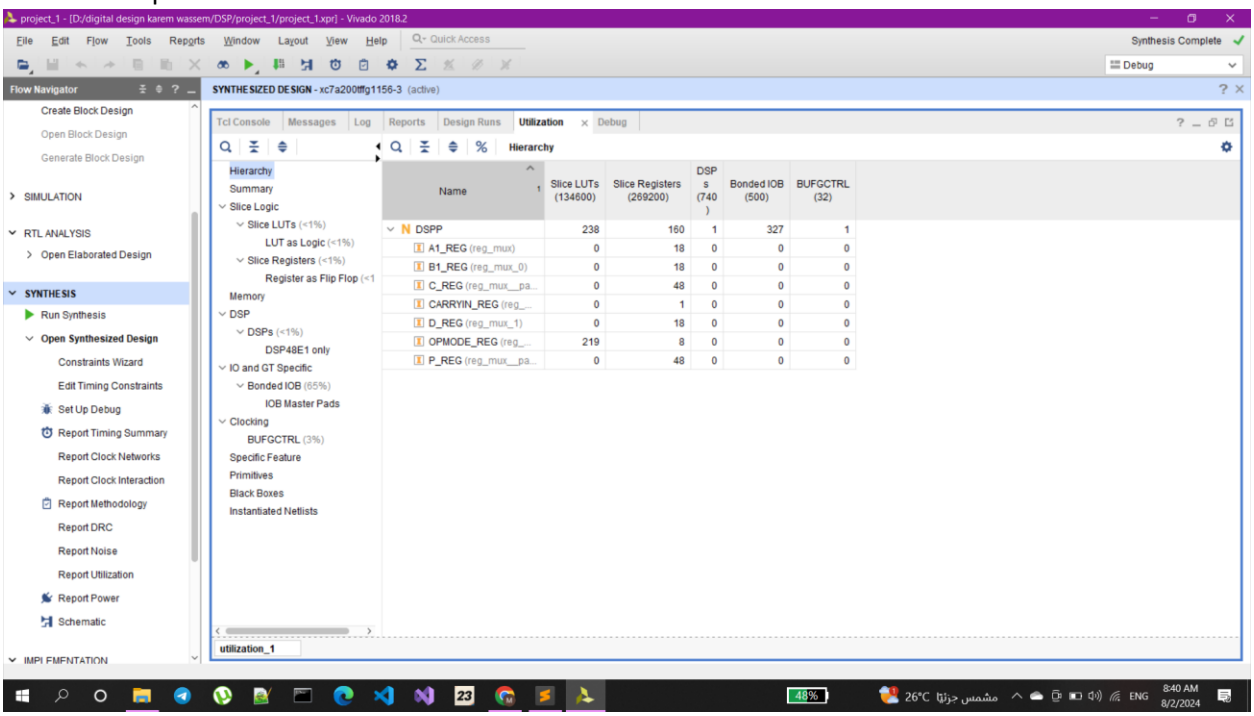
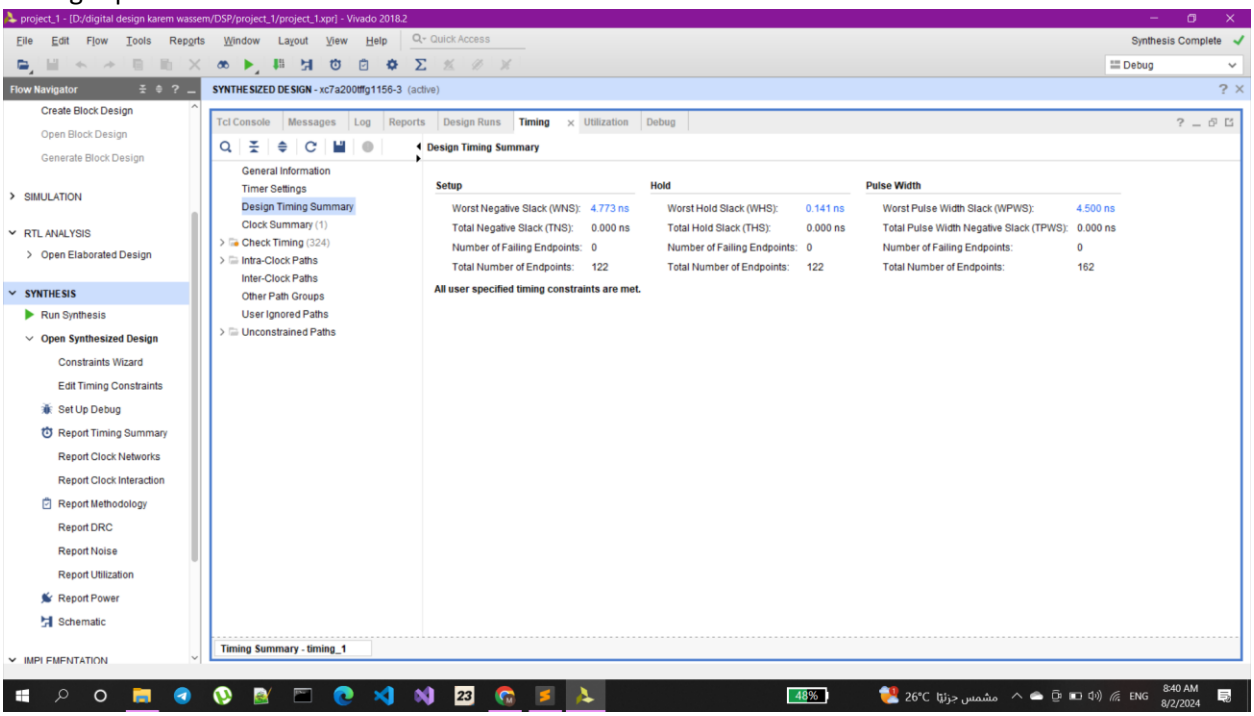
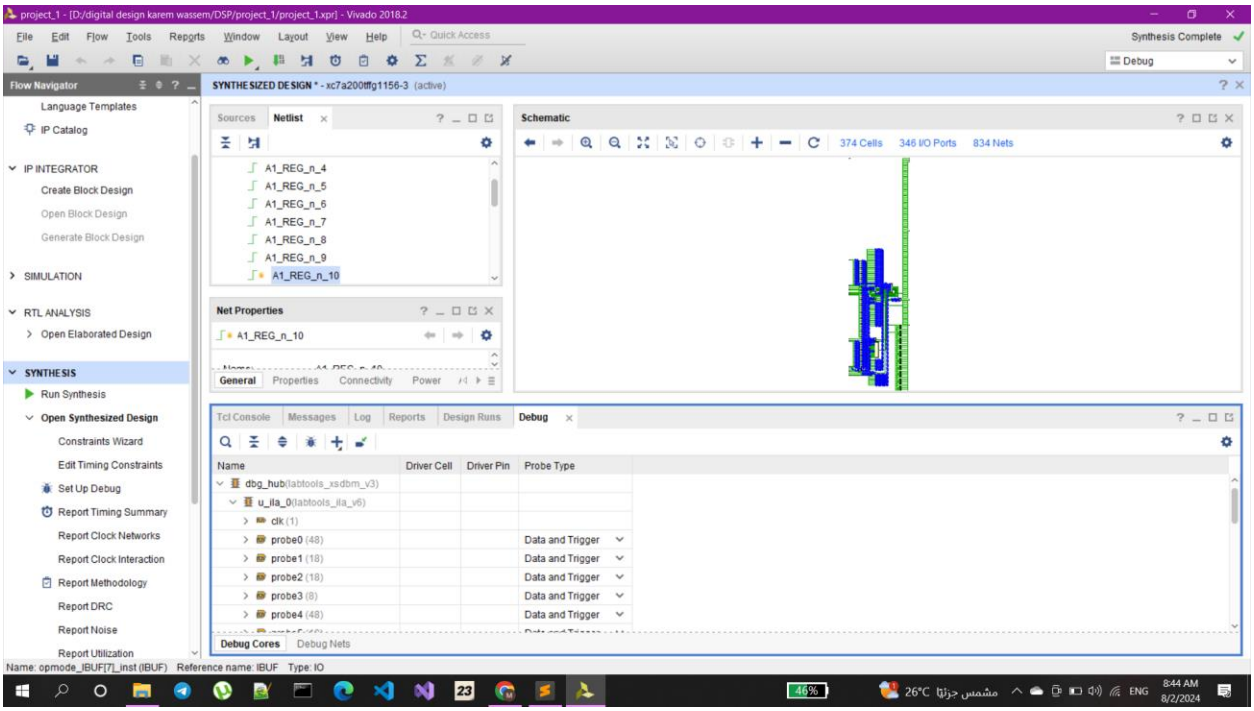
Report Utilization
Report Power
Schematic
IMPLEMENTATION
SYNTHESIZED DESIGN - xc7a200tffg1156-3 (active)
Sources
Netlist
DSPP
Nets (834)
Leaf Cells (370)
A1_REG (reg_mux)
B1_REG (reg_mux_0)
C_REG (reg_mux__parameterized0)
CARRYIN_REG (reg_mux__parameterized3)
D_REG (reg_mux_1)
Properties
Select an object to see properties
Schematic
374 Cells
346 I/O Ports
834 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Utilization
Debug
Hierarchy
Summary
Slice Logic
Slice LUTs (<1%)
LUT as Logic (<1%)
Slice Registers (<1%)
Register as Flip Flop
Name
Slice LUTs (134600)
Slice Registers (269200)
DSPs (740)
Bonded IOB (500)
BUFGCTRL (32)
DSPP 238 160 1 327 1
A1_REG (reg_mux) 0 18 0 0 0
B1_REG (reg_mux_0) 0 18 0 0 0
C_REG (reg_mux__pa... 0 48 0 0 0
utilization_1
48%
26°C
ENG
8:39 AM
8/2/2024

utilization report:



Timing report:




project_1 - [D:/digital design karem wassem/DSP/project_1/project_1.xpr] - Vivado 2018.2
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SYNTHESIZED DESIGN * - xc7a200tffg1156-3 (active)
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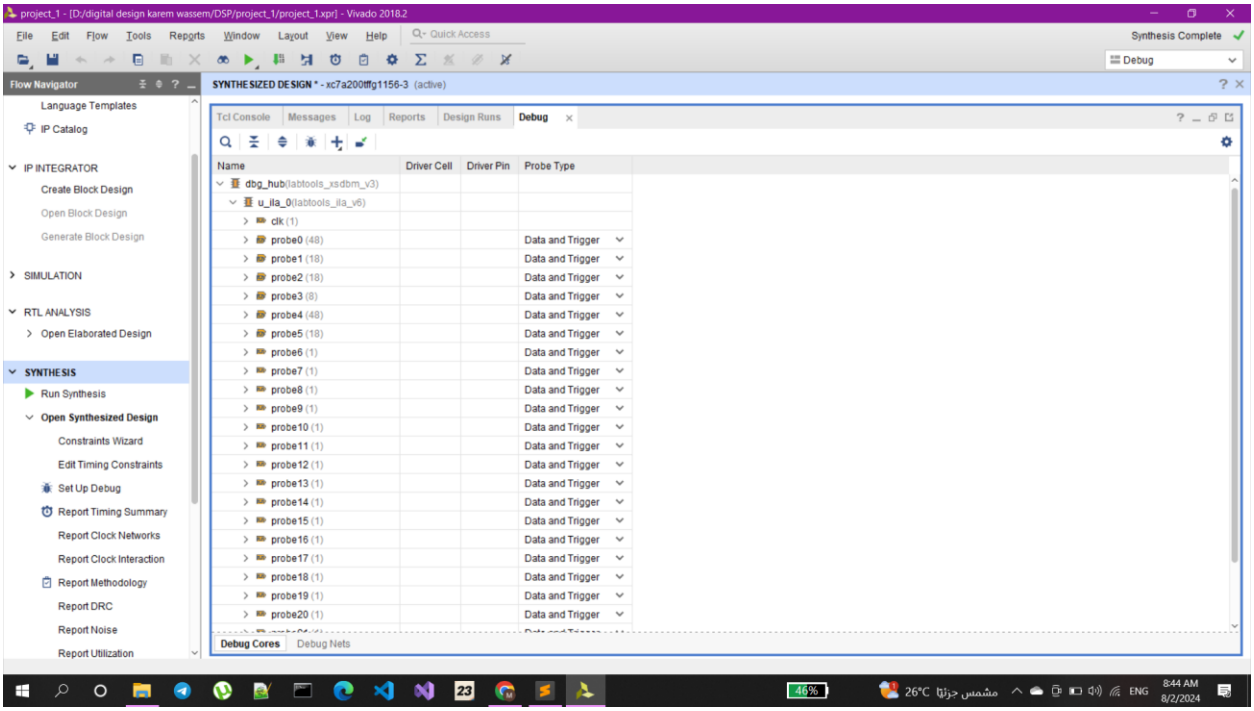
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Sources
Netlist
A1_REG_n_4
A1_REG_n_5
A1_REG_n_6
A1_REG_n_7
A1_REG_n_8
A1_REG_n_9
A1_REG_n_10
Net Properties
A1_REG_n_10
General
Properties
Connectivity
Power
Schematic
374 Cells
346 I/O Ports
834 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Debug
Name
Driver Cell
Driver Pin
Probe Type
dbg_hub (labtools_xsdbm_v3)
u_ila_0 (labtools_ila_v6)
clk (1)
probe0 (48)
probe1 (18)
probe2 (18)
probe3 (8)
probe4 (48)
Data and Trigger
Debug Cores
Debug Nets
Name: opmode_IBUF[7]_inst (IBUF)
Reference name: IBUF
Type: IO
46%
26°C
ENG
8:44 AM
8/2/2024


project_1 - [D:/digital design karem wassem/DSP/project_1/project_1.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
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Synthesis Complete
Debug
Flow Navigator
SYNTHESIZED DESIGN * - xc7a200tffg1156-3 (active)
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IP INTEGRATOR
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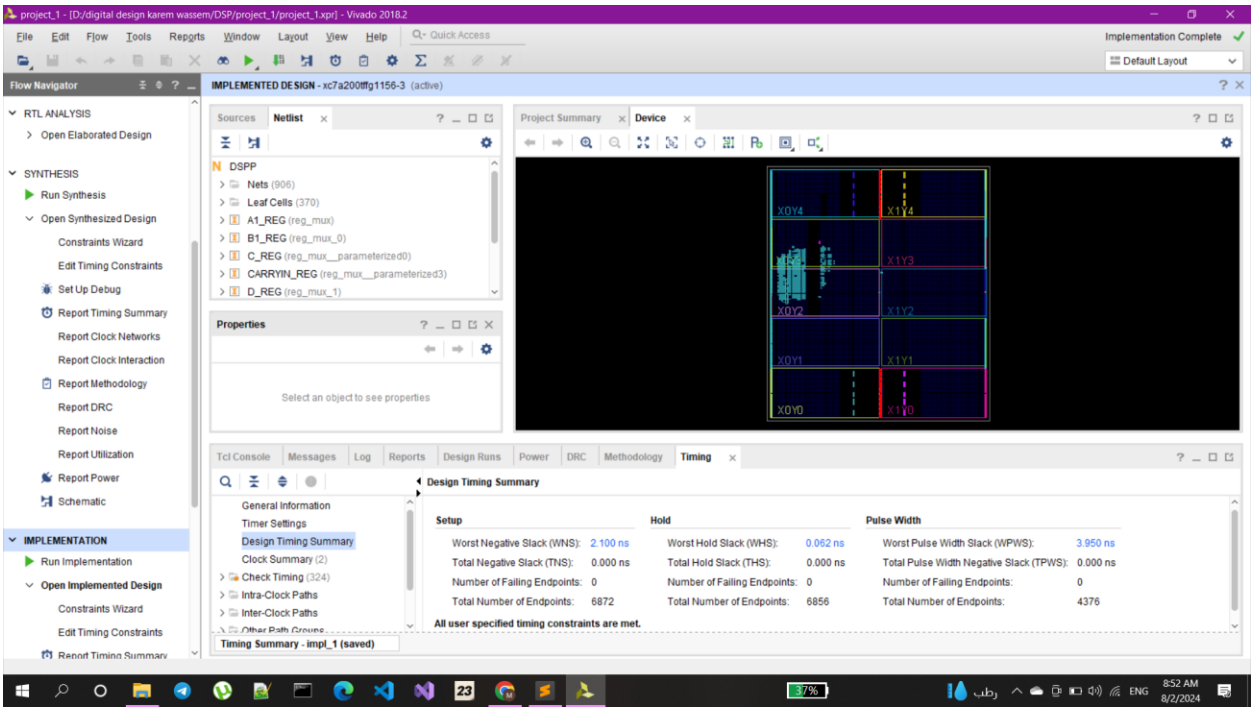
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Tcl Console
Messages
Log
Reports
Design Runs
Debug
Name
Driver Cell
Driver Pin
Probe Type
dbg_hub (labtools_xsdbm_v3)
u_ila_0 (labtools_ila_v6)
clk (1)
probe0 (48)
probe1 (18)
probe2 (18)
probe3 (8)
probe4 (48)
probe5 (18)
probe6 (1)
probe7 (1)
probe8 (1)
probe9 (1)
probe10 (1)
probe11 (1)
probe12 (1)
probe13 (1)
probe14 (1)
probe15 (1)
probe16 (1)
probe17 (1)
probe18 (1)
probe19 (1)
probe20 (1)
Data and Trigger
Debug Cores
Debug Nets
46%
26°C
ENG
8:44 AM
8/2/2024


project_1 - [D:/digital design karem wassem/DSP/project_1/project_1.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
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Implementation Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a200tffg1156-3 (active)
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Sources
Netlist
DSPP
Nets (906)
Leaf Cells (370)
A1_REG (reg_mux)
B1_REG (reg_mux_0)
C_REG (reg_mux__parameterized0)
CARRYIN_REG (reg_mux__parameterized3)
D_REG (reg_mux_1)
Properties
Select an object to see properties
Project Summary
Device
X0Y4
X1Y4
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
General Information
Timer Settings
Design Timing Summary
Clock Summary (2)
Check Timing (324)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
Timing Summary - impl_1 (saved)
Design Timing Summary
Setup
Worst Negative Slack (WNS): 2.100 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 6872
Hold
Worst Hold Slack (WHS): 0.062 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 6856
Pulse Width
Worst Pulse Width Slack (WPWS): 3.950 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 4376
All user specified timing constraints are met.
37%
ENG
8:52 AM
8/2/2024