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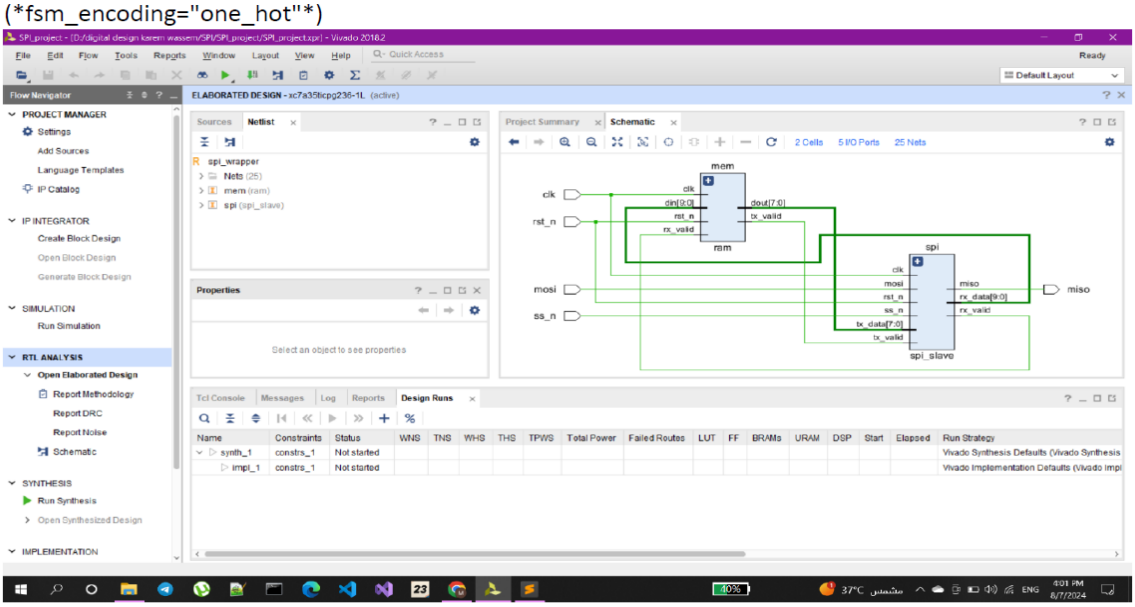
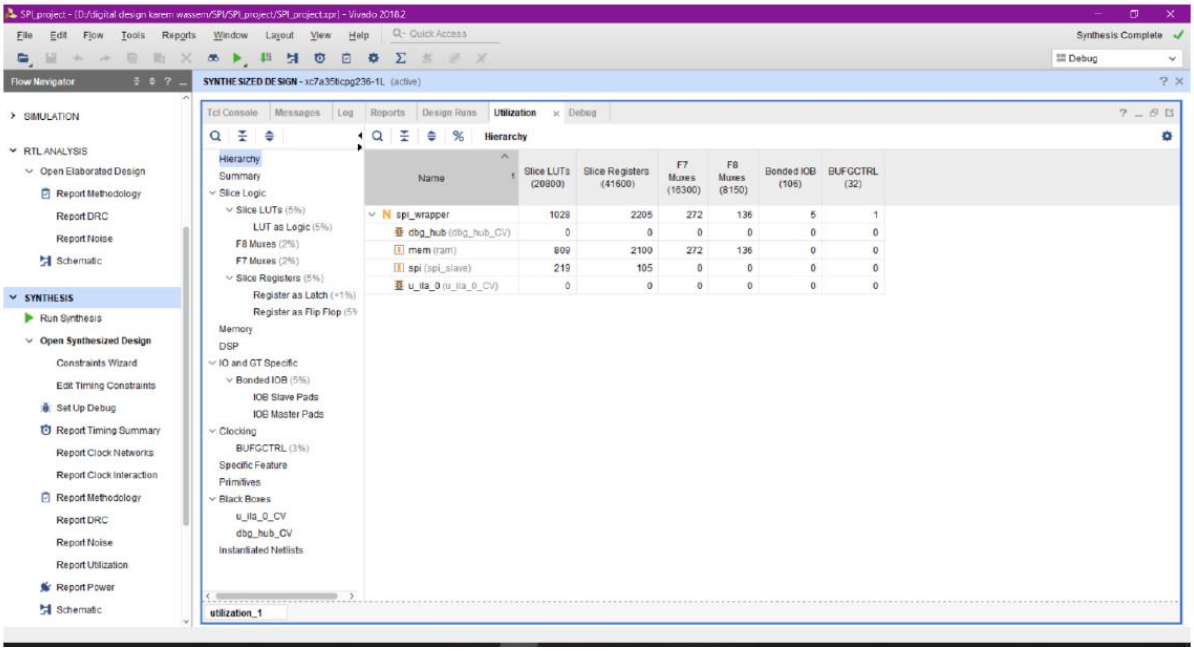
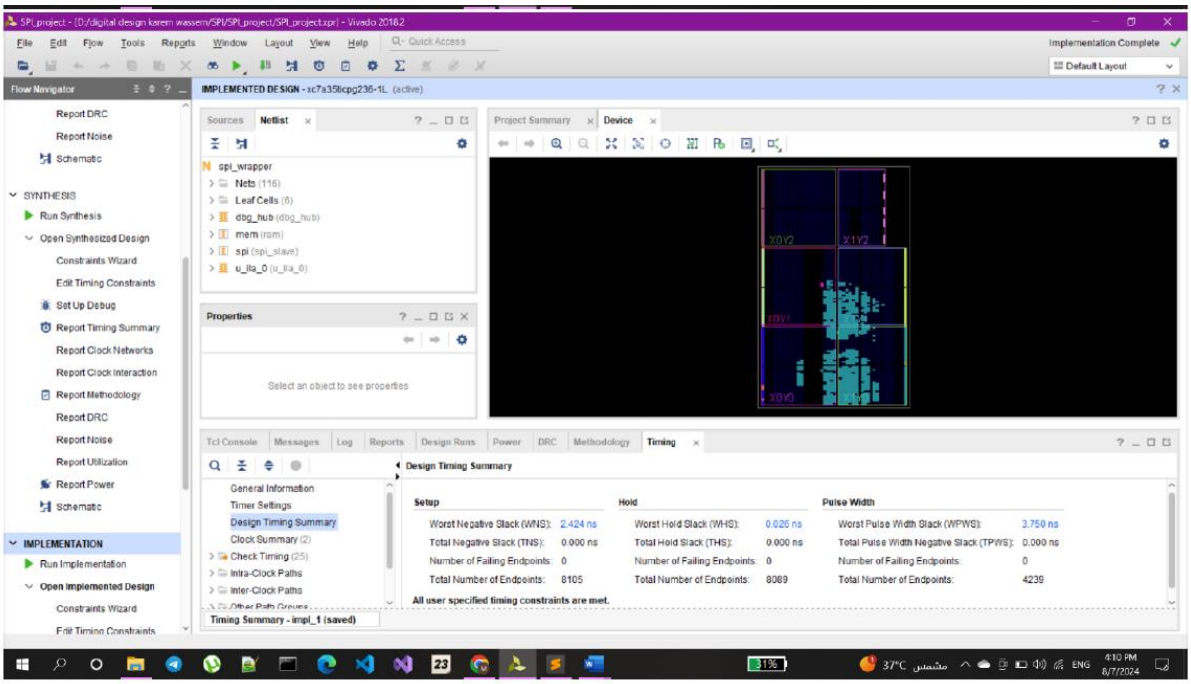


utilization report





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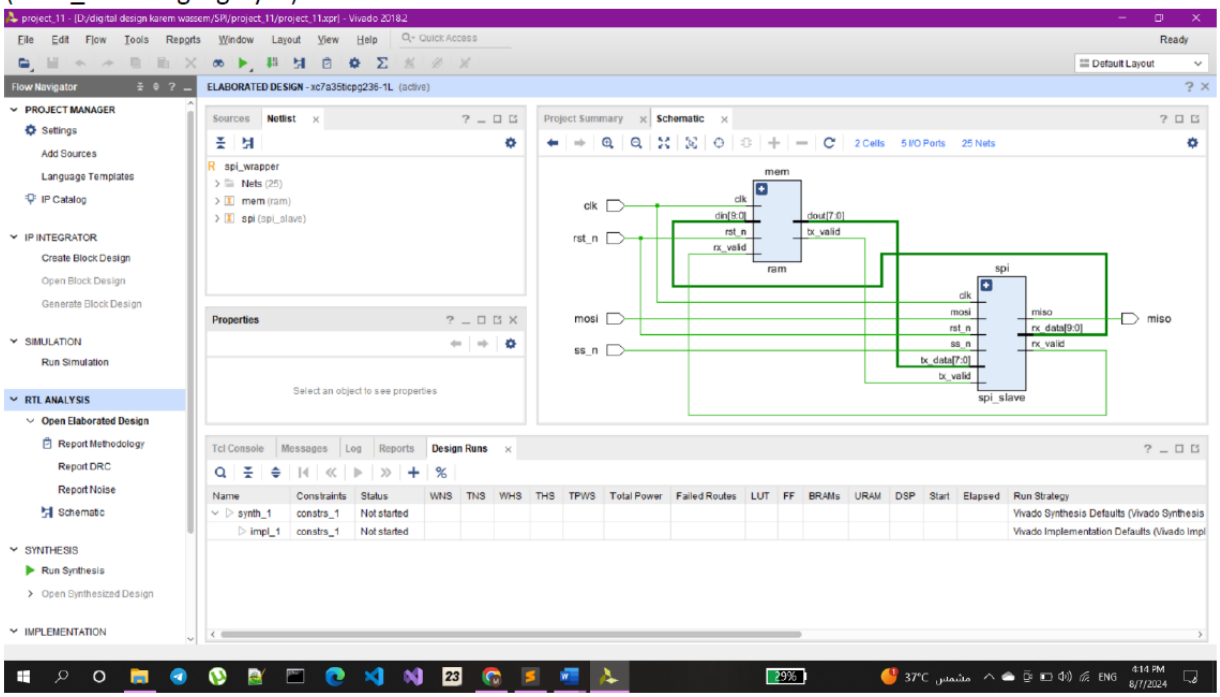
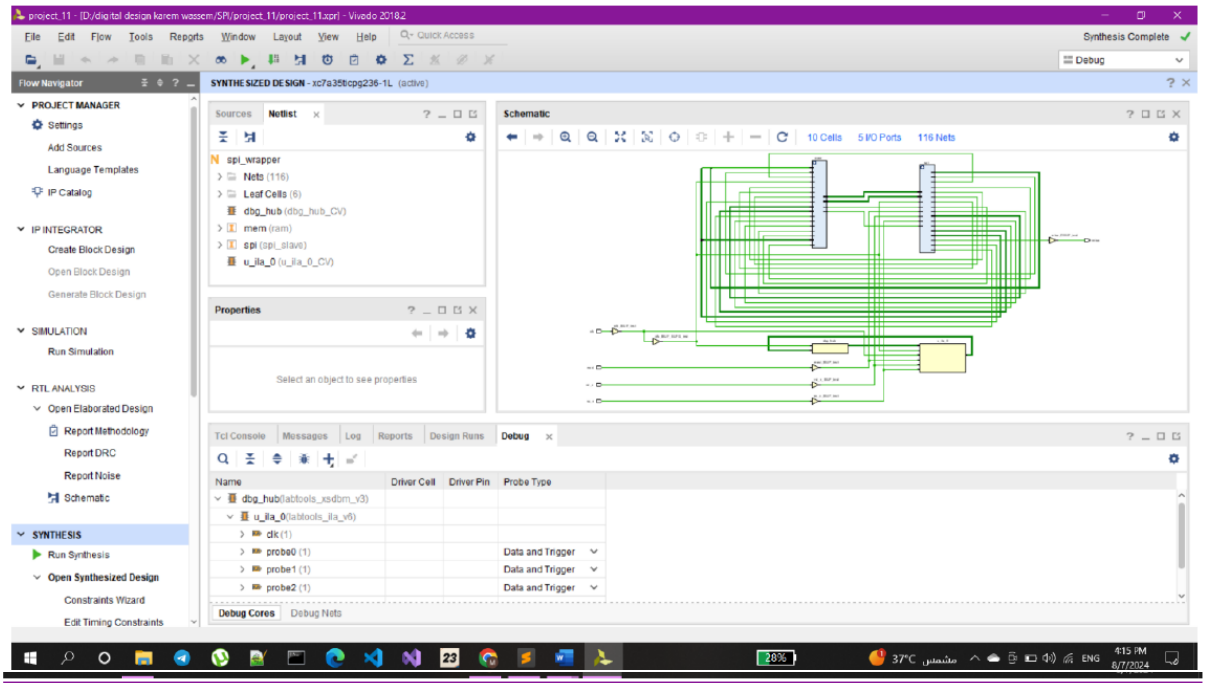
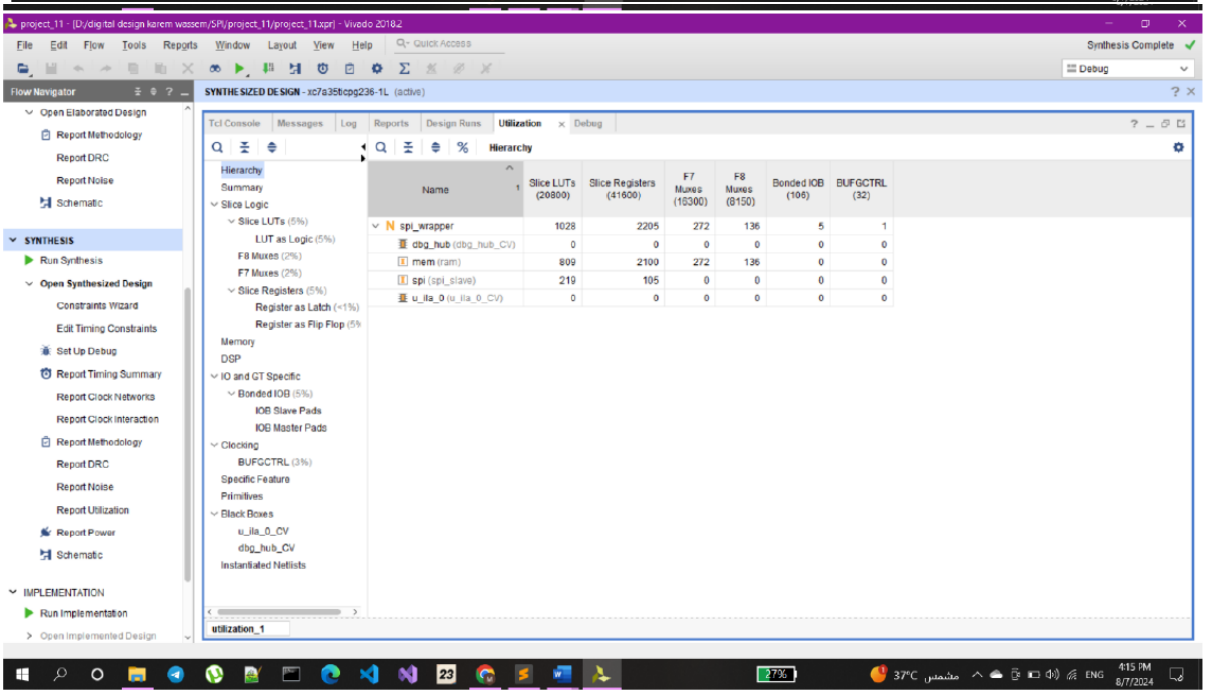
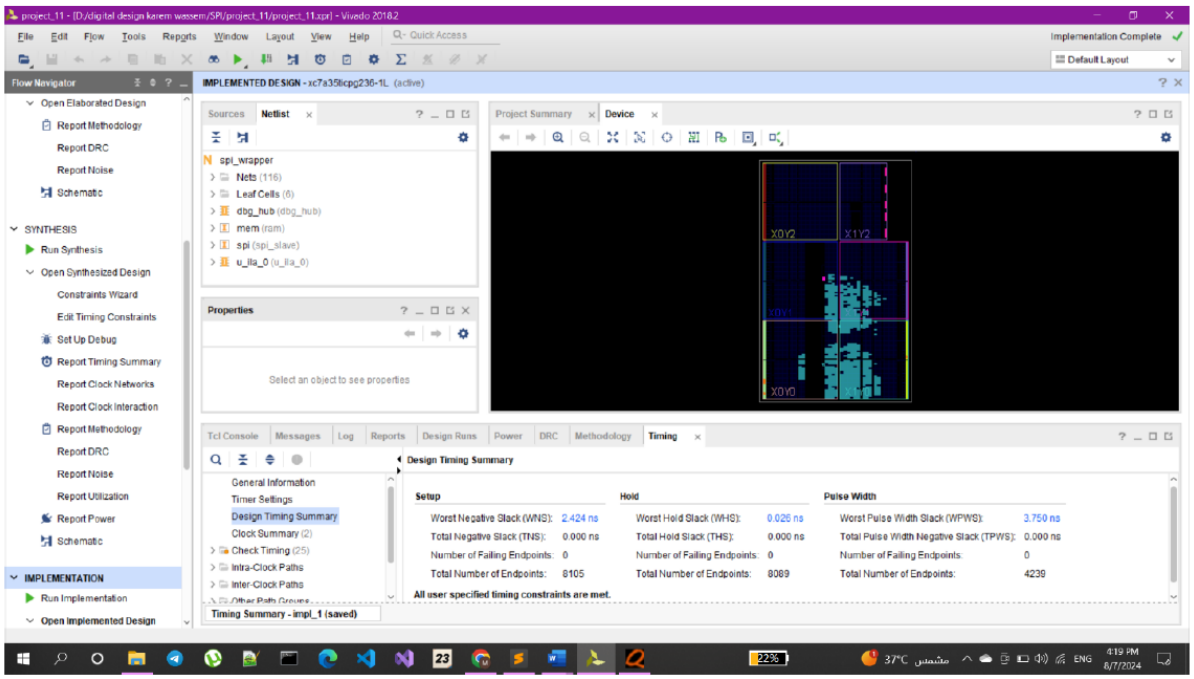



project_11 - [D:/digital design karem wassem/SPI/project_11/project_11.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Complete
Debug
Flow Navigator
SYNTHESIZED DESIGN - xc7a35tcpg236-1L (active)
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Sources
Netlist
spi_wrapper
Nets (116)
Leaf Cells (6)
dbg_hub (dbg_hub_CV)
mem (ram)
spi (spi_slave)
u_ila_0 (u_ila_0_CV)
Properties
Select an object to see properties
Schematic
10 Cells
5 I/O Ports
116 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Debug
Name
Driver Cell
Driver Pin
Probe Type
dbg_hub(labtools_xsdbm_v3)
u_ila_0(labtools_ila_v6)
clk (1)
probe0 (1)
probe1 (1)
probe2 (1)
Data and Trigger
Debug Cores
Debug Nets
28%
37°C
ENG
4:15 PM
8/7/2024


project_11 - [D:/digital design karem wassem/SPI/project_11/project_11.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Complete
Debug
Flow Navigator
SYNTHESIZED DESIGN - xc7a35tcpg236-1L (active)
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
IMPLEMENTATION
Run Implementation
Open Implemented Design
Tcl Console
Messages
Log
Reports
Design Runs
Utilization
Debug
Hierarchy
Hierarchy
Summary
Slice Logic
Slice LUTs (5%)
LUT as Logic (5%)
F8 Muxes (2%)
F7 Muxes (2%)
Slice Registers (5%)
Register as Latch (<1%)
Register as Flip Flop (5%)
Memory
DSP
IO and GT Specific
Bonded IOB (5%)
IOB Slave Pads
IOB Master Pads
Clocking
BUFGCTRL (3%)
Specific Feature
Primitives
Black Boxes
u_ila_0_CV
dbg_hub_CV
Instantiated Netlists
Name
Slice LUTs (20800)
Slice Registers (41600)
F7 Muxes (16300)
F8 Muxes (8150)
Bonded IOB (106)
BUFGCTRL (32)
spi_wrapper 1028 2205 272 136 5 1
dbg_hub (dbg_hub_CV) 0 0 0 0 0 0
mem (ram) 809 2100 272 136 0 0
spi (spi_slave) 219 105 0 0 0 0
u_ila_0 (u_ila_0_CV) 0 0 0 0 0 0
utilization_1
27%
37°C
ENG
4:15 PM
8/7/2024



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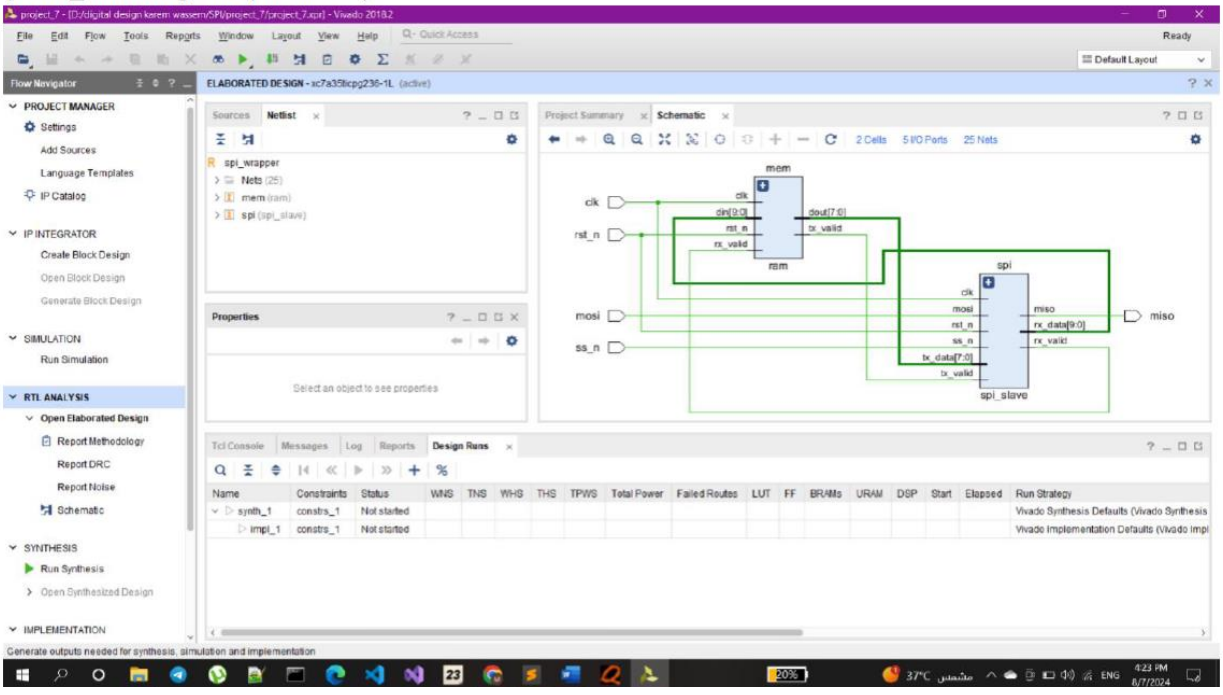

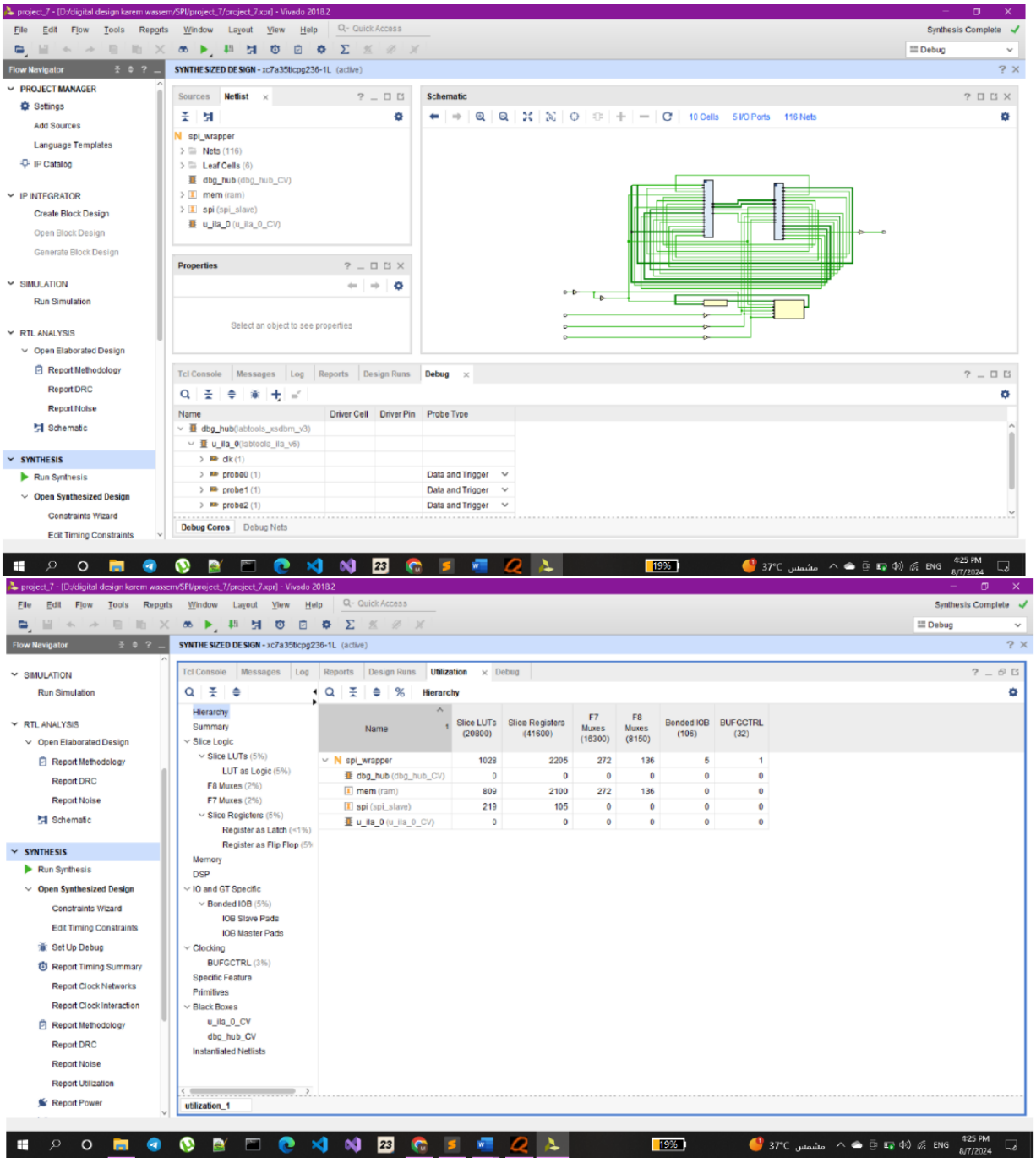
project_7 - [D:/digital design karem wassem/SPI/project_7/project_7.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Complete
Debug
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
SYNTHESIZED DESIGN - xc7a35ticpg236-1L (active)
Sources
Netlist
spi_wrapper
Nets (116)
Leaf Cells (6)
dbg_hub (dbg_hub_CV)
mem (ram)
spi (spi_slave)
u_ila_0 (u_ila_0_CV)
Properties
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Schematic
10 Cells
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Tcl Console
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Log
Reports
Design Runs
Debug
Name
Driver Cell
Driver Pin
Probe Type
dbg_hub (labtools_xsdbm_v3)
u_ila_0 (labtools_ila_v6)
clk (1)
probe0 (1)
probe1 (1)
probe2 (1)
Data and Trigger
Debug Cores
Debug Nets
19%
37°C
ENG
4:25 PM
8/7/2024

project_7 - [D:/digital design karem wassem/SPI/project_7/project_7.xpr] - Vivado 2018.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Complete
Debug
Flow Navigator
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
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Schematic
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spi (spi_slave) 219 105 0 0 0 0
u_ila_0 (u_ila_0_CV) 0 0 0 0 0 0
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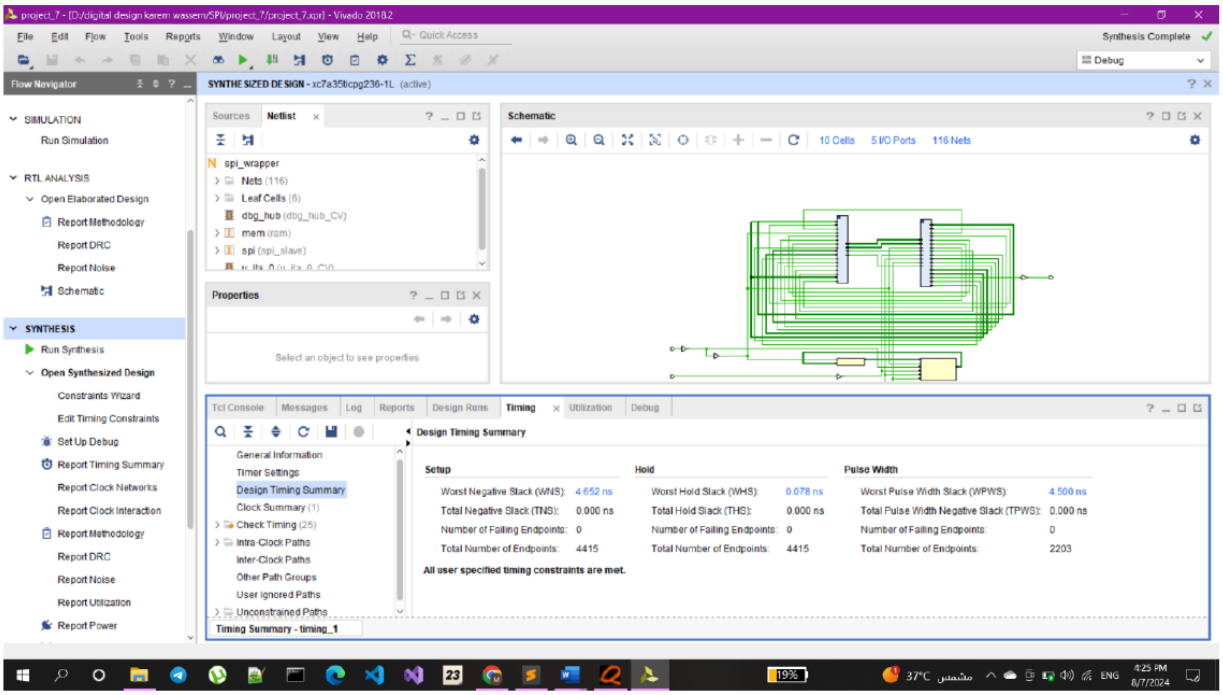
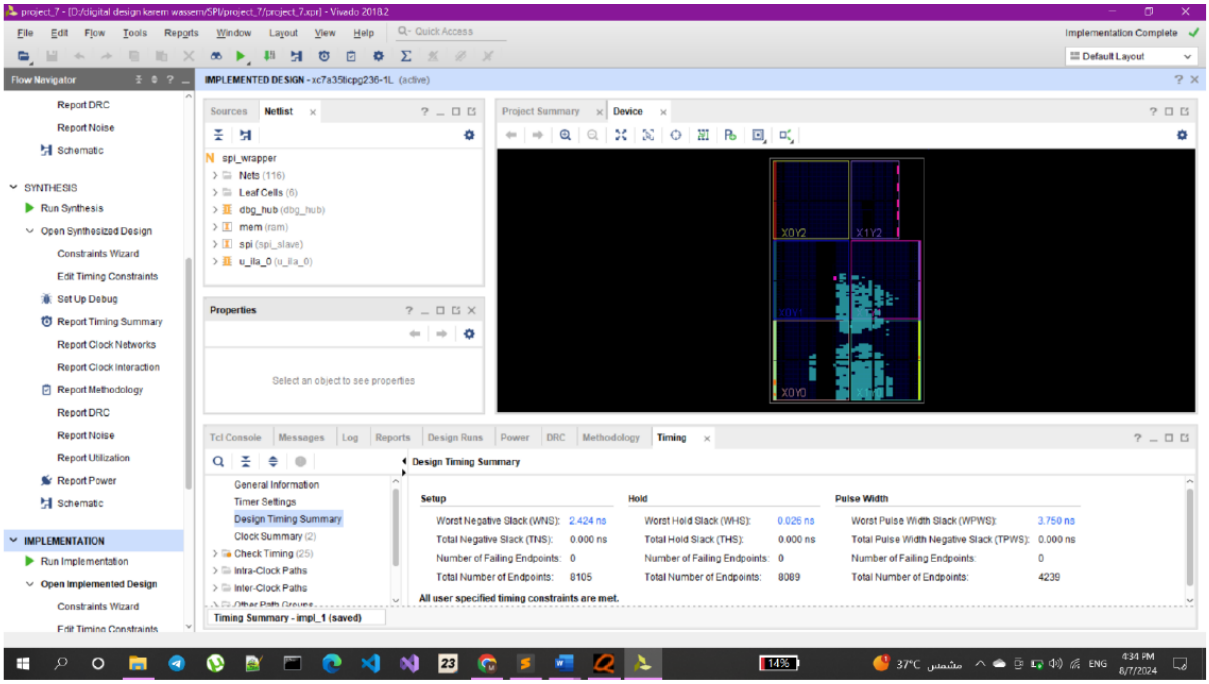
19%
37°C
ENG
4:25 PM
8/7/2024





Timing rebort