16.265 Logic Design Laboratory Grade Sheet

Do not staple this page to the report

1. (This section to be completed by student)

Student logic number: \_116\_\_

Student name: (Last) \_\_\_\_\_Downing\_\_\_\_\_, (first) \_\_\_\_\_\_\_Jason\_\_\_\_\_\_\_\_\_\_

Experiment number: 3

Date/time: \_\_3\_\_/\_27\_\_/ \_\_2015\_\_, \_\_\_\_\_\_\_\_\_\_a.m./p.m.

1. Preliminary checking
2. Is the report written on 8½” x 11” paper and stapled at left margin?
3. Is a cover page included?
4. Is the report written using the given template?
5. Is a CD/DVD included (with name and student logic number on CD/DVDl)?
6. Is the correct assignment used in design?

Report will not be accepted if the answer is “NO” to any of the above questions.

1. Grade

1. Design procedures: supporting theory, details, etc. (20) \_\_\_\_\_\_\_\_\_\_\_

23. Is design correct? (60) \_\_\_\_\_\_\_\_\_\_\_

3. Minimization of design (10) \_\_\_\_\_\_\_\_\_\_\_

5. List of ICs and unused gates (10) \_\_\_\_\_\_\_\_\_\_\_

Gross grade (100) \_\_\_\_\_\_\_\_\_\_

1. Adjustment to grade

1. Cover page, folder, disk (−5) \_\_\_\_\_\_\_\_\_\_\_

2. Title box of schematic diagram (−5) \_\_\_\_\_\_\_\_\_\_\_

3. Schematic diagram in correct format (−10) \_\_\_\_\_\_\_\_\_\_\_

4. Misrepresentation of test (simulation) results (−30) \_\_\_\_\_\_\_\_\_\_\_

1. 5. Neatness and legibility (−10) \_\_\_\_\_\_\_\_\_\_
2. 6. Templates (−20) \_\_\_\_\_\_\_\_\_\_

Final grade (100) \_\_\_\_\_\_\_\_\_\_

Comments: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Grader: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Date: \_\_\_\_/\_\_\_\_/\_\_\_\_\_\_\_\_

|  |  |
| --- | --- |
| 16.265 Logic Design Spring 2014 | |
| Student Logic Number | 116 |
| Name | Jason Downing |
| E-mail address (print) | Jason\_downing@student.uml.edu |
| Experiment Number | 3 |
| Date | 3/27/2015 |

|  |  |
| --- | --- |
| For grader use | |
| No CD/disk or  No schematic file on CD/disk | 5 points deduction |
| Schematic diagram on CD/disk is different from the one in the report. (Need to re-submit the schematic diagram in the report or will be graded based on a maximum of 50 points. | 5 points deduction |
| Cannot open file |  |
| File is not readable |  |
| Date student is notified to re-submit a schematic file by e-mail |  |
| Date schematic file received |  |

Report will be graded based on a maximum of 50 (out of 100 points) if a schematic diagram is not received within three calendar days of notification or the re-submitted schematic file still cannot be opened or is not readable.

Grade: \_\_\_\_\_\_\_\_\_\_\_

1. Function Set Assignment

Function set number \_\_9\_\_\_

F1(x,y,z) = 1 ⊕ x’y ⊕ z’

F2(x,y,z) = x ⊕ y ⊕ z’ ⊕ xy’z

F3(w,x,y,z) = y’(w + xz) + y(wxz + w’x’z’)

F4(w,x,y,z) = Σm(1, 2, 6, 7, 8, 14) + d(9, 10, 12, 13)

F5(w,x,y,z) = (w’ + y)(x’ + y + z’)(w + x + y’)(w + y’ + z)

2. Design Procedures

Express all the functions in minterm list form

F1(x,y,z) = Σm (1, 2, 5, 7)

F2(x,y,z) = Σm (0, 3, 6)

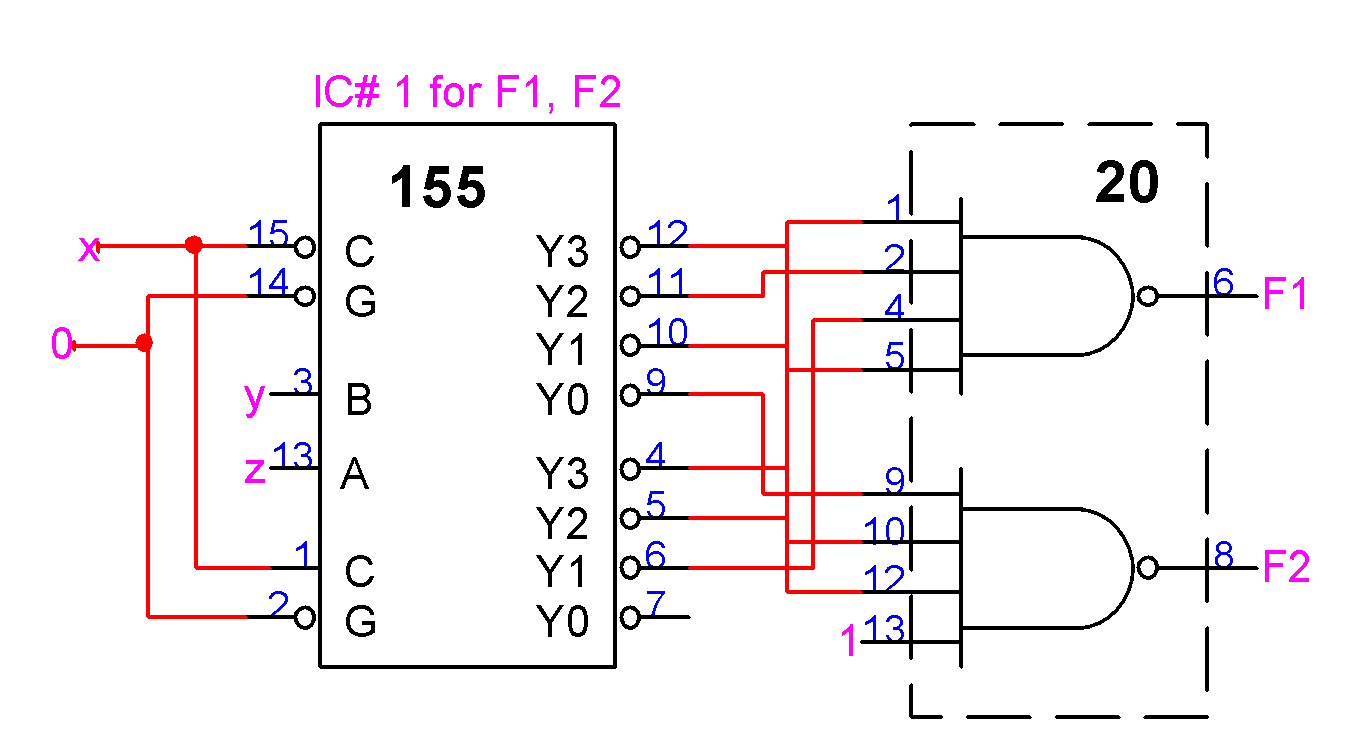
F3(w,x,y,z) = Σm (2, 5, 8, 9, 12, 13, 15)

F4(w,x,y,z) = Σm (1, 2, 6, 7, 8, 14) + d(9, 10, 12, 13)

F5(w,x,y,z) = Σm (0, 1, 4, 7, 10, 11, 14, 15)

Design for F1 and F2

(Show the implementation of F1 and F2 by a 74155 IC and some external gates. Draw a circuit diagram.)



Design for F3

Draw the sub-function K-maps for F3 with w, x, z as expansion variables.



Based on the sub-function K-maps, the data inputs to the 8-to-1 multiplexers are as follows:

I0 =

I1 =

I2 =

I3 =

I4 =

I5 =

I6 =

I7 =

Design for F4 and F5



K-map for F4 K-map for F5

(i) Partition the K-maps with w and x as control signals.





The data inputs are as follows:

For F4 For F5

I0 = I0 =

I1 = I1 =

I2 = I2 =

I3 = I3 =

1. Partition the K-maps with w and y as control signals.



The data inputs are as follows:

For F4 For F5

I0 = I0 =

I1 = I1 =

I2 = I2 =

I3 = I3 =

(iii) Partition the K-maps with w and z as control signals.



The data inputs are as follows:

For F4 For F5

I0 = I0 =

I1 = I1 =

I2 = I2 =

I3 = I3 =

(iv) Partition the K-maps with x and y as control signals.



The data inputs are as follows:

For F4 For F5

I0 = I0 =

I1 = I1 =

I2 = I2 =

I3 = I3 =

(v) Partition the K-maps with x and z as control signals.



The data inputs are as follows:

For F4 For F5

I0 = I0 =

I1 = I1 =

I2 = I2 =

I3 = I3 =

(vi) Partition the K-maps with y and z as control signals.



The data inputs are as follows:

For F4 For F5

I0 = I0 =

I1 = I1 =

I2 = I2 =

I3 = I3 =

By comparing the six different combinations for control signals, the best selection is \_\_\_\_\_\_\_\_.

3. List of ICs and unused gates

|  |  |  |  |
| --- | --- | --- | --- |
| IC number | Type number | Function | Unused gates |
| 1 | 74155 | Dual 2-to-4 decoders | None |
| 2 | 74153 | Dual 4-to-1 multiplexers | None |
| 3 | 74153 | Dual 4-to-1 multiplexers | None |
| 4 | 7400 | Quad 2-input NAND | 0 |
| 5 | 7400 | Quad 2-input NAND | 0 |
| 6 | 7402 | Quad 2-input NOR | 0 |
| 7 | 7420 | Dual 4-input NAND | 0 |
| 8 | 7486 | Quad 2-input XOR | 0 |

### 4. Simulation results

### Table for simulation results

(Place a check mark in the column “Incorrect results” for each simulation value that is different from the value listed in the truth table in Section 2. All don’t-care terms should have values of either 0 or 1.)

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Inputs | Simulation results | | | | | Incorrect results | | | | |
| w x y z | F1 | F2 | F3 | F4 | F5 | F1 | F2 | F3 | F4 | F5 |
| 0 0 0 0 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |  |
| 0 0 0 1 | 1 | 0 | 0 | 1 | 1 |  |  |  |  |  |
| 0 0 1 0 | 1 | 0 | 1 | 1 | 0 |  |  |  |  |  |
| 0 0 1 1 | 0 | 1 | 0 | 0 | 0 |  |  |  |  |  |
| 0 1 0 0 | 0 | 0 | 0 | 0 | 1 |  |  |  |  |  |
| 0 1 0 1 | 1 | 0 | 1 | 0 | 0 |  |  |  |  |  |
| 0 1 1 0 | 0 | 1 | 0 | 1 | 0 |  |  |  |  |  |
| 0 1 1 1 | 1 | 0 | 0 | 1 | 1 |  |  |  |  |  |
| 1 0 0 0 | 0 | 1 | 1 | 1 | 0 |  |  |  |  |  |
| 1 0 0 1 | 1 | 0 | 1 | 1 | 0 |  |  |  |  |  |
| 1 0 1 0 | 1 | 0 | 0 | 1 | 1 |  |  |  |  |  |
| 1 0 1 1 | 0 | 1 | 0 | 0 | 1 |  |  |  |  |  |
| 1 1 0 0 | 0 | 0 | 1 | 1 | 0 |  |  |  |  |  |
| 1 1 0 1 | 1 | 0 | 1 | 0 | 0 |  |  |  |  |  |
| 1 1 1 0 | 0 | 1 | 0 | 1 | 1 |  |  |  |  |  |
| 1 1 1 1 | 1 | 0 | 1 | 0 | 1 |  |  |  |  |  |

5. Schematic diagram

### Schematic diagram for the 4-input 5-output circuit

Attach a complete schematic diagram including the title box.