EXPERIMENT NO:9

TITLE: Realization of RS, JK and D flip flop using universal logic gates.

OBJECTIVE: To implement RS, JK and D flip flop using NAND gates.

EQUIPMENTS:

Sl No.	Name	Manufacturer	Model No.

THEORY:

Flip Flops are memory elements capable of storing one bit of information. A flip flop circ
indefinitely until directed by an input signal to switch states. A flip flop has two states. A
state when Q=1 and reset when Q=1.There are different types of flip flops like RS,JK, D

Preset (Pr) and Clear (Cr) inputs are called asynchronous inputs.

When Pr=1 and Cr=1 circuit will operate as normal flip flops.
When Pr=1 and Cr=0 the flop flop will reset.
When Pr=0 and Cr=1 the flip flop will set.

The condition Pr=Cr=0 must not be used since, this leads to uncertain state.

- RS FLIP FLOP: Clocked RS flip flop consists of four NAND gates. When the clo
remains unchanged. When the clock input is high, output changes according to va

- JK FLIP FLOP: JK flip flop is a refinement of an RS flip flop. The undefined stat
in a JK flip flop.

- D FLIP FLOP:D flip flop receives its designation from its ability to transfer data
SR flip flop with an inverter at the R input.

CIRCUIT DIAGRAM

7410 3-input NAND gate