Gate Question

SECTION A

February 2, 2024

1. In the circuit shown below, assume that the comparators are ideal and all components have zero propagation delay. In one period of the input signal $Vin = 6\sin(\omega t)$, the fraction of the time for which the output OUT is in logic HIGH is (GATE-IN2019,34)

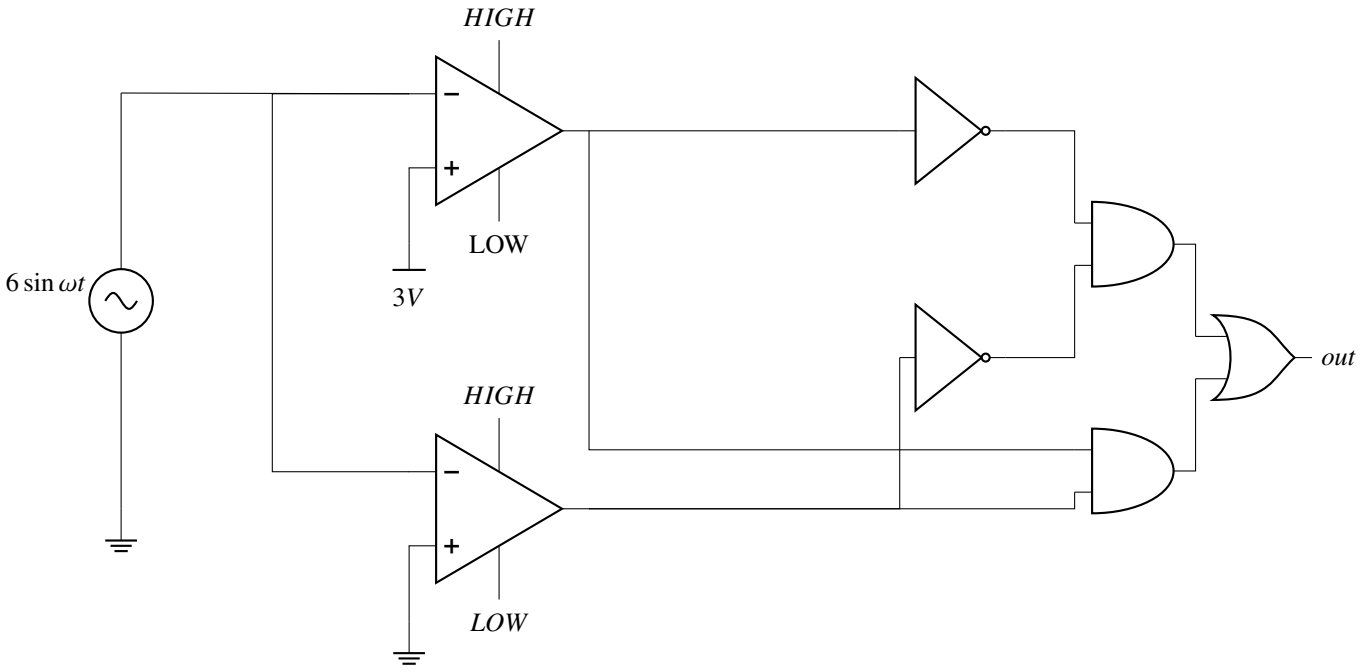

Figure 1: Circuit Daigram

1. $\frac{1}{12}$
2. $\frac{1}{2}$
3. $\frac{2}{3}$
4. $\frac{5}{6}$