



Project 1: phase one

Name: Mohand Mahmoud Farag

ID: 16p6042

Email: Mohand.zawrah98@yahoo.com

Group: 1

Section: 2

Department :CESS

The Finite state machine:

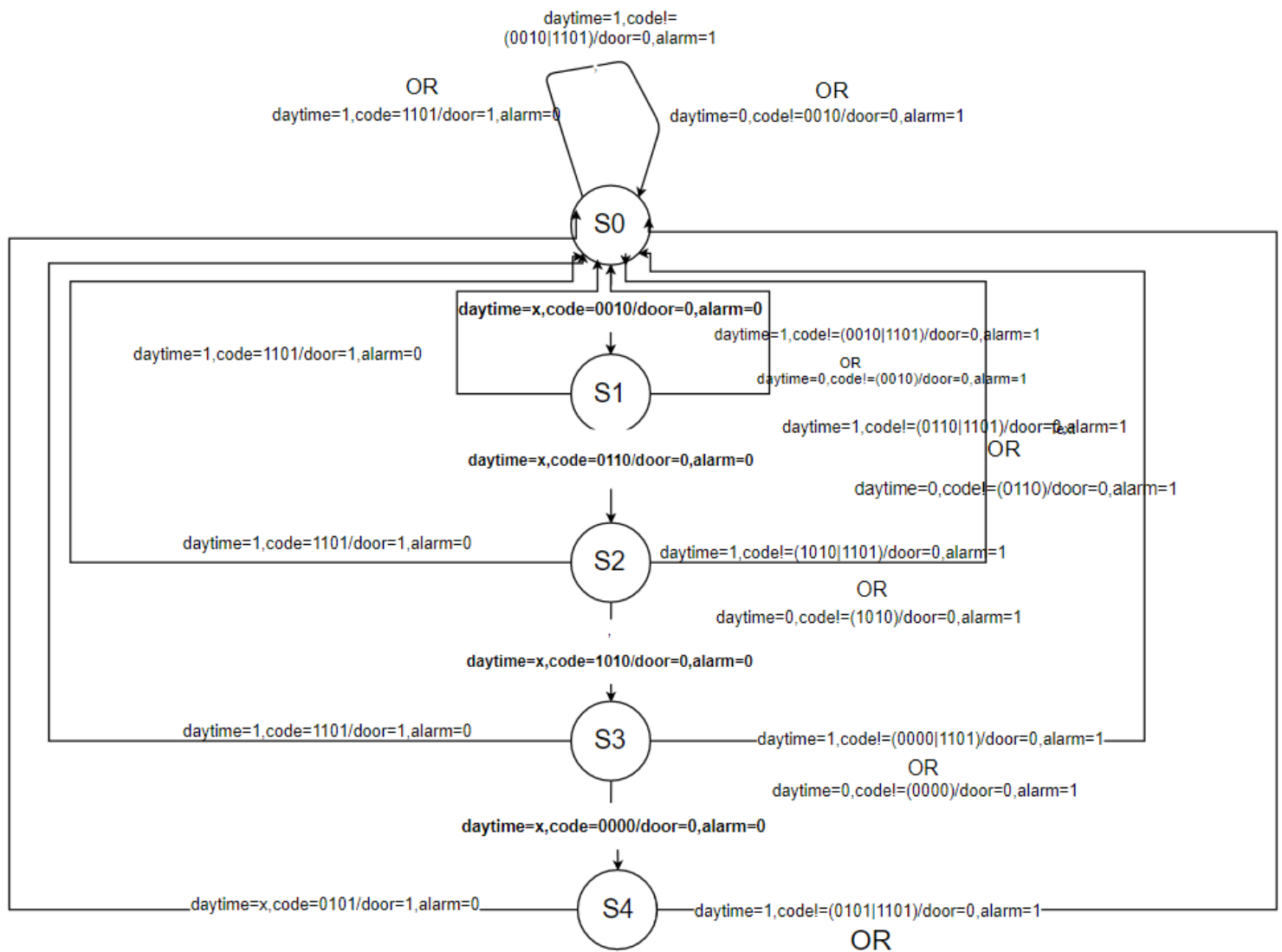


Table:

Current state	Daytime	Code	reset	New State	Door	Alarm
X	X	X	1	S0	0	0
S0	1	1101	0	S0	1	0
S0	X	0010	0	S1	0	0
S0	1	!(0010 1101)	0	S0	0	1
S0	0	!(0010)	0	S0	0	1
S1	1	1101	0	S0	1	0
S1	X	0110	0	S2	0	0
S1	1	!(0110 1101)	0	S0	0	1
S1	0	!(0110)	0	S0	0	1
S2	1	1101	0	S0	1	0
S2	X	1010	0	S3	0	0
S2	1	!(1010 1101)	0	S0	0	1
S2	0	!(1010)	0	S0	0	1
S3	1	1101	0	S0	1	0
S3	X	0000	0	S4	0	0
S3	1	!(0000 1101)	0	S0	0	1
S3	0	!(0000)	0	S0	0	1
S4	1	1101	0	S0	1	0
S4	X	0101	0	S0	1	0
S4	1	!(0101 1101)	0	S0	0	1
S4	0	!(0101)	0	S0	0	1

The Code:

```
library Sxlib_ModelSim;

library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;

use ieee.NUMERIC_STD.all;

entity project1 is
port (
    clk    : in    bit;
        code : in    bit_vector(3 downto 0) ;
        daytime : in bit;
        reset : in    bit;
        vdd   : in    bit;
        vss   : in    bit;
        door   : out   bit;
        alarm  : out   bit
    );
end project1;

architecture FSM of project1 is
    type STATE_TYPE is (S0, S1,s2,s3,s4);
    signal NS, CS : STATE_TYPE;
begin
    p1: process (CS, code, daytime, reset)
    begin
        if (reset='1') then
            NS<=S0;
            door<='0';
```

```

    alarm<='0';
else
case CS is
    when s0=>
        if(daytime='1') then
            if(code="1101") then
                door <= '1';
                alarm <= '0';
                NS <=s0;
            elsif(code="0010") then
                door<='0';
                alarm<='0';
                NS<=s1;
            else
                door<='0';
                alarm<='1';
                NS <= S0;
            end if;
        elsif (daytime='0')then
            if(code="0010") then
                door<='0';
                alarm<='0';
                NS<=s1;
            else
                door<='0';
                alarm<='1';
                NS <= S0;
            end if;
        end if;
    end case;
end if;

```

```
        end if;  
    end if;
```

```
when s1=>
```

```
    if(daytime='1') then  
        if(code="1101") then  
            door <= '1';  
            alarm <= '0';  
            NS <=s0;  
        elsif(code="0110") then  
            door<='0';  
            alarm<='0';  
            NS<=s2;  
        else  
            door<='0';  
            alarm<='1';  
            NS <= S0;  
        end if;  
    elsif (daytime='0') then  
        if(code="0110") then  
            door<='0';  
            alarm<='0';  
            NS<=s2;  
        else
```

door<='0';

alarm<='1';

NS <= S0;

end if;

end if;

when s2=>

if(daytime='1') then

if(code="1101") then

door <= '1';

alarm <= '0';

NS <=s0;

elsif(code="1010") then

door<='0';

alarm<='0';

NS<=s3;

else

door<='0';

alarm<='1';

NS <= S0;

end if;

elsif (daytime='0') then

if(code="1010") then

door<='0';

alarm<='0';

NS<=s3;

else

door<='0';

alarm<='1';

NS <= S0;

end if;

end if;

when s3=>

if(daytime='1') then

if(code="1101") then

door <= '1';

alarm <= '0';

NS <=s0;

elsif(code="0000") then

door<='0';

alarm<='0';

NS<=s4;

else

door<='0';

alarm<='1';

NS <= S0;

end if;

elsif (daytime='0')then

if(code="0000") then

door<='0';

alarm<='0';


```
        NS<=s4;
    else
        door<='0';
        alarm<='1';
        NS <= S0;
```

```
    end if;
end if;
```

```
when s4=>
```

```
    if(daytime='1') then
        if(code="1101") then
            door <= '1';
            alarm <= '0';
            NS <=s0;
        elsif(code="0101") then
            door<='1';
            alarm<='0';
            NS<=s0;
        else
            door<='0';
            alarm<='1';
            NS <= S0;
        end if;
    elsif (daytime='0') then
        if(code="0101") then
```

```

        door<='1';
        alarm<='0';
        NS<=s0;
    else
        door<='0';
        alarm<='1';
        NS <= S0;

    end if;
end if;
-----

end case;
end if;
end process;
p2: process(clk)
begin
    if(clk = '1' and clk'event)then

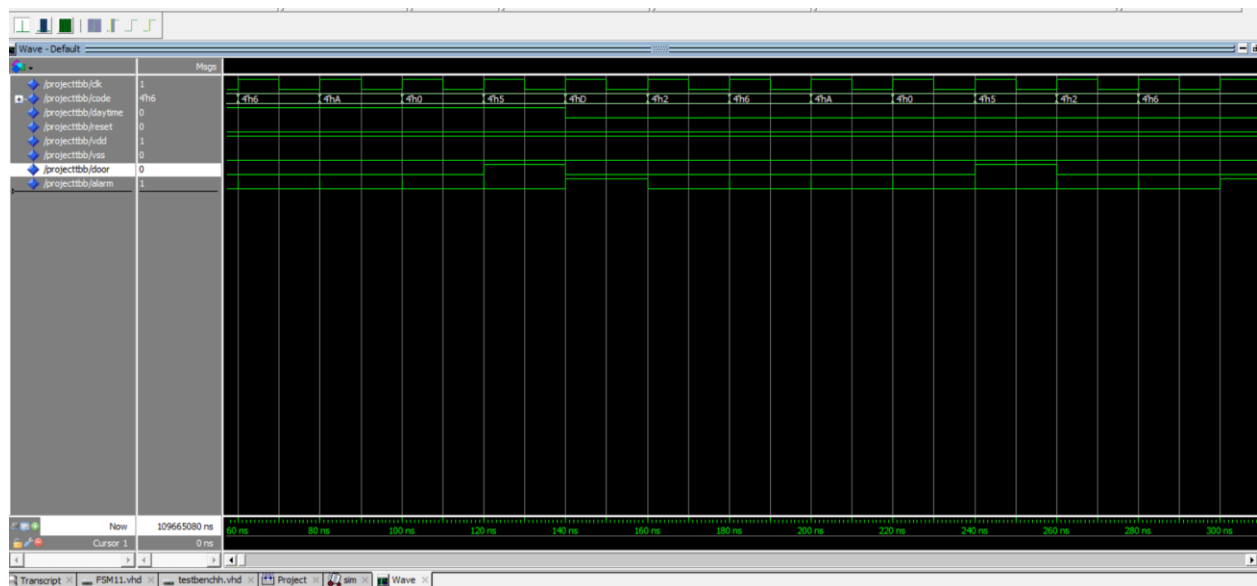
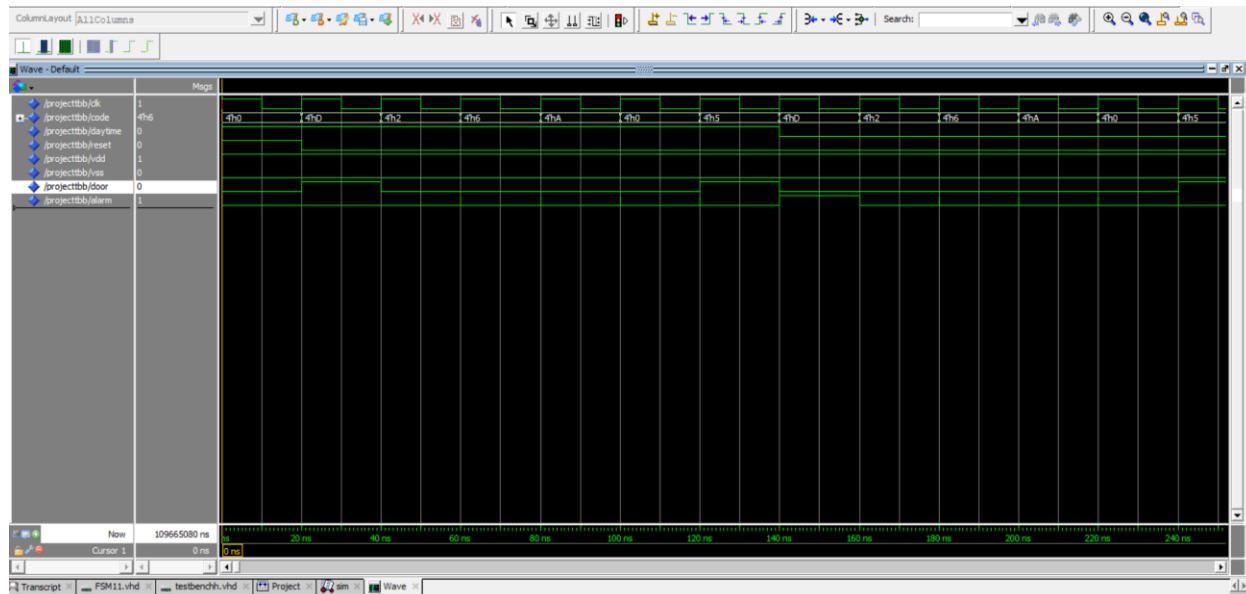
        CS <= NS;
    end if;
end process;
end FSM;

```

The test bench:

Test number	Daytime	Code	Reset	Expected Door	Expected Alarm	Door	Alarm
Reset test	X	X	1	0	0	0	0
O with dt=1 (test case 1)	1	1101	0	1	0	1	0
Full input with dt=1 (test case 2)	1	0010	0	0	0	0	0
	1	0110	0	0	0	0	0
	1	1010	0	0	0	0	0
	1	0000	0	0	0	0	0
	1	0101	0	1	0	1	0
O with dt=0 (test case 3)	0	1101	0	0	1	0	1
Full input with dt=0 (test case 4)	0	0010	0	0	0	0	0
	0	0110	0	0	0	0	0
	0	1010	0	0	0	0	0
	0	0000	0	0	0	0	0
	0	0101	0	1	0	1	0
Incorrect input (test case 5)	0	0010	0	0	1	0	1
	0	0110	0	0	1	0	1
	0	0110	0	0	1	0	1

The output:



The code:

```
library Sxlib_ModelSim;

library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;

use ieee.NUMERIC_STD.all;

ENTITY projecttbb IS

END ENTITY projecttbb;

ARCHITECTURE fsmtbb OF projecttbb IS

component project1 is

port (

    clk    : in    bit;

        code : in    bit_vector(3 downto 0) ;

        daytime : in bit;

        reset : in    bit;

        vdd   : in    bit;

        vss   : in    bit;

        door  : out   bit;

        alarm : out   bit

    );

end component;

FOR dut: project1 USE ENTITY WORK.project1 (FSM);

SIGNAL clk    : bit := '0';

SIGNAL code    : bit_vector(3 downto 0) := "0000";

SIGNAL daytime : bit := '1';

SIGNAL reset : bit := '1';

SIGNAL vdd : bit := '1';
```

```

SIGNAL vss : bit := '0';

signal door : bit:= '0';

signal alarm : bit := '0';

begin

dut: project1 PORT MAP (clk, code, daytime, reset, door, alarm, vdd, vss);

clk_process :process

begin

    clk <= '1';

    wait for 10 ns;

    clk <= '0';

    wait for 10 ns;


    end process;

p1:process is begin

wait For 20 ns;

ASSERT door = '0' and alarm ='0'

REPORT "1 error"

SEVERITY error;

---- first testbensh

daytime<='1';

code<="1101";

reset<='0';

wait For 20 ns;

ASSERT door = '1' and alarm ='0'

REPORT "2 error"

SEVERITY error;

-----second testbench

```

```
daytime<='1';  
code<="0010";  
reset<='0';  
wait For 20 ns;  
ASSERT door = '0' and alarm = '0'  
REPORT " 3 error"  
SEVERITY error;
```

```
daytime<='1';  
code<="0110";  
reset<='0';  
wait For 20 ns;  
ASSERT door = '0' and alarm = '0'  
REPORT " 4 error"  
SEVERITY error;
```

```
daytime<='1';  
code<="1010";  
reset<='0';  
wait For 20 ns;  
ASSERT door = '0' and alarm = '0'  
REPORT " 5 error"  
SEVERITY error;
```

```
daytime<='1';  
code<="0000";  
reset<='0';
```

```

wait For 20 ns;
ASSERT door = '0' and alarm ='0'
REPORT " 6 error"
SEVERITY error;
-----

daytime<='1';
code<="0101";
reset<='0';
wait For 20 ns;
ASSERT door = '1' and alarm ='0'
REPORT " 7 error"
SEVERITY error;
-----third testbench

daytime<='0';
code<="1101";
reset<='0';
wait For 20 ns;
ASSERT door = '0' and alarm ='1'
REPORT "8 error"
SEVERITY error;
-----fourth testnech

daytime<='0';
code<="0010";
reset<='0';
wait For 20 ns;
ASSERT door = '0' and alarm ='0'
REPORT "9 error"

```


SEVERITY error;

daytime<='0';

code<="0110";

reset<='0';

wait For 20 ns;

ASSERT door = '0' and alarm = '0'

REPORT "10 error"

SEVERITY error;

daytime<='0';

code<="1010";

reset<='0';

wait For 20 ns;

ASSERT door = '0' and alarm = '0'

REPORT "11 error"

SEVERITY error;

daytime<='0';

code<="0000";

reset<='0';

wait For 20 ns;

ASSERT door = '0' and alarm = '0'

REPORT "12 error"

SEVERITY error;

daytime<='0';

```
code<="0101";
reset<='0';
wait For 20 ns;
ASSERT door = '1' and alarm ='0'
REPORT "13 error"
SEVERITY error;
-----fifth testbench

daytime<='0';
code<="0010";
reset<='0';
wait For 20 ns;
ASSERT door = '0' and alarm ='0'
REPORT "14 error"
SEVERITY error;
-----

daytime<='0';
code<="0110";
reset<='0';
wait For 20 ns;
ASSERT door = '0' and alarm ='0'
REPORT "15 error"
SEVERITY error;
-----

daytime<='0';
code<="0110";
reset<='0';
wait For 20 ns;
```

ASSERT door = '0' and alarm ='1'

REPORT "16 error"

SEVERITY error;

WAIT;

END PROCESS ;

END ARCHITECTURE ;