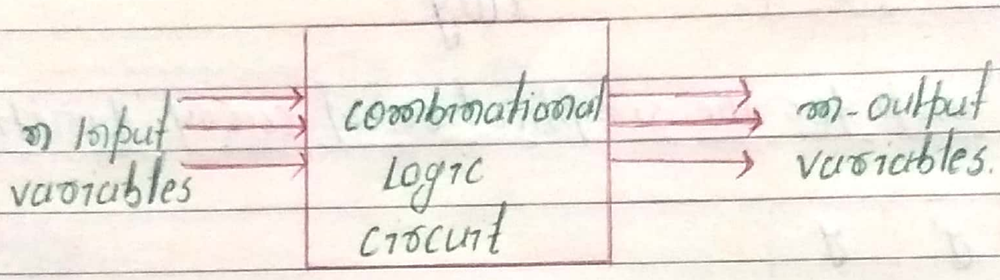
Combinational logic Circuits:

- A combinational circuit consists of logic gates, they perform a specific information processing operation fully specified logically by a set of Boolean function.



- n input variables these 2^n possible combinations of binary inputs. for each possible input combination, there is one and only one possible output combination.

- A combinational circuit can be described by m Boolean function. one for each output variable.

Half Adder:

It is a combinational CKT that perform addition of Two bits.

: Truth Table:

x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

: addition
1+1 with a carry 1

÷ K→ map for the simplification of sum function

	y'	y
x'	0	1
x	1	0

÷ $S = x'y + xy'$
$x \oplus y$

÷ K→ map for the simplification of carry function

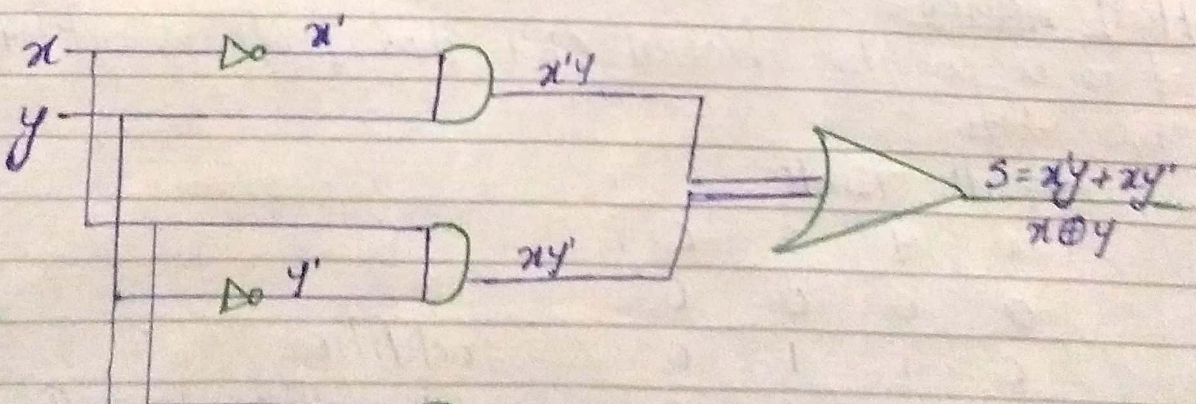
	y'	y
x'	0	0
x	0	1

÷ $C = xy.$

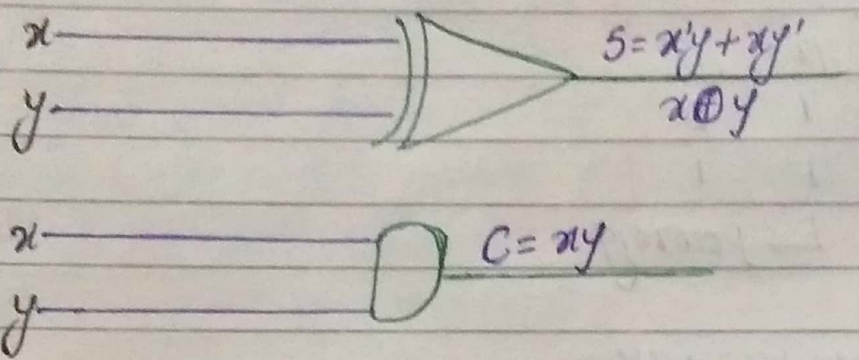
÷ Implementation of Half adder

$S = x'y + xy'$
$x \oplus y$

$C = xy$



÷ Implementation of half adder with EX-OR and AND Gate



Full adder:

- It is combinational CKT that performed addition of three Bits.

÷ Truth table

x	y	z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

÷ K→ Map for the simplification of sum function ÷

	y'z'	y'z	yz	yz'
x'	0	1	0	1
x	1	0	1	0

÷ $S = x'y'z + x'yz' + xy'z' + xyz$

$x'[y'z + yz'] + x[y'z' + yz]$

$S = x \oplus y \oplus z$

÷ K→ Map for the simplification of carry function.

	$y'z'$	$y'z$	yz	yz'
x'	0	0	1	0
x	0	1	1	1

↳ pairing.

÷ $C = yz + xz + xy$

÷ Implementation of full adder ÷

$S = x'yz' + x'yz' + xy'z' + xyz$

$= x'[yz' + yz'] + x[y'z' + yz]$

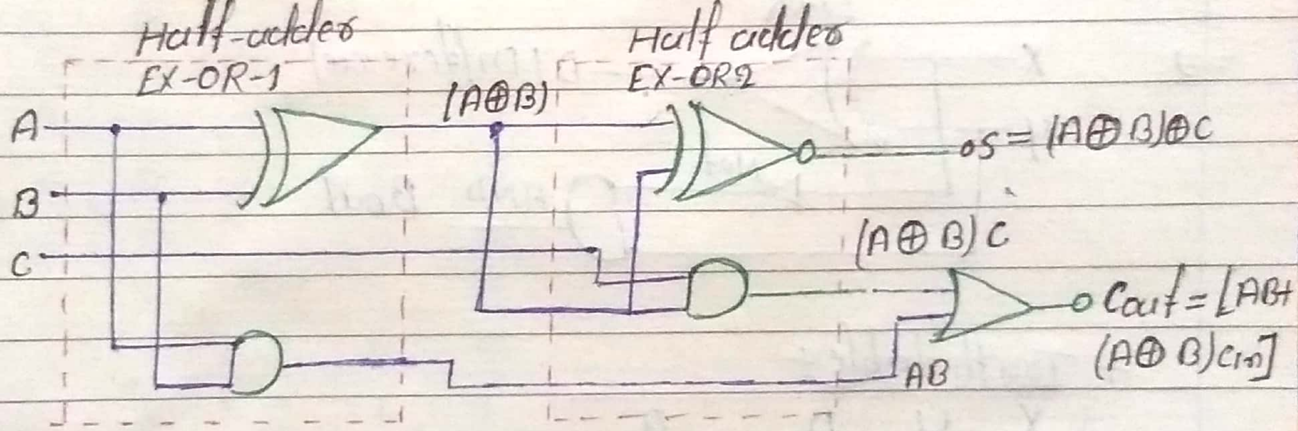
$S = x \oplus y \oplus z$

$C = yz + xz + xy$

Design a FULL adder with two Half adder:

- The Full-adder must add the two input bits and the input carry.
- The input carry to be added to the input bits, it must be EX-OR with $A \oplus B$ giving the equation for the sum output of the full adder.

$$S = (A \oplus B) \oplus C$$



BINARY Subtractor:

- opposite of the Binary adder. it subtracts two binary no. from each other. The output is Difference [D] and a Borrow [B]

Binary substructor of two Bits:

(I) 0-0 → 0 [D], Borrow not req.

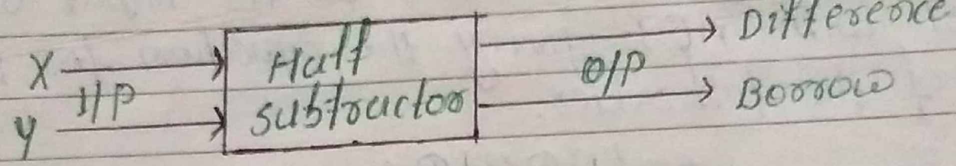
(III) 1-1 → 0 (D), B X

(II) 1-0 → 1 [D], B X

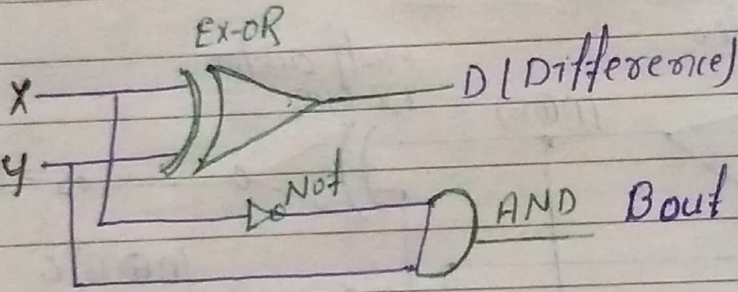
(IV) 0-1 → 1 [D], 1 Borrow

Half subtractor

- it produced a difference and borrow Bits.
- A half subtractor is an arithmetic circuit which is used to perform subtraction of two bits.



⇒



÷ Truth table ÷

X	y	D	B
0	0	0	0
1	0	1	0
0	1	1	1
1	1	0	0

$$D = \bar{x}y + x\bar{y}$$

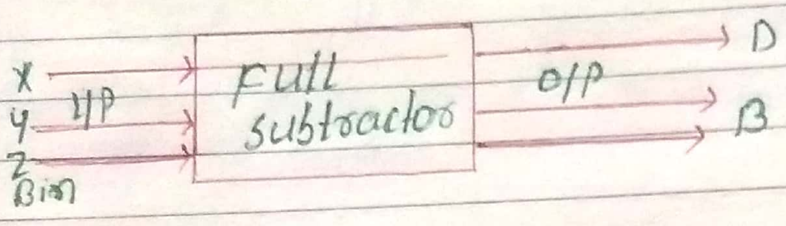
$$x \oplus y \quad \text{— (I)}$$

$$B = \bar{x} \cdot y \quad \text{— (II)}$$

Disadv.→ No provision for Borrow in from ~~Provision~~ previous circuit.

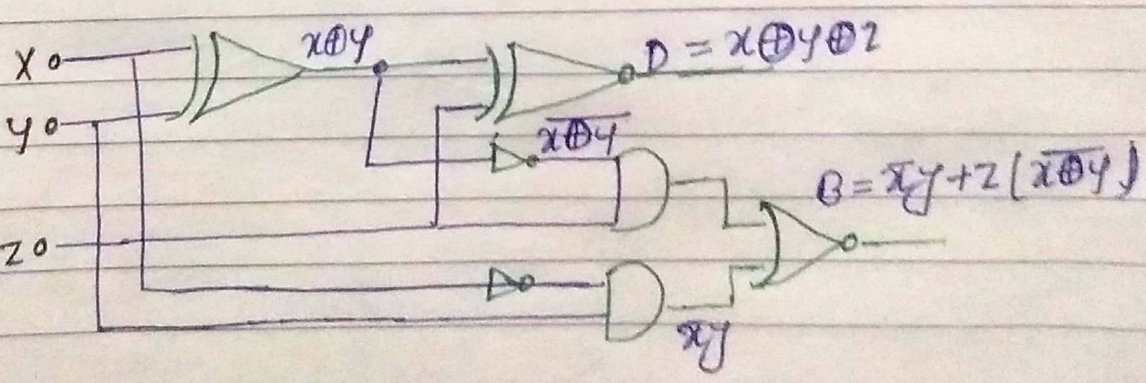
Full subtractor :-

- it has three input, one additional Borrow in (Bin) I/P to receive the Borrow generated by the subtraction process from previous stage ~~input~~.



:- Truth table :-

Bin	X	Y	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

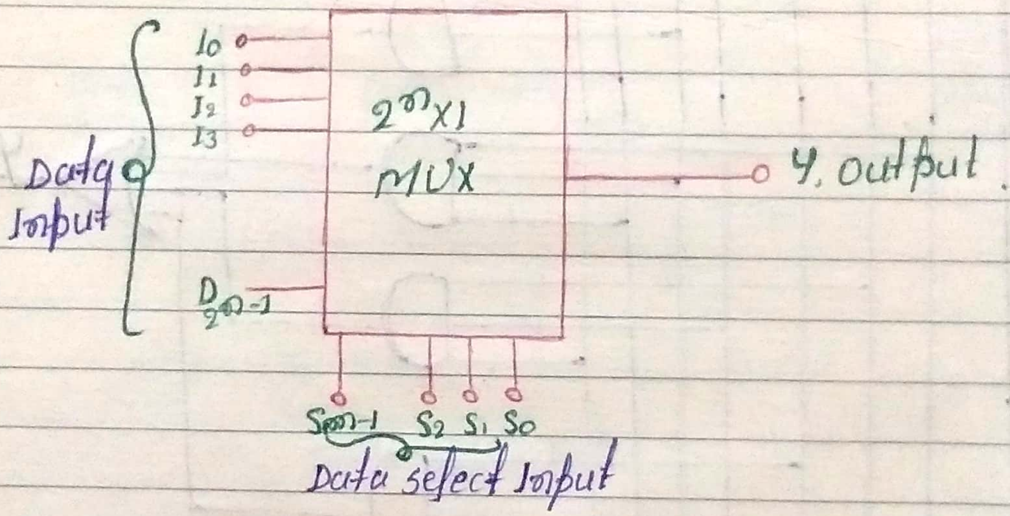


$D = (X \oplus Y) \oplus B_{in}$ — ①

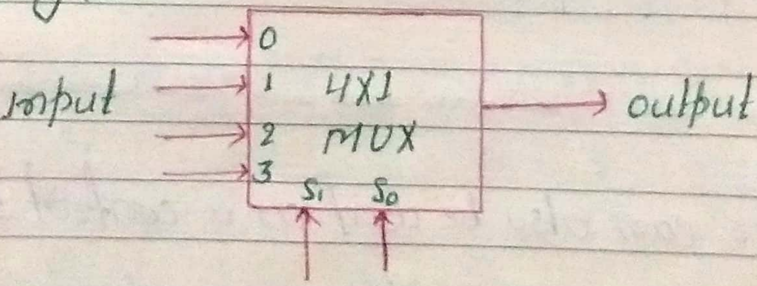
$B_{out} = (\bar{X} \cdot Y) + (\overline{X \oplus Y})\, B_{in}$ — (iii)

Multiplexer : [MUX]

- Multiplexer is a combinational logic circuit used to select only one input among several input based on selection lines
- This can act as digital switch.
- This is also called as data selector
- For a MUX there can be 2^n input n selection lines and only one output.



- Block diagram :



- Function Table :

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

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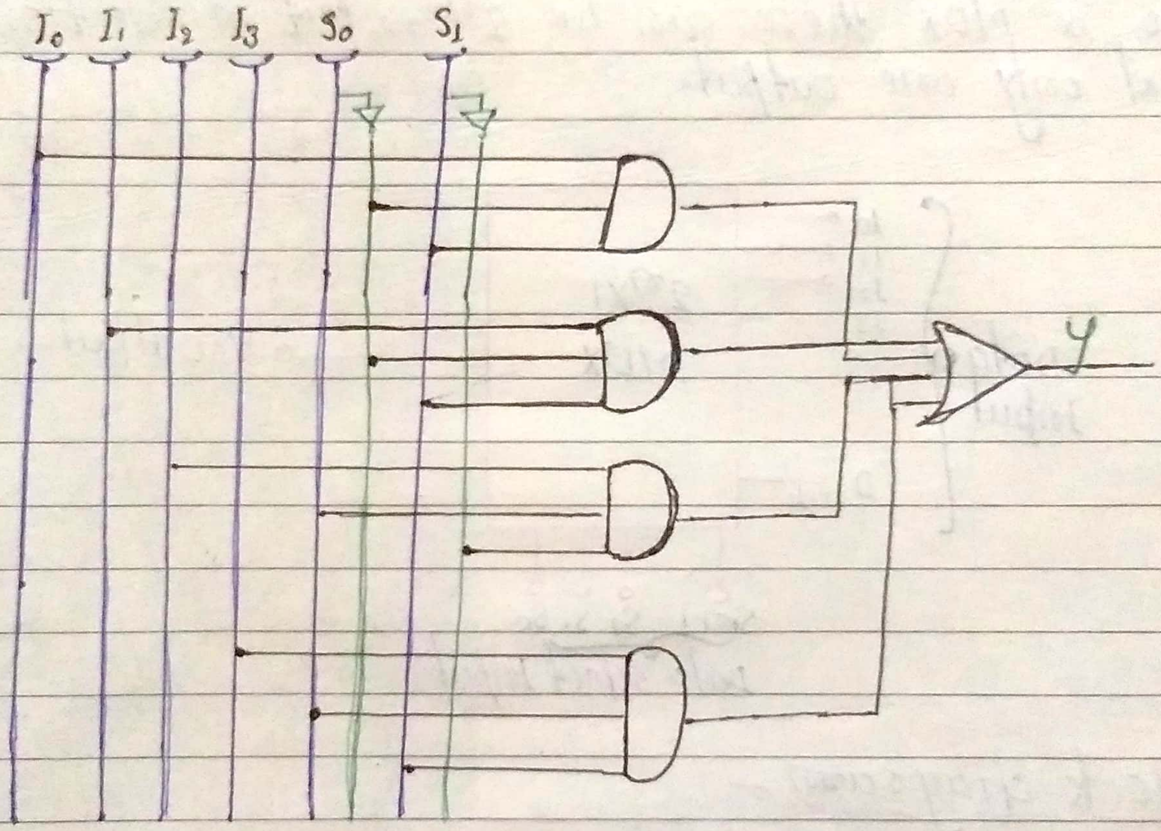
Logic Diagram :-

$$y = D_0 \bar{S}_0 \bar{S}_1 + D_1 \bar{S}_0 S_1 + D_2 S_0 \bar{S}_1 + D_3 S_0 S_1$$

$$= I_0 \bar{S}_0 S_1 + I_1 \bar{S}_0 S_1 + I_2 S_0 \bar{S}_1 + I_3 S_0 S_1$$

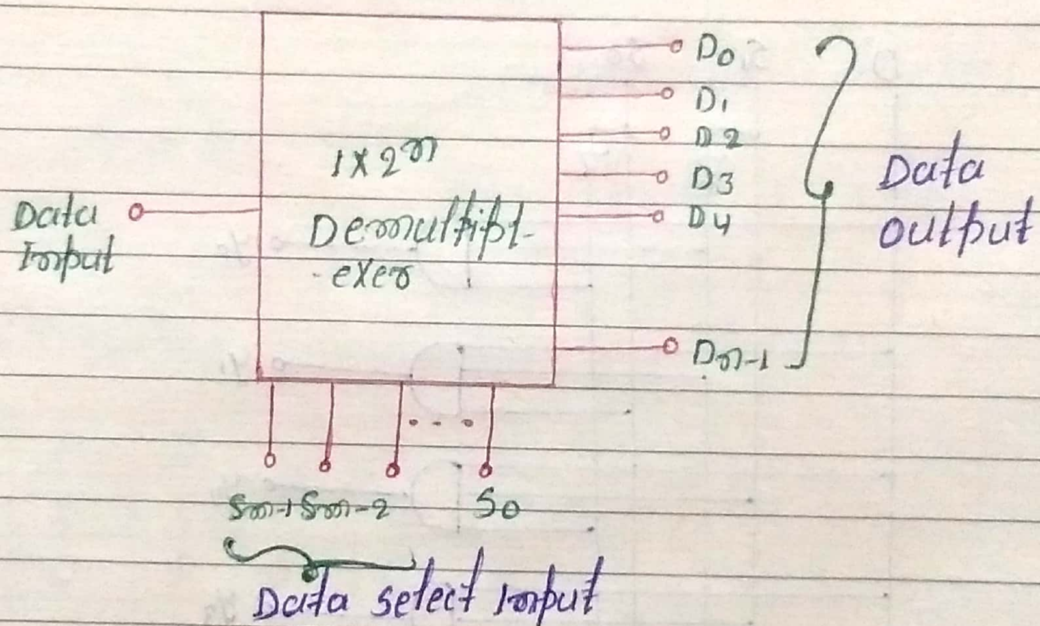


Application :-

- A multiplexer can also be used as a control sequencer.
- A multiplexer can be used for waveform generation.
- The data in parallel form is converted to serial form using multiplexer.

De-multiplexer :-

- It takes a single input line and routes it to one of several digital line.
- 2^n output has n select lines.
- it is also called data distributor.
- it is opposite of multiplexer.

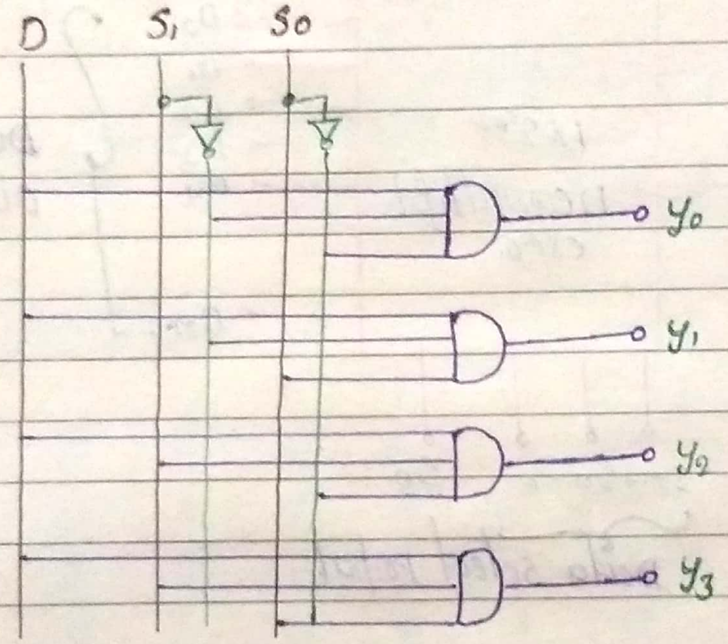


- Function Table :-

Data I/P	Data select input		Outputs			
D	S_1	S_0	Y_3	Y_2	Y_1	Y_0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

- **Logic diagram:-**

$$y_0 = \bar{S}_1 \bar{S}_0 D \quad \text{— (i)}$$
$$y_1 = \bar{S}_1 S_0 D \quad \text{— (ii)}$$
$$y_2 = S_1 \bar{S}_0 D \quad \text{— (iii)}$$
$$y_3 = S_1 S_0 D \quad \text{— (iv)}$$

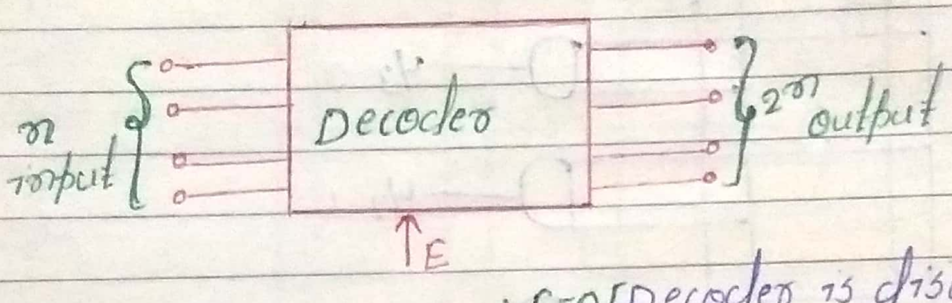


- **Application:-**
- Demultiplexers are used a clock demultiplexers in synchronous data transmission systems in the receivers and security monitoring systems etc.

- This device is very useful if multiple output combinational circuit is to be designed.

Decoder:

- Decoder is a multi-input multi-output logic circuit which decodes n input into 2^n possible output.



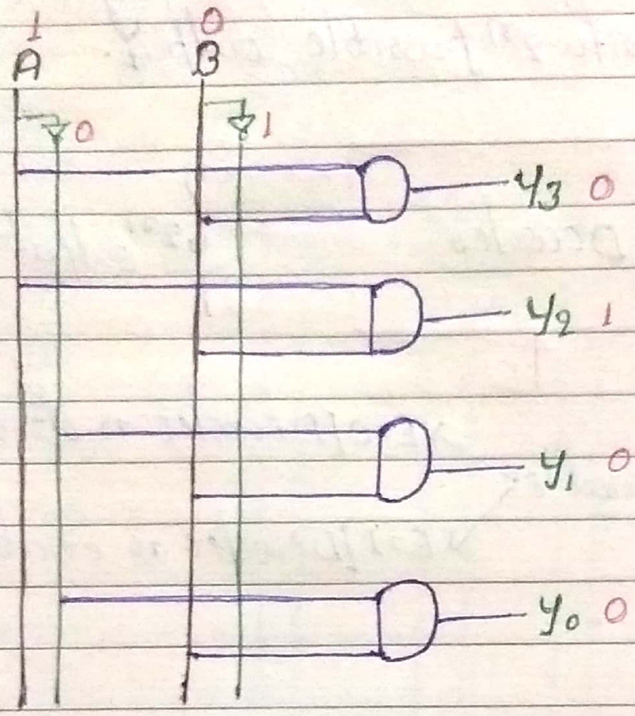
where E = Enable → E=0 [Decoder is disable]
→ E=1 [Decoder is enable]

2 to 4 Decoder

E	A	B	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
	0	1	0	0	1	0
	1	0	0	1	0	0
	1	1	1	0	0	0

$$\left.\begin{aligned} Y_0 &= \bar{A}\bar{B} \\ Y_1 &= \bar{A}B \\ Y_2 &= A\bar{B} \\ Y_3 &= AB \end{aligned}\right\} Y$$

logic diagram :



Application :

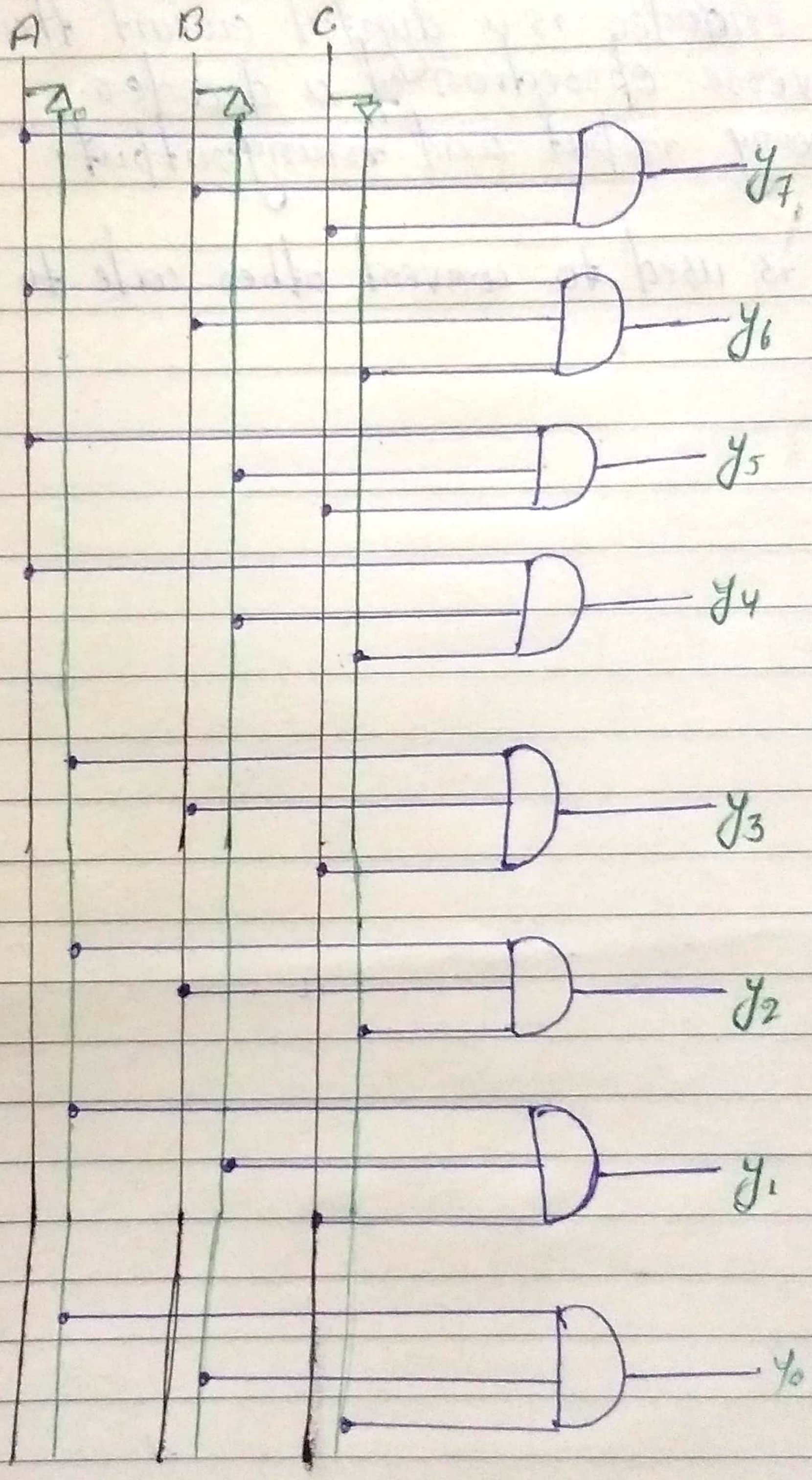
- They are used in analog to digital converters.
- Decoder output can be used to drive a display system.

3 to 8 line decoder

A	B	C	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

logic diagram :-

$y_7 = ABC$
$y_6 = AB\bar{C}$
$y_5 = A\bar{B}C$
$y_4 = A\bar{B}\bar{C}$
$y_3 = \bar{A}BC$
$y_2 = \bar{A}B\bar{C}$
$y_1 = \bar{A}\bar{B}C$
$y_0 = \bar{A}\bar{B}\bar{C}$



Encoder:-

- An encoder is a digital circuit that performs the inverse operation of a decoder.
- many input and many output.
- it is used to convert other code to binary.