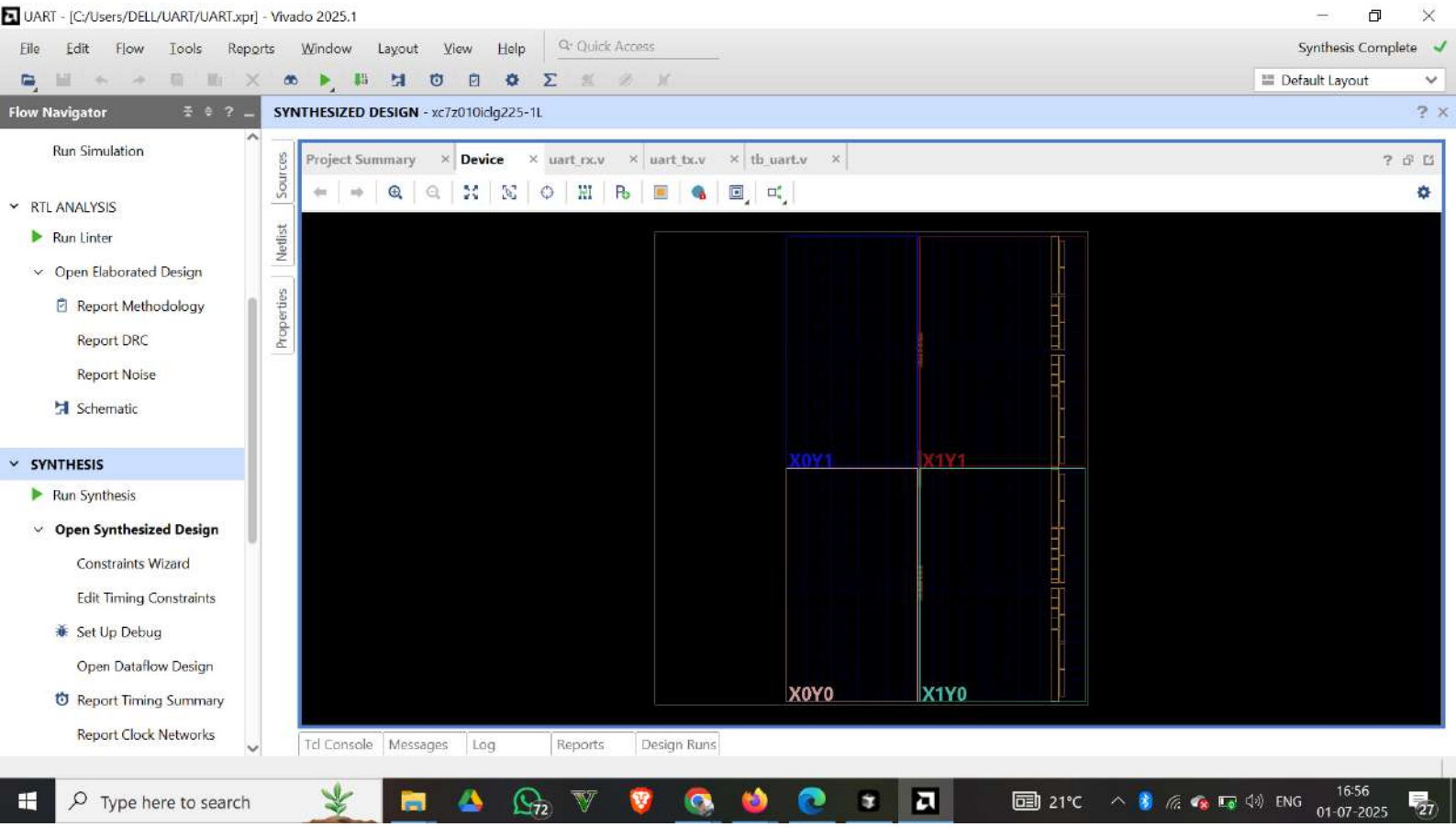
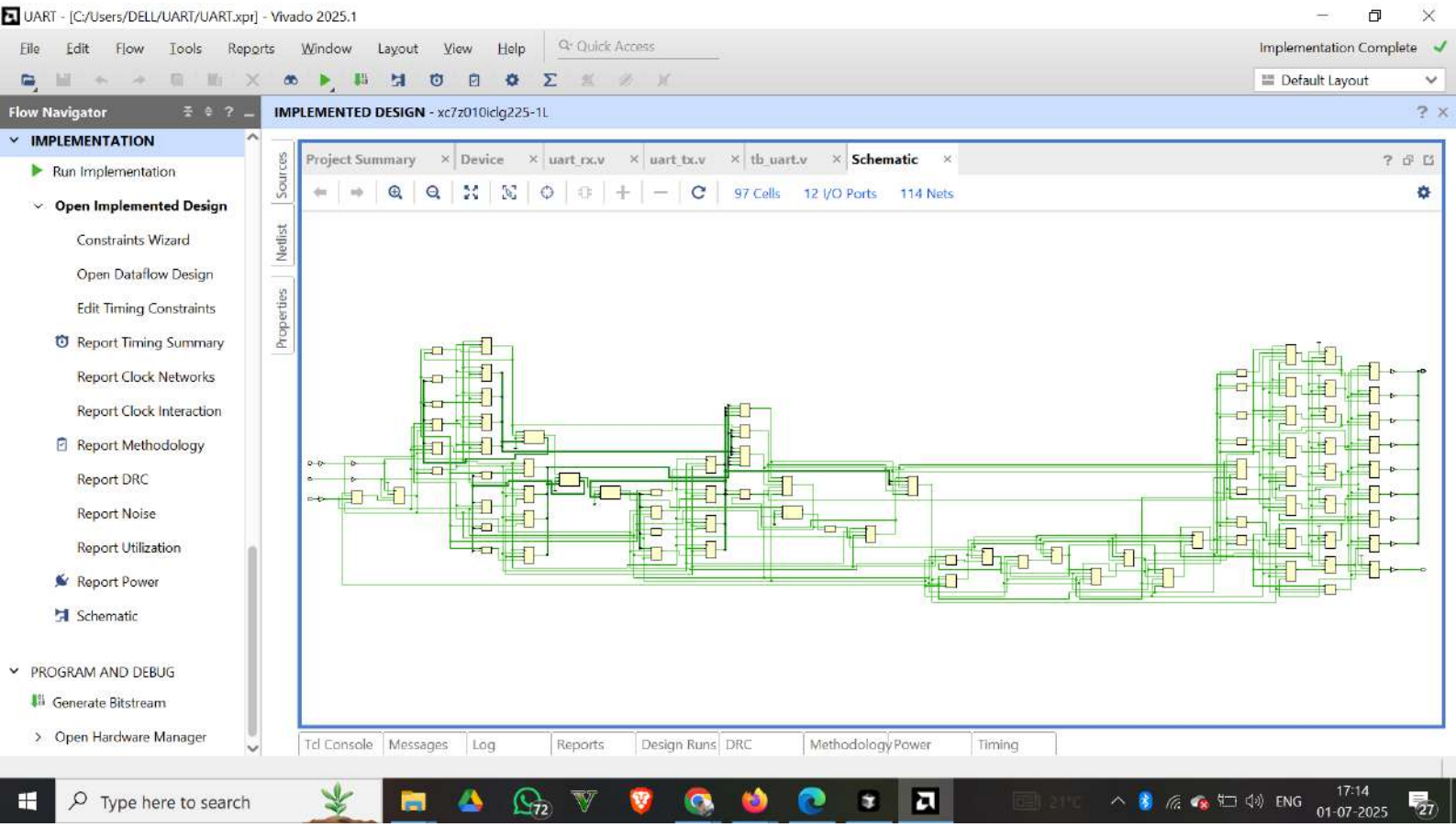
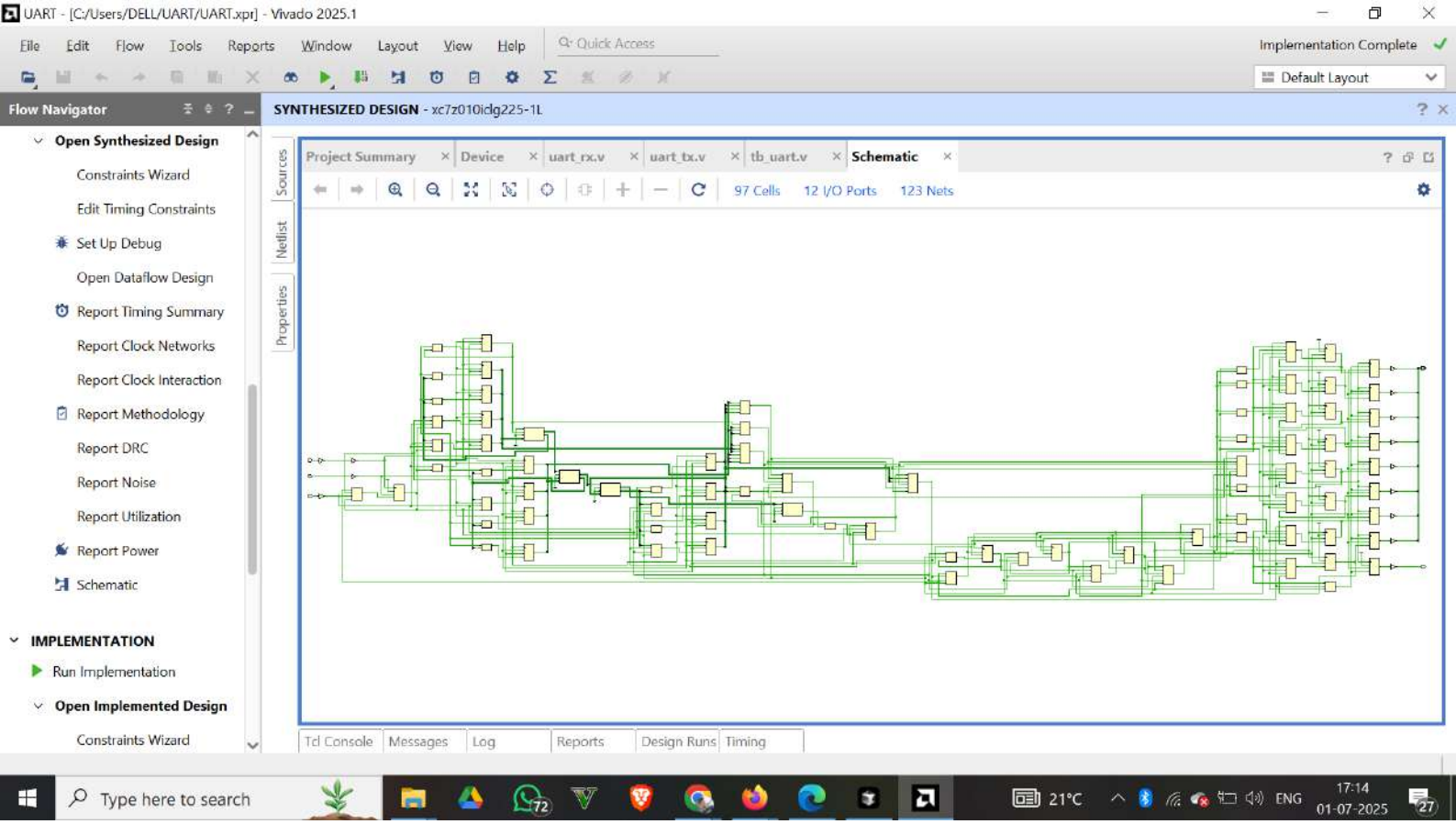
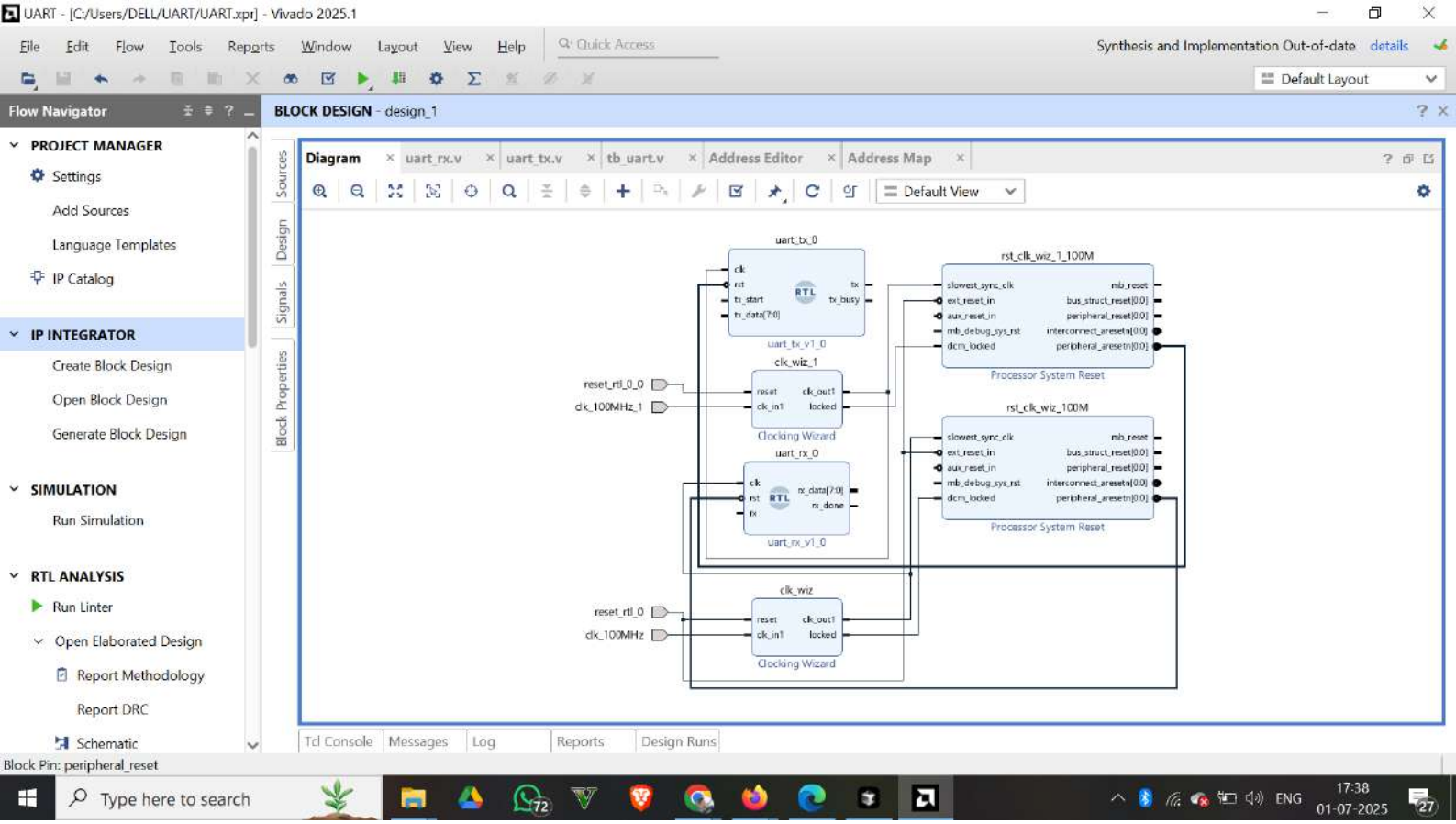
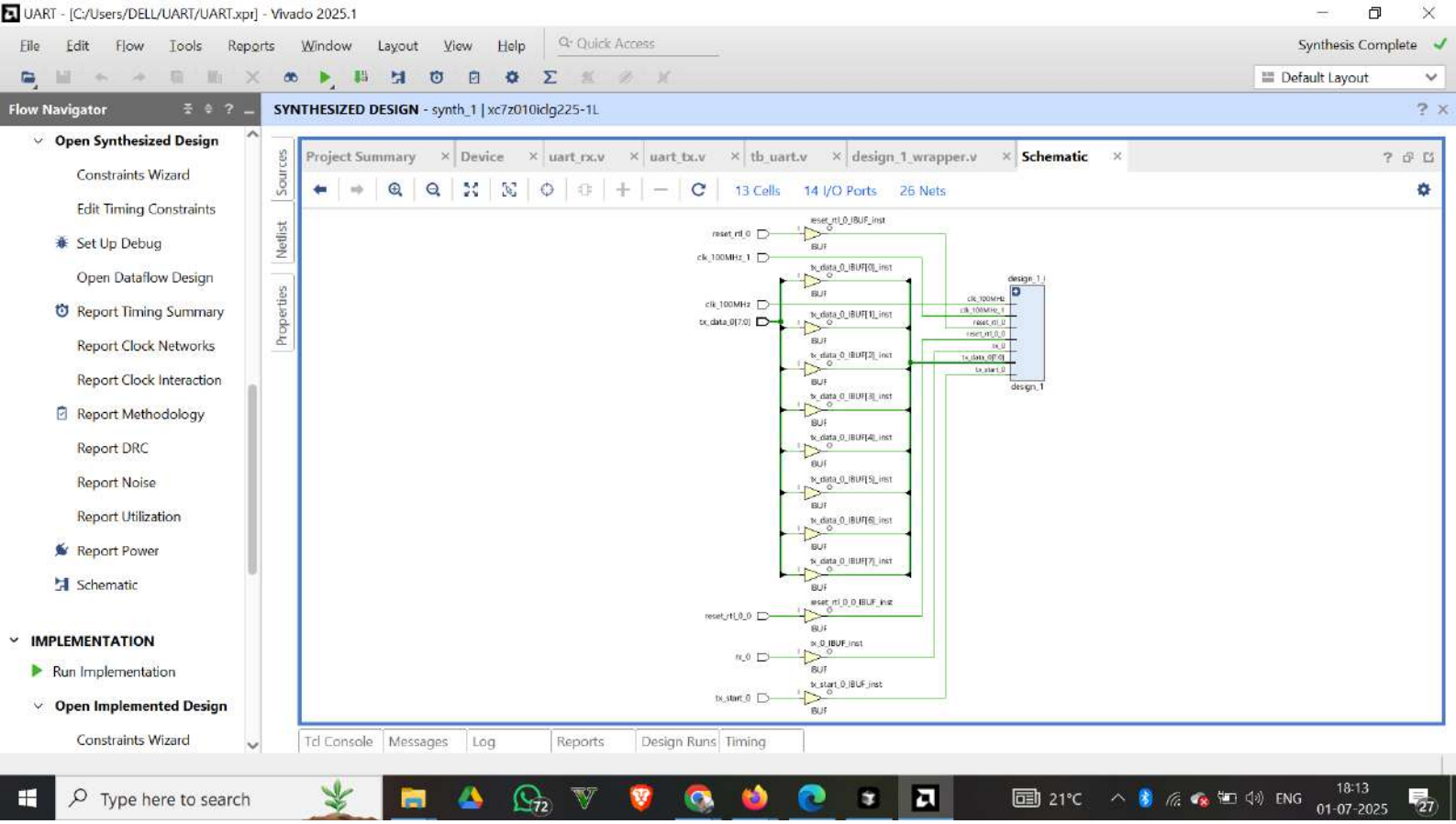
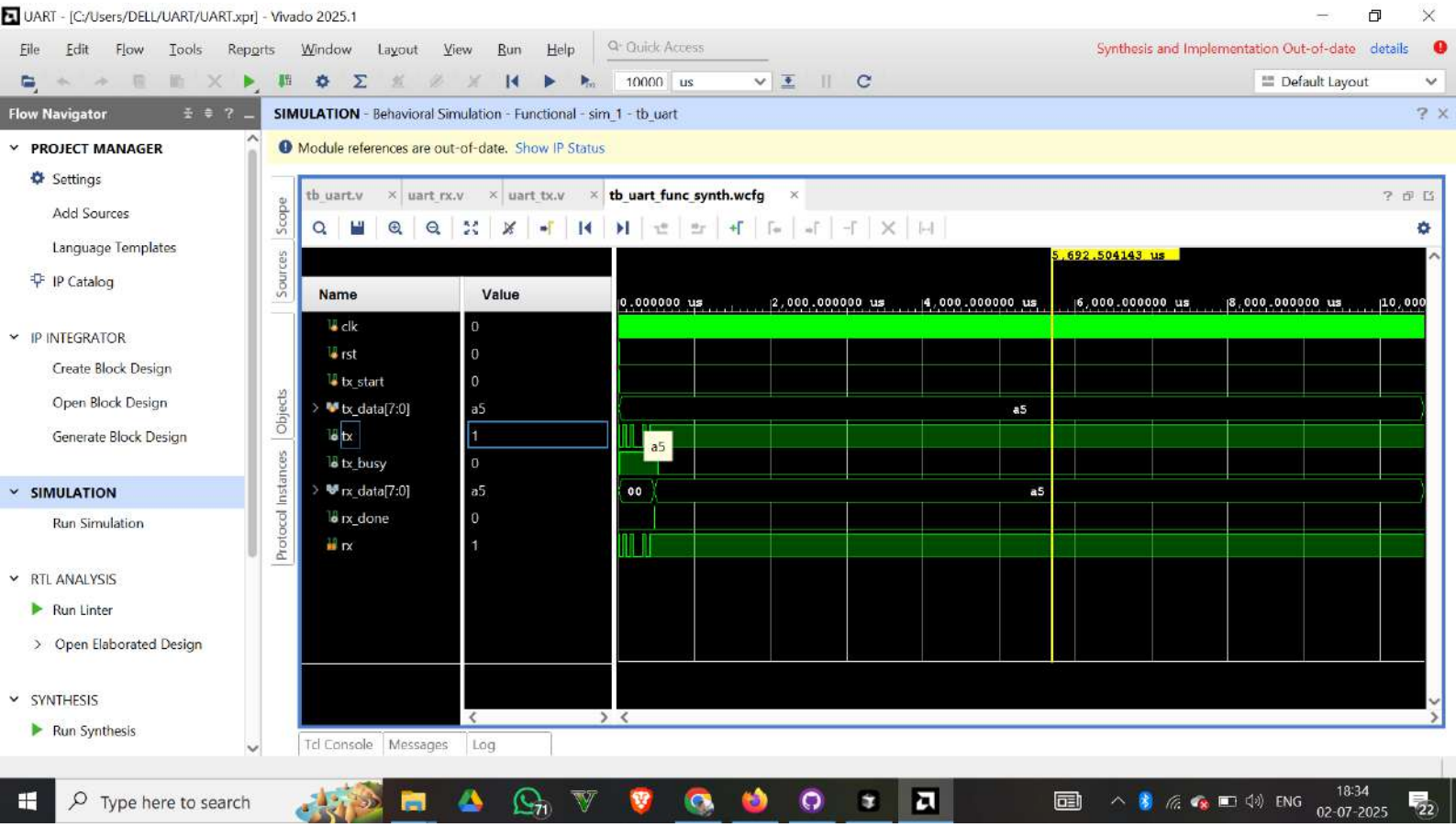

UART - [C:/Users/DELL/UART/UART.xpr] - Vivado 2025.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Complete
Default Layout
Flow Navigator
SYNTHESIZED DESIGN - xc7z010iclg225-1L
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Open Dataflow Design
Report Timing Summary
Report Clock Networks
Sources
Netlist
Properties
Project Summary
Device
uart_rx.v
uart_tx.v
tb_uart.v
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
Type here to search
21°C
ENG
16:56
01-07-2025

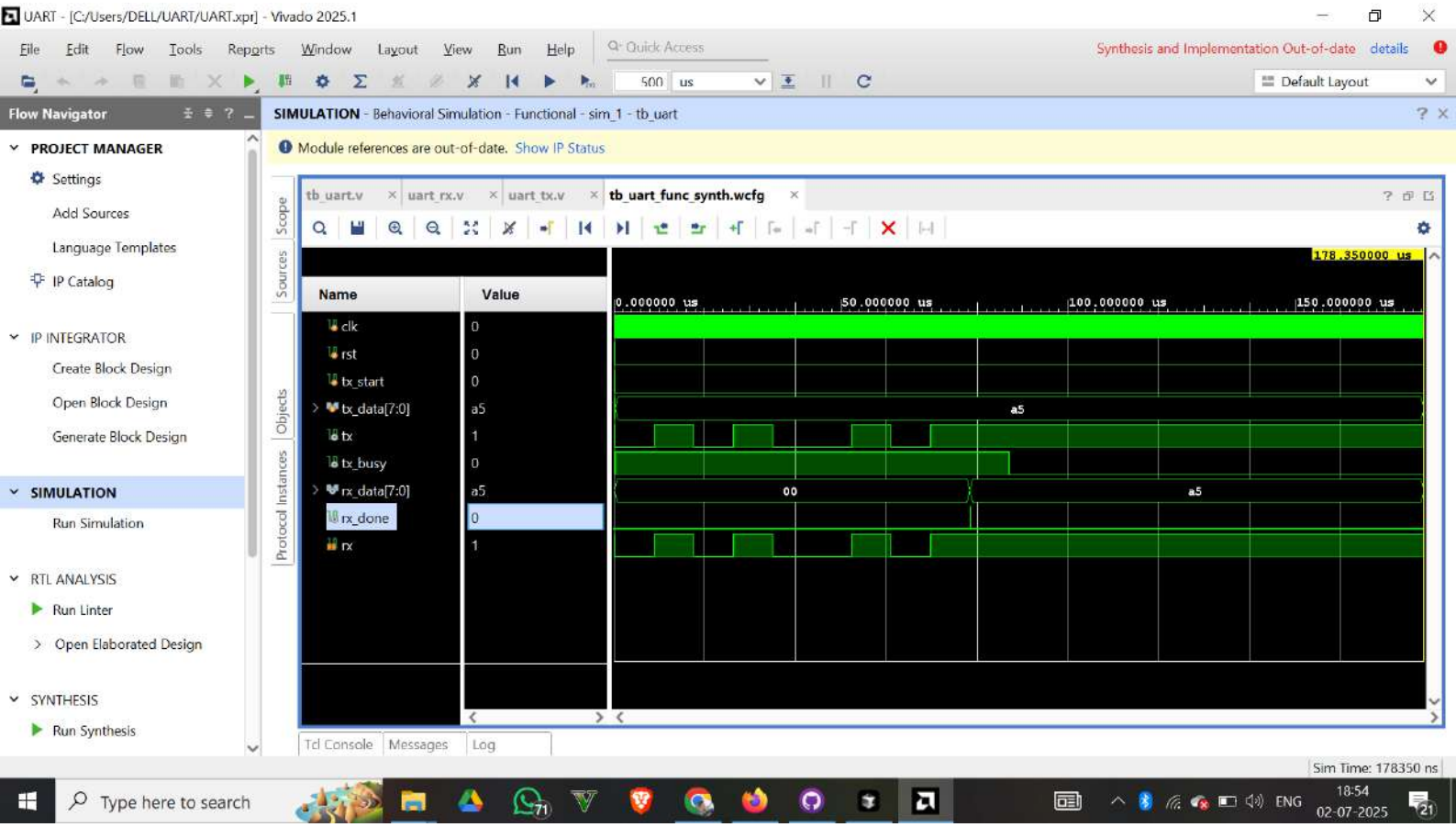

UART - [C:/Users/DELL/UART/UART.xpr] - Vivado 2025.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Open Dataflow Design
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
IMPLEMENTED DESIGN - xc7z010iclg225-1L
Sources
Netlist
Properties
Project Summary
Device
uart_rx.v
uart_tx.v
tb_uart.v
Schematic
97 Cells
12 I/O Ports
114 Nets
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Methodology
Power
Timing
Type here to search
ENG
17:14
01-07-2025


UART - [C:/Users/DELL/UART/UART.xpr] - Vivado 2025.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
SYNTHESIZED DESIGN - xc7z010iclg225-1L
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Open Dataflow Design
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Sources
Netlist
Properties
Project Summary
Device
uart_rx.v
uart_tx.v
tb_uart.v
Schematic
97 Cells
12 I/O Ports
123 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Timing
Type here to search
21°C
ENG
17:14
01-07-2025


UART - [C:/Users/DELL/UART/UART.xpr] - Vivado 2025.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis and Implementation Out-of-date details
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Schematic
BLOCK DESIGN - design_1
Diagram
uart_rx.v
uart_tx.v
tb_uart.v
Address Editor
Address Map
Default View
Sources
Design
Signals
Block Properties
uart_tx_0
uart_tx_v1_0
clk_wiz_1
Clocking Wizard
reset_rtl_0_0
clk_100MHz_1
uart_rx_0
uart_rx_v1_0
rst_clk_wiz_1_100M
Processor System Reset
clk_wiz
reset_rtl_0
clk_100MHz
Tcl Console
Messages
Log
Reports
Design Runs
Block Pin: peripheral_reset
Type here to search
ENG
17:38
01-07-2025


UART - [C:/Users/DELL/UART/UART.xpr] - Vivado 2025.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Synthesis Complete
Default Layout
Flow Navigator
SYNTHESIZED DESIGN - synth_1 | xc7z010iclg225-1L
Open Synthesized Design
Constraints Wizard
Edit Timing Constraints
Set Up Debug
Open Dataflow Design
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Sources
Netlist
Properties
Project Summary
Device
uart_rx.v
uart_tx.v
tb_uart.v
design_1_wrapper.v
Schematic
13 Cells
14 I/O Ports
26 Nets
reset_rtl_0
clk_100MHz_1
clk_100MHz
tx_data_0[7:0]
reset_rtl_0_0
tx_0
tx_start_0
design_1
IBUF
Tcl Console
Messages
Log
Reports
Design Runs
Timing
Type here to search
21°C
ENG
18:13
01-07-2025


UART - [C:/Users/DELL/UART/UART.xpr] - Vivado 2025.1
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Synthesis and Implementation Out-of-date details
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
SYNTHESIS
Run Synthesis
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_uart
Module references are out-of-date. Show IP Status
tb_uart.v
uart_rx.v
uart_tx.v
tb_uart_func_synth.wcfg
Scope
Sources
Objects
Protocol Instances
Name
Value
clk 0
rst 0
tx_start 0
tx_data[7:0] a5
tx 1
tx_busy 0
rx_data[7:0] a5
rx_done 0
rx 1
5,692.504143 us
0.000000 us
2,000.000000 us
4,000.000000 us
6,000.000000 us
8,000.000000 us
10,000
a5
a5
00
a5
Tcl Console
Messages
Log
Type here to search
ENG
18:34
02-07-2025


UART - [C:/Users/DELL/UART/UART.xpr] - Vivado 2025.1
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Synthesis and Implementation Out-of-date details
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
SYNTHESIS
Run Synthesis
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_uart
Module references are out-of-date. Show IP Status
tb_uart.v
uart_rx.v
uart_tx.v
tb_uart_func_synth.wcfg
Name
Value
clk 0
rst 0
tx_start 0
tx_data[7:0] a5
tx 1
tx_busy 0
rx_data[7:0] a5
rx_done 0
rx 1
178.350000 us
0.000000 us
50.000000 us
100.000000 us
150.000000 us
a5
00
a5
Tcl Console
Messages
Log
Sim Time: 178350 ns
Type here to search
ENG
18:54
02-07-2025