**ECE-585 – Microprocessor System Design**

**Test Plan – Group 12**

**Simulation of the Last Level Cache (LLC) for a new processor**

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1. Test case – 01

To verify if the cache initialized correctly that is all line should be invalid upon giving reset.

Steps:

1. Test case – 02 Basic Read/Write operations:

To verify if it is a hit or a miss.

|  |  |
| --- | --- |
| Cache Read: To ensure read operations retrieve data from cache or main memory correctly | Cache write: To ensure write operations update cache and main memory according to write policy |
| Test case – 2.1  Cache Operation: Read Cache Hit/Miss: Hit  Example:  Precondition: Address 0x0004 already exists in the cache  Action taken: Read from the location 0x0004  Expected Result: Data is retrieved from the cache without accessing the main memory. | Test case – 2.3  Cache Operation: Write Cache Hit/Miss: Hit  Example:  Precondition: Address 0x0001 in the cache with Dirty bit set to 0.  Action taken: Write new data to location 0x0001  Expected Result: Cache line is updated, dirty bit is set to 1, but main memory is not updated as this is write back policy. |
| Test case – 2.2  Cache Operation: Read Cache Hit/Miss: Miss  Example:  Precondition: Address 0x0004 is not in the cache  Action taken: Read from the location 0x0004  Expected Result: Cache miss occurs, hence data is fetched from the main memory and cache line is updated | Test case – 2.4  Cache Operation: Write Cache Hit/Miss: Miss  Example:  Precondition: Address 0x0008 not in the cache  Action taken: Write to location 0x0008  Expected Result: Cache miss occurs, fetch the block into the cache, update the cache line and set the dirty bit. |

Number of commands =

Total CPU requests =

Total Cache requests =

Total Cache Hits =

Total Cache Miss =

Cache Hit Ratio =

Cache Hit Percentage =

1. Test case – 03 Eviction Policy

To test the behaviour of the cache when eviction occurs and to check if the dirty bit is managed correctly.

Cache eviction:  
Example:  
Precondition: Set 0 is occupied and address 0x002(LRU) has its dirty bit set

Action: Address 0x002 is evicted and data is written back into the main memory and the new address needed will be loaded into the cache.

1. Test case – 04 Snooping testing