J.C. BOSE UNIVERSITY OF SCIENCE & TECHNOLOGY ,
YMCA **, FARIDABAD , HARYANA**

SEM (2022-2023)

PROJECT REPORT : *VISITOR COUNTER*

SUBMITTED BY :

Mohit (21001008504)

AIM

VISITOR COUNTER

INTRODUCTION

The complete circuit design of Visitor Counter can be divided in two parts: -

1. **Generation of Square Wave while IR Light beam obstructed: -**

This circuit is wired is standard 555-monostable mode. In this, the timing capacitor & resistor define the square wave time duration when the pulse occurs at pin no-3. The pin no-2 (Trigger) is connected to a resistor R-2 to prevent false triggering. When the IR light beam at photo transistor (connected to pin 2 and (+)ve supply) is obstructed, a square wave pulse is generated and this goes to counter for pulse counting circuit via FM transmitter and receiver link.

2. **Pulse Counter: -**

In this given circuit, the two similar decade counters are connected to count 99 max. When the pulse at pin no-1 of IC-4033 it counts and display at seven segment display. And after digit 9 is given a carry pulse to the next counter for rest of the counting digits. The both IC's can be resetted by pressing reset button connected at pin-15.

RIPPLE COUNTER

A counter is a register of counting the number of clock pulses that have arrived at its clock input. In its simplest form it is the electronic equivalent of a binary odometer.

THE CIRCUIT: -

Fig. shows a counter built with JK flip-flops. Since the J and K inputs are returned to a high voltage, each flip-flop will toggle when its clock input receives a negative edge.

Here's how the counter works. Visualize the Q outputs as a binary word

$$Q = Q_3 Q_2 Q_1 Q_0$$

Q_3 is the most significant bit (MSB), and Q_0 is the least significant bit (LSB). When CLR goes low; all flip-flops reset. This results in a digital word of

$$Q = 0000$$

When CLR returns to high, the counter is ready to go. Since the LSB flip-flop receives each clock pulse, Q_0 toggles

once per negative clock edge, as shown in the timing diagram of Fig. The remaining flip-flops toggle less often because they receive their negative edges from the preceding flip-flops.

For instance, when Q_0 goes from 1 back to 0, the Q_1 flip-flop receives a negative edge and toggles. Likewise, when Q_1 changes from 1 back to 0, the Q_2 flip-flop gets a negative edge and toggles. And when Q_2 goes from 1 to 0, the Q_3 flip-flop toggles. In other words, whenever a flip-flop resets to 0, the next higher flip-flop toggles.

What does this remind you of? Reset and carry! Each flip-flop acts like a wheel in a binary odometer; whenever it resets to 0, it sends a carry to the next higher flip-flop. Therefore, the counter of Fig. is the electronic equivalent of a binary odometer.

COUNTING

If CLR goes low then high, the register contents of Fig. become

Q = 0000

When the first clock pulse hits the LSB flip-flop, Q_0 becomes a 1. So the first output word is

Q = 0001

When the second clock pulse arrives, Q_0 resets and carries; therefore, the next output word is

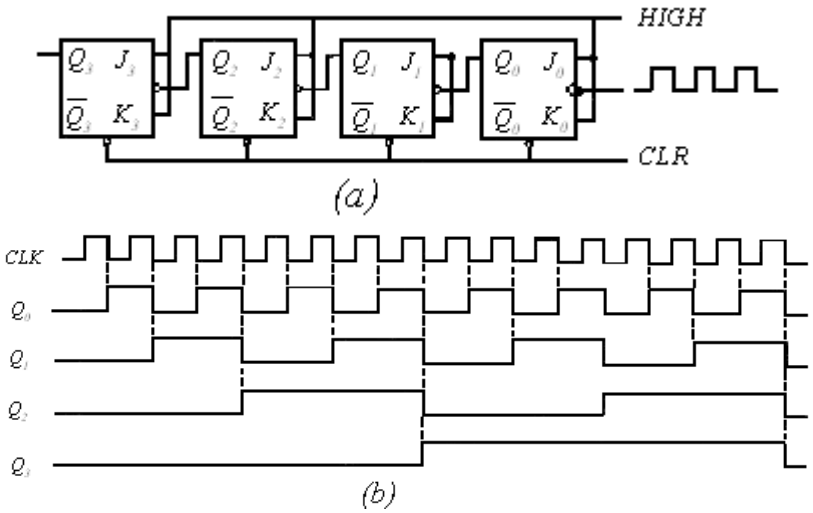
Q = 0010

The third clock pulse advances Q_0 to 1, this gives

Q = 0011

The fourth clock pulse forces the Q_0 the flip-flop to reset and carry. In turn, the Q_1 flip-flop resets and carries. The resulting output word is

Q = 0100



The fifth clock pulse gives

Q = 0110

and the seventh gives

Q = 0111

On the eighth clock pulse, Q_0 resets and carries, Q_1 resets and carries, Q_2 resets and carries, and Q_3 advances to 1. So the output word becomes

Q = 1000

The ninth clock pulse gives

Q = 1001

The tenth gives

Q = 1010

and so on.

The last word is

Q = 1111

corresponding to the fifteenth clock pulse. The next clock pulse resets all flip-flops. Therefore, the counter resets to

Q = 0000

and the cycle repeats.

Table given summarizes the operation of the counter. Count represents the number of clock pulses that have arrived. As you see, the counter output is the binary equivalent of the decimal count.

TABLE: RIPPLE COUNTER

COUNT	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1

2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

DECADE COUNTER

The modulus of a counter is the number of output states it has. A 4-bit ripple counter has a modulus of 16 because it has 16 distinct states numbered from 0000 to 1111. By changing the design we can produce a counter with any desired modulus.

MOD-10 COUNTER :-

Fig. (a) shows a way to build a moduls-10(or mod-10)counter. The circuit counts from 0000 to 1001,as before. However, on the tenth clock pulse, the counter generates its own

clear signal and the count jumps back to 0000. In other words, the count sequence is

$$
\begin{aligned}
Q &= 0000\ (0)\\
Q &= 0001\ (1)\\
Q &= 0010\ (2)\\
Q &= 0011\ (3)\\
Q &= 0100\ (4)\\
Q &= 0101\ (5)\\
Q &= 0110\ (6)\\
Q &= 0111\ (7)\\
Q &= 1000\ (8)\\
Q &= 1001\ (9)\\
Q &= 0000\ (10)
\end{aligned}
$$

As you see, the circuit skips states 10 to 15 (1010 through 1111). The counting sequence is summarized by the state diagram in Fig (b).

Why does the counter skip the states from 10 to 15? Because of the AND gate, the counter can be reset by a low CLR or a low Y. Initially, CLR goes low to produce

$$Q = 0000$$

When $\overline{CLR}$ returns to high, the counter is ready for action. The output of the NAND gate is

$$Y = \overline{Q_3 Q_1}$$

This output is high for the first nine states (0000 to 1001). Nothing unusual happens when the circuit is counting from 0 to 9. Or the tenth clock pulse, however, the Q word becomes

$$Q = 1010$$

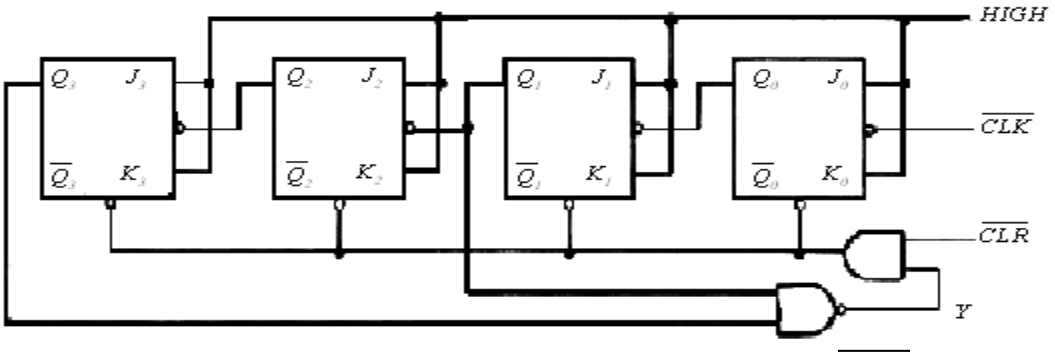
which means that Q_3 and Q_1 are high. Almost immediately, Y goes low, forcing the counter to reset to

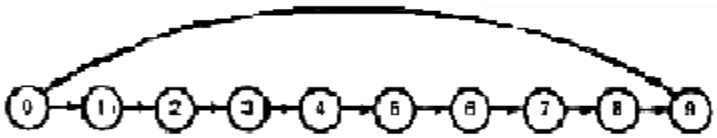
$$Q = 0000$$

Y then goes high, and the counter is ready to start over.

Since it takes 10 clock pulses to reset the counter, the output frequency of the Q, flip-flop is one-tenth of the clock frequency. This is why a mod-10 counter is also known as a divide-by-10 circuit.

A mod-10 counter like Fig. is often called a decade counter. Because it counts from 0 to 9, it is a natural choice in BCD applications like frequency counters, digital voltmeters, and electronic wristwatches.





COMPONENTS LIST

SEMICONDUCTORS:

1. IC1, IC2 4033
2. IC3, IC4 555
3. FND..... 7 SEGMENT DISPLAY (2NOS.)
   (NEGATIVE COMMON)

RESISTORS:

1. R1-R3 ..... 100 K□
2. VR1-VR2 ..... 1M

CAPACITOR:

1. C-1.....10µF Capacitor.

MISCELLANEOUS:

1. S-1 ..... DPDT Switch
2. S-2 ..... Push to ON Switch
3. L.D.R. ..... Light Dependent Resistor
4. LED ..... Light Emitting Diode

CIRCUIT DIAGRAM FOR COUNTERS

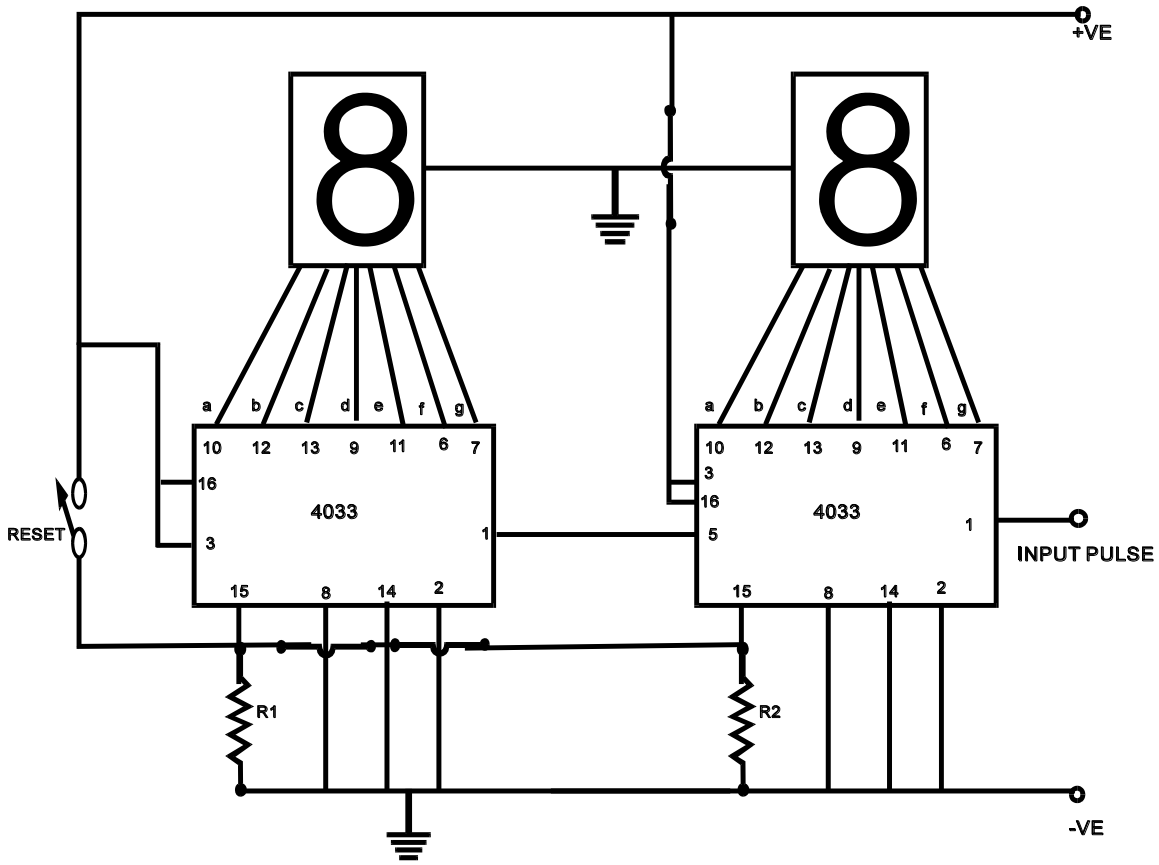
INTERNAL LAYOUT OF I.C. CD4033

DECADE COUNTER/7 SEGMENT DECODER,RIPPLE BLANKING

R	Strobe	LT	T	Function
H	X	X	X	Reset

L	H	L	⎍	Count
L	H	H	X	Lamp test

CIRCUIT DIAGRAM FOR COUNTERS



WORKING

The complete circuit design of Visitor Counter, can be divided in two parts:-

1. GENERATION OF SQUARE WAVE WHILE LDR OBSTRUCTED:-

This circuit is wired is standard 555 monostable mode. In this, the timing capacitor & resistor define the square wave time duration when the pulse occur at pin no-3. When the light at LDR (connected to pin 2 and (+)ve supply) is obstructed, a square wave pulse is generated and this goes to counter for pulse counting circuit.

2. PULSE COUNTER:-

In this given circuit, two similar decade counters are connected to count 99 max. When the pulse at pin no-1 of IC-4033 it counts and display at seven segment display. And after digit 9 is given a carry pulse to the next counter for rest of the counting digits. The both IC's can be resetted by pressing reset button connected at pin-15.