Lab 13
DDR SDRAM

Spring 2025

Submitted by: **Mohsin Sajjad**

Registration No: **22pwsce2149**

Class Section: **A**

"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Mohsin Sajjad

Student Signature: _____

Submitted to:

Engr. Faheem Jan

Month Day, Year (29 05, 2025)

Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

DDR SDRAM

Objective:

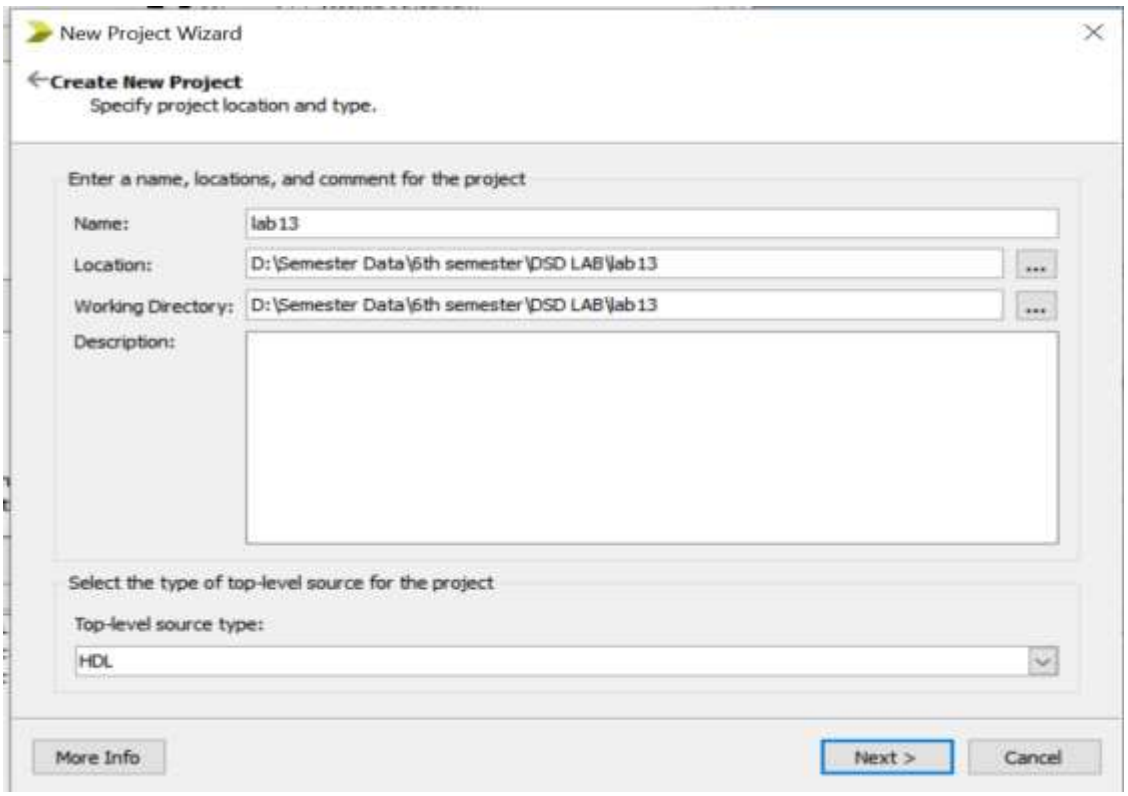
To interface and access DDR SDRAM (512Mbit LPDDR) on the Mimas V2 FPGA development board using Xilinx Spartan-6 and Xilinx ISE 14.7 tools.

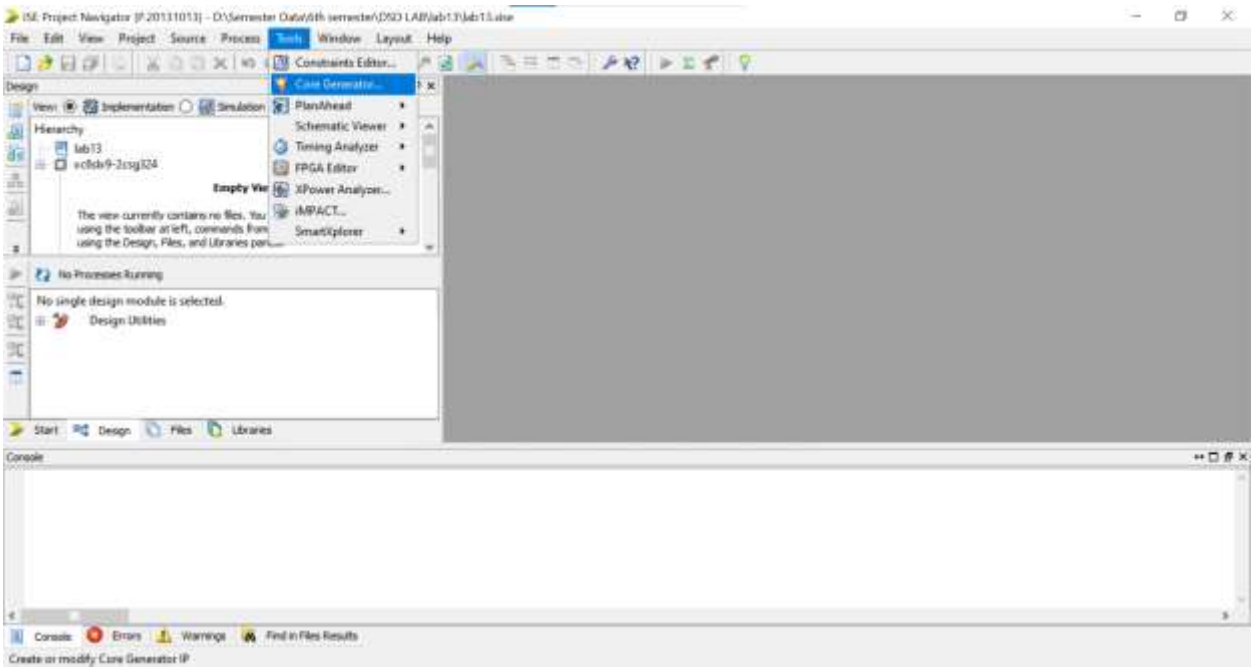
DDR SDRAM: High-speed, volatile memory used for storing data in FPGA-based applications.

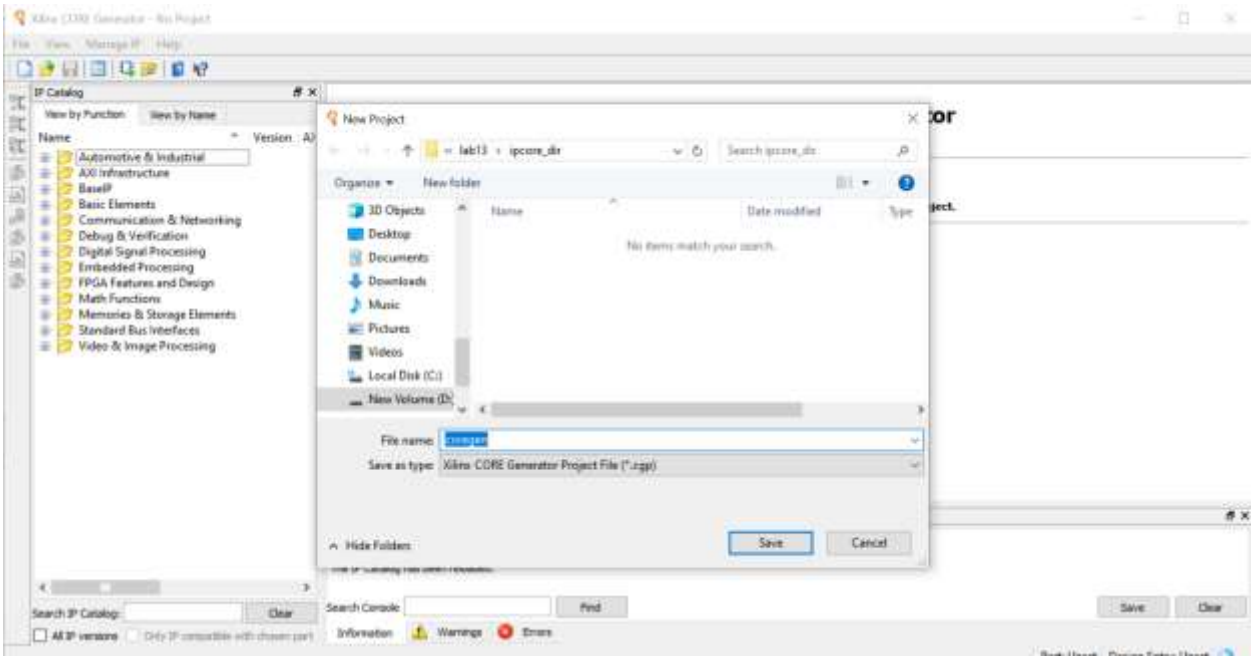
- **Memory Controller**: A logic block (hard or soft) that manages communication between FPGA and DDR.
- **Wrapper Logic**: Bridges user logic to memory controller with a simplified interface.
- **User Logic**: Your custom logic that reads/writes to memory.

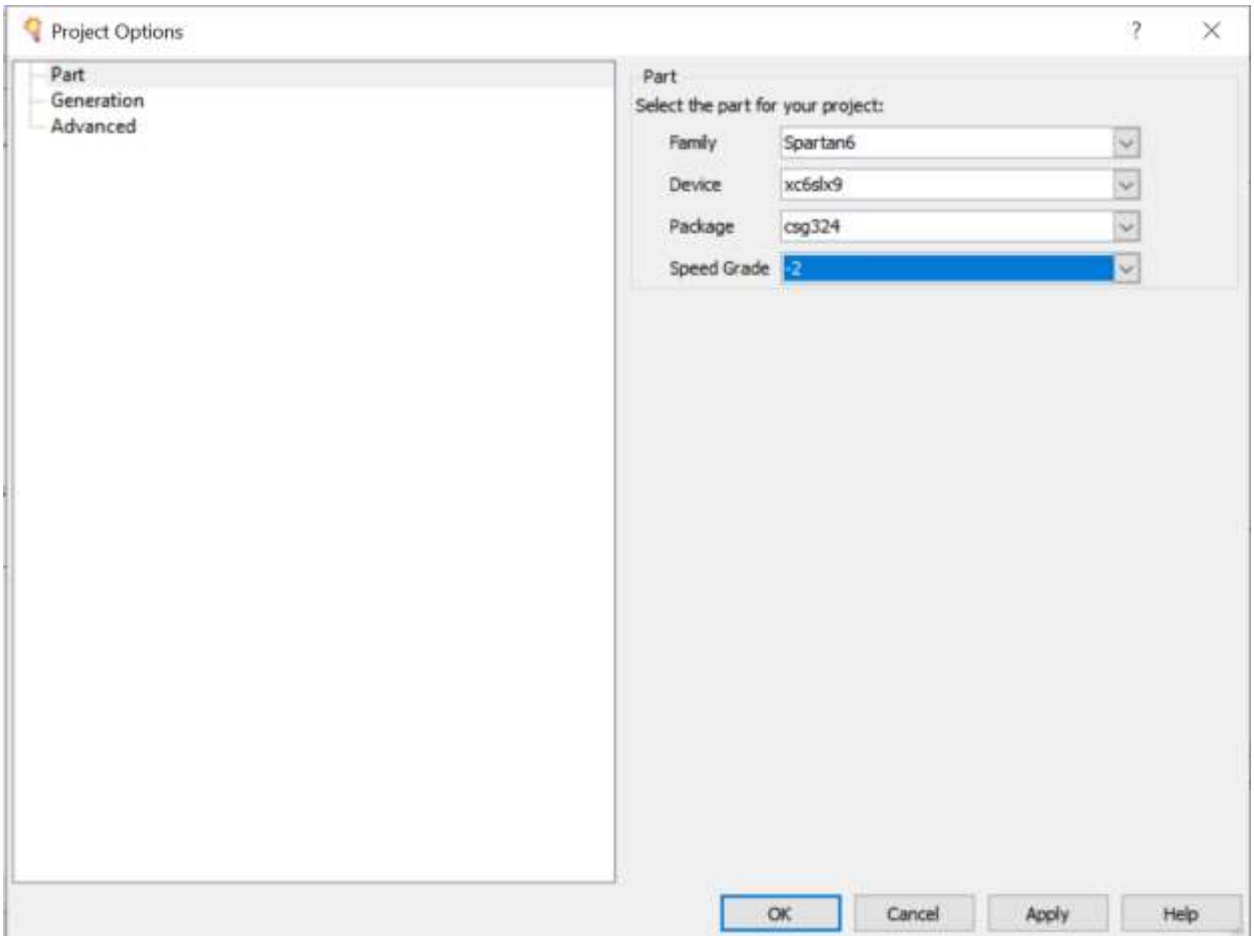
Spartan-6 LX9 (CSG324) includes **two built-in DDR memory controllers**; one is connected to onboard LPDDR on Mimas V2.

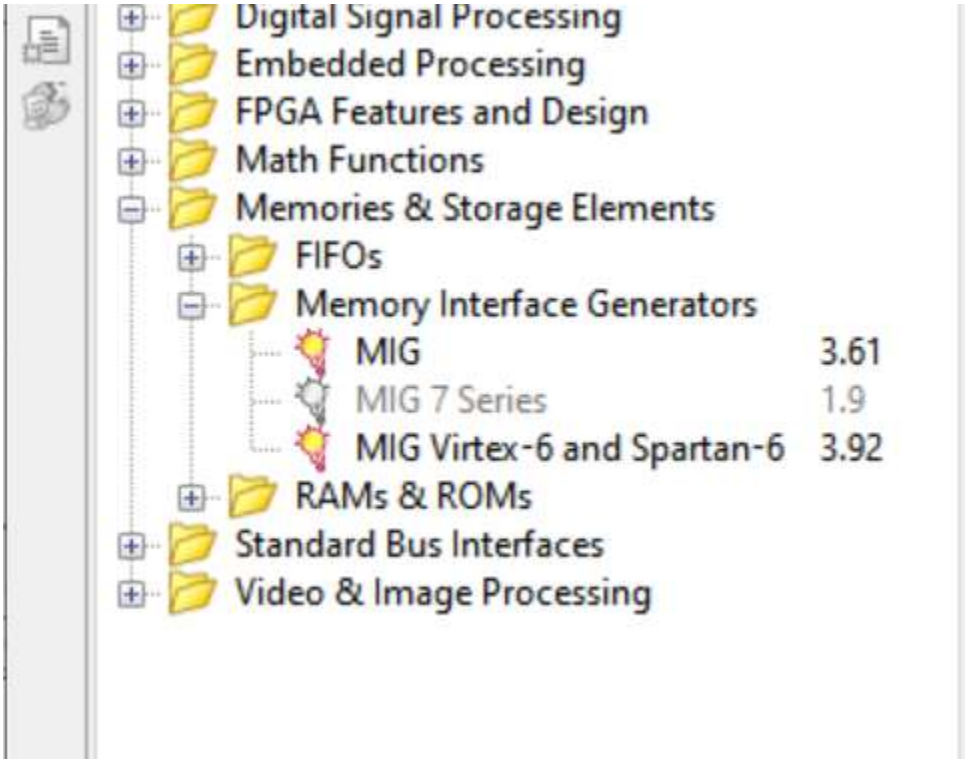
STEPS:



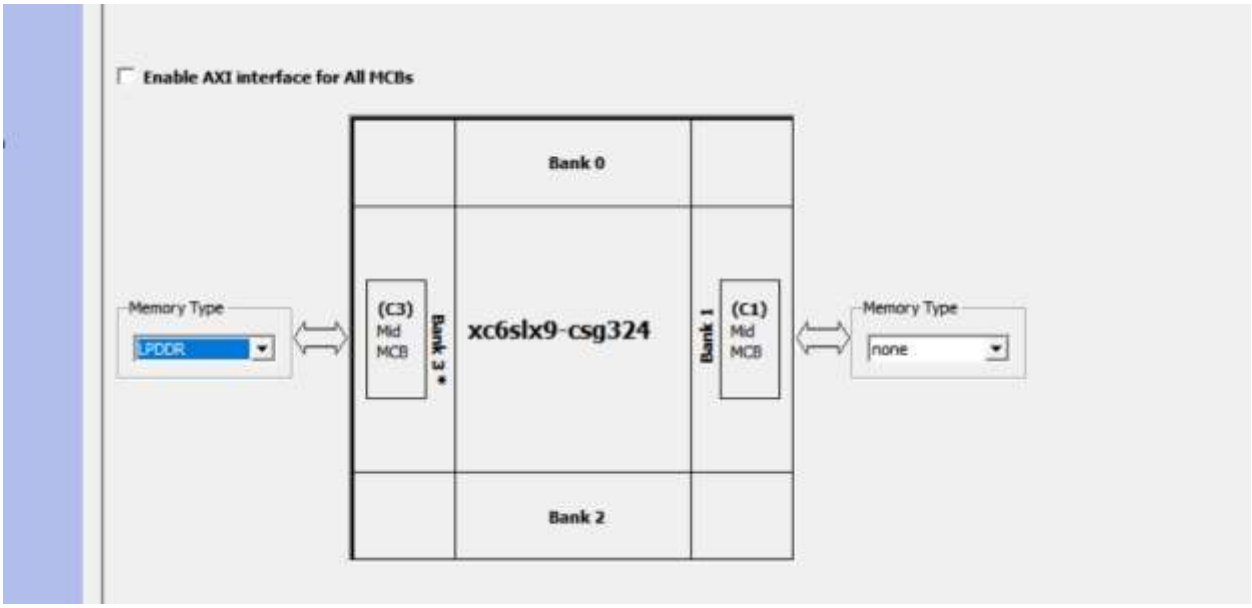

File Edit View Project Source Process Tools Window Layout Help
Constraints Editor...
Core Generator...
PlanAhead
Schematic Viewer
Timing Analyzer
FPGA Editor
XPower Analyzer...
iMPACT...
SmartXplorer
Hierarchy
lab13
No Processes Running
No single design module is selected.
Design Utilities
Start
Design
Files
Libraries
Console
Errors
Warnings
Find in Files Results
Create or modify Core Generator IP

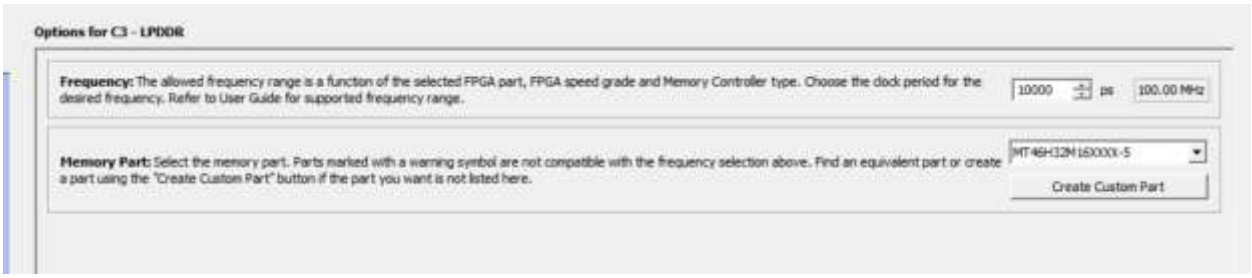

IP Catalog
View by Function
View by Name
Automotive & Industrial
AXI Infrastructure
BaseIP
Basic Elements
Communication & Networking
Debug & Verification
Digital Signal Processing
Embedded Processing
FPGA Features and Design
Math Functions
Memories & Storage Elements
Standard Bus Interfaces
Video & Image Processing
New Project
lab13 › ipcore_dir
Organize
New folder
3D Objects
Desktop
Documents
Downloads
Music
Pictures
Videos
Local Disk (C:)
New Volume (D:)
No items match your search.
File name:
Save as type: Xilinx CORE Generator Project File (*.cgp)
Hide Folders
Save
Cancel
Search IP Catalog:
Clear
Search Console:
Find
Information
Warnings
Errors

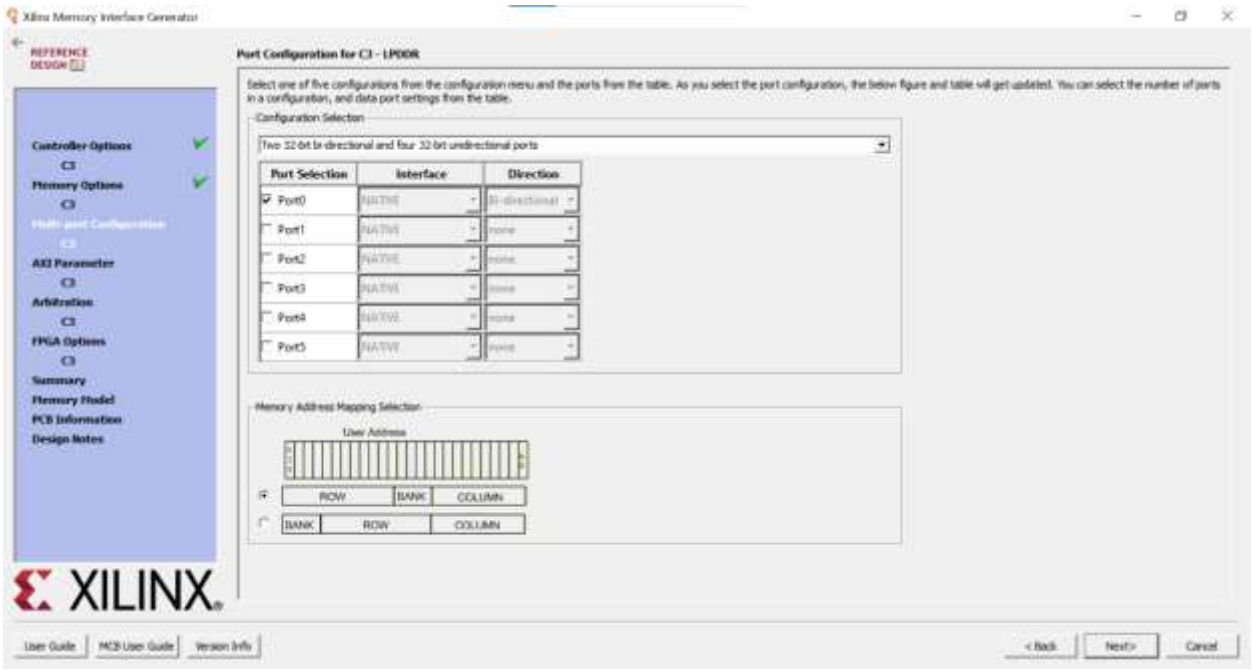

Project Options
Part
Generation
Advanced
Part
Select the part for your project:
Family
Spartan6
Device
xc6slx9
Package
csg324
Speed Grade
-2
OK
Cancel
Apply
Help

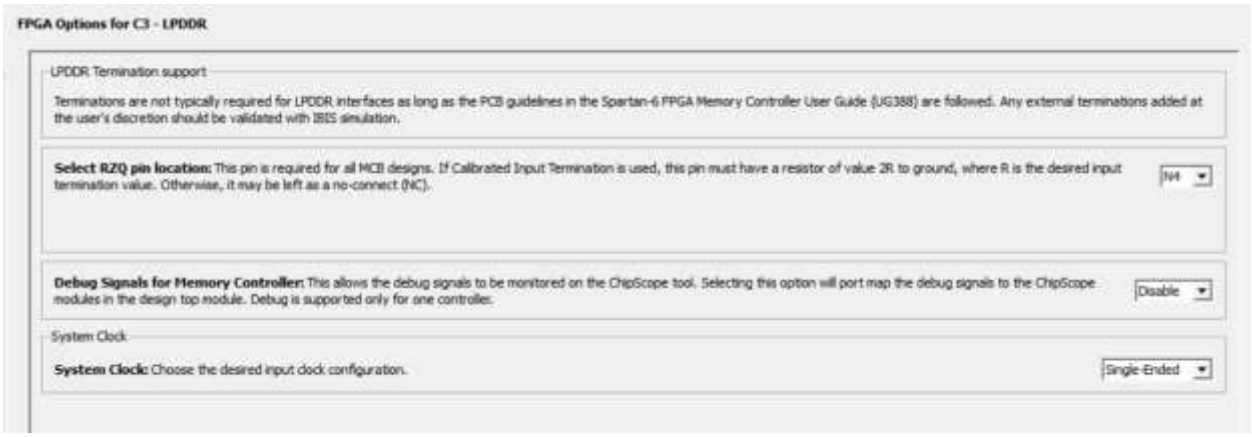

Digital Signal Processing
Embedded Processing
FPGA Features and Design
Math Functions
Memories & Storage Elements
FIFOs
Memory Interface Generators
MIG 3.61
MIG 7 Series 1.9
MIG Virtex-6 and Spartan-6 3.92
RAMs & ROMs
Standard Bus Interfaces
Video & Image Processing

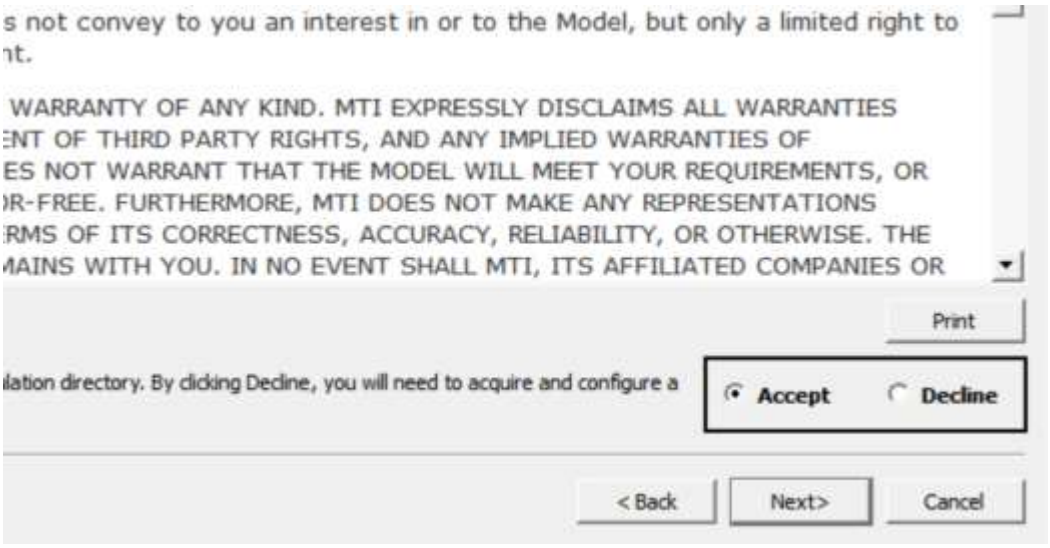

Xilinx Memory Interface Generator
REFERENCE DESIGN
Memory
Interface
Generator
XILINX
MIG Output Options
Create Design
Select this option to generate a new memory controller. Generating a memory controller will create RTL, design constraints (UCF), implementation and simulation files.
Xilinx Reference Boards
Select this option for information on specific designs for Xilinx reference boards.
Update Design and UCF
Select this option to update an existing design to the design provided by this version of MIG. You will need to select the project file in the next screen. Refer to the User Guide for more information.
Component Name
Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example_design","user_design" and "docs". The user_design will contain the generated memory interface. The example_design adds a simple example application connected to the generated memory interface.
Component Name
mt_lpddr
User Guide
MCB User Guide
Version Info
< Back
Next >
Cancel


Enable AXI interface for All MCBs
Bank 0
Memory Type
LPDDR
(C3)
Mid
MCB
Bank 3
xc6slx9-csg324
Bank 1
(C1)
Mid
MCB
Memory Type
none
Bank 2

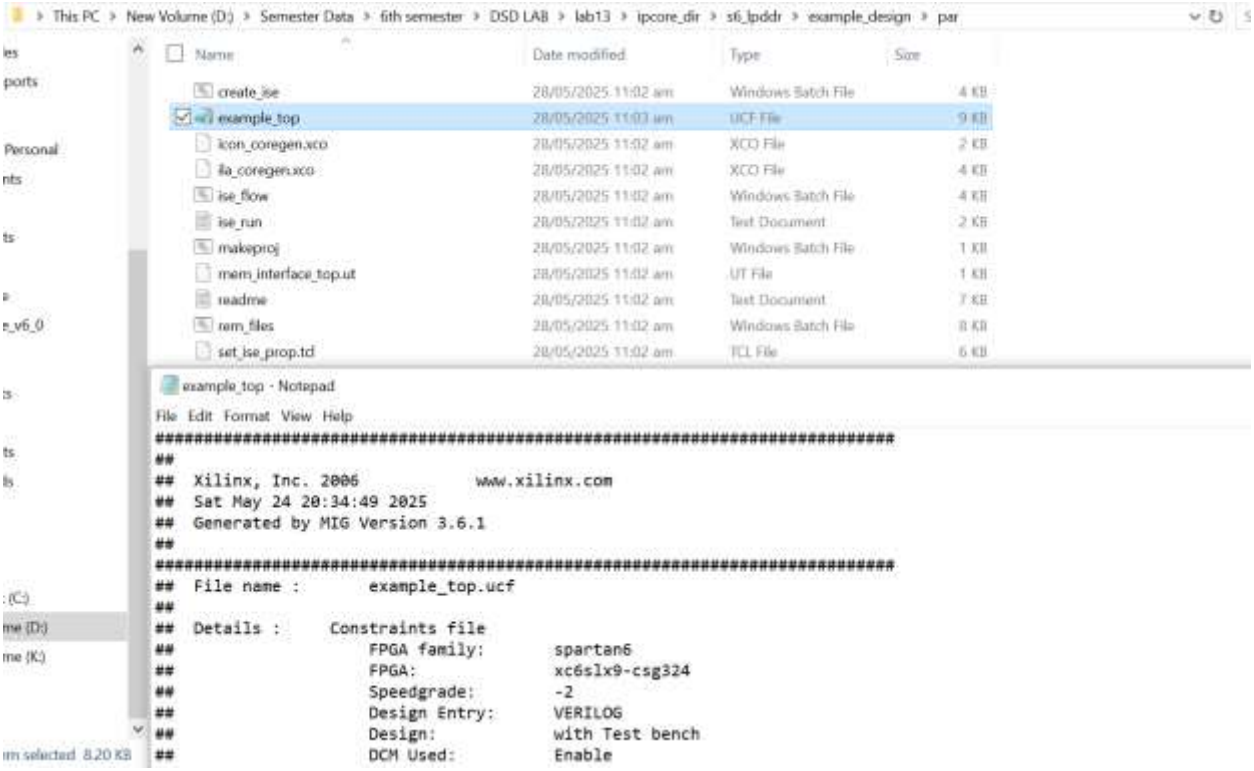

Options for C3 - LPDDR
Frequency: The allowed frequency range is a function of the selected FPGA part, FPGA speed grade and Memory Controller type. Choose the clock period for the desired frequency. Refer to User Guide for supported frequency range.
10000
ps
100.00 MHz
Memory Part: Select the memory part. Parts marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part you want is not listed here.
MT46H32M16XXXX-5
Create Custom Part


Xilinx Memory Interface Generator
REFERENCE DESIGN
Controller Options
C3
Memory Options
C3
Multi-port Configuration
C3
AXI Parameter
C3
Arbitration
C3
FPGA Options
C3
Summary
Memory Model
PCB Information
Design Notes
Port Configuration for C3 - LPDDR
Select one of five configurations from the configuration menu and the ports from the table. As you select the port configuration, the below figure and table will get updated. You can select the number of ports in a configuration, and data port settings from the table.
Configuration Selection
Two 32-bit bi-directional and four 32-bit unidirectional ports
Port Selection
Interface
Direction
Port0
NATIVE
Bi-directional
Port1
NATIVE
none
Port2
NATIVE
none
Port3
NATIVE
none
Port4
NATIVE
none
Port5
NATIVE
none
Memory Address Mapping Selection
User Address
ROW
BANK
COLUMN
BANK
ROW
COLUMN
XILINX
User Guide
PCB User Guide
Version Info
< Back
Next>
Cancel

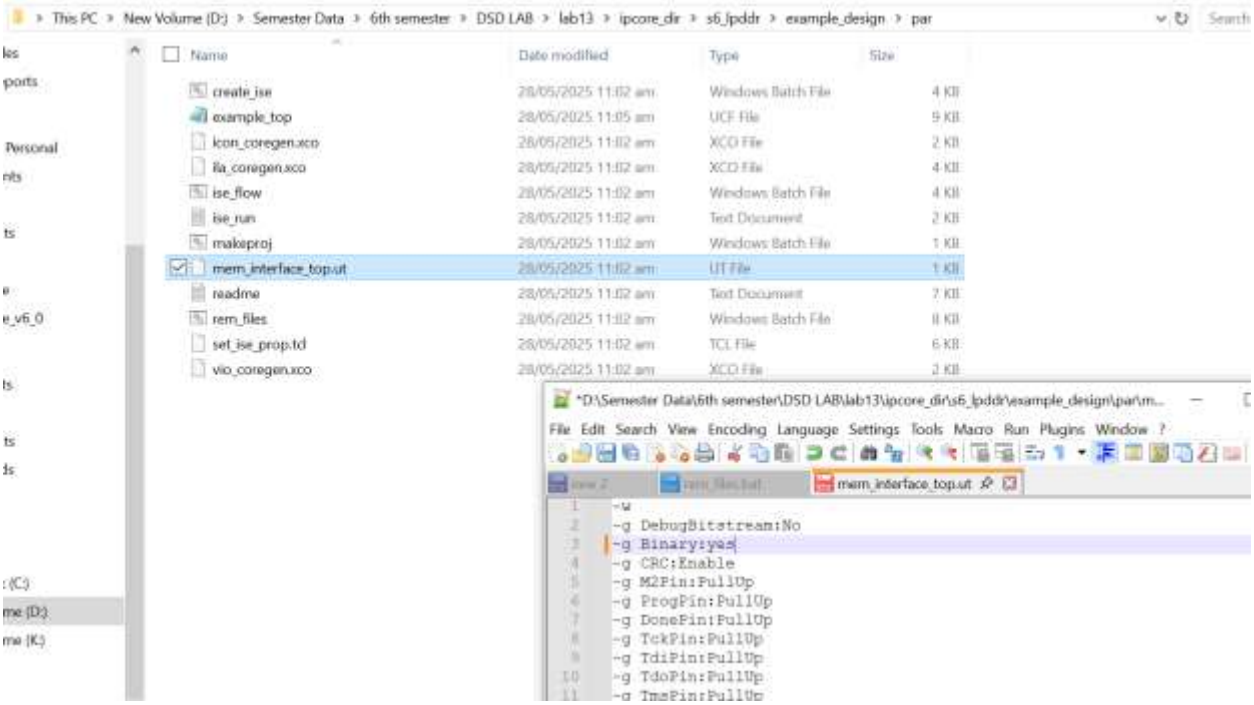

FPGA Options for C3 - LPDDR
LPDDR Termination support
Terminations are not typically required for LPDDR interfaces as long as the PCB guidelines in the Spartan-6 FPGA Memory Controller User Guide (UG388) are followed. Any external terminations added at the user's discretion should be validated with IBIS simulation.
Select RZQ pin location: This pin is required for all MCB designs. If Calibrated Input Termination is used, this pin must have a resistor of value 2R to ground, where R is the desired input termination value. Otherwise, it may be left as a no-connect (NC).
N4
Debug Signals for Memory Controller: This allows the debug signals to be monitored on the ChipScope tool. Selecting this option will port map the debug signals to the ChipScope modules in the design top module. Debug is supported only for one controller.
Disable
System Clock
System Clock: Choose the desired input clock configuration.
Single-Ended


s not convey to you an interest in or to the Model, but only a limited right to
nt.
WARRANTY OF ANY KIND. MTI EXPRESSLY DISCLAIMS ALL WARRANTIES
ENT OF THIRD PARTY RIGHTS, AND ANY IMPLIED WARRANTIES OF
ES NOT WARRANT THAT THE MODEL WILL MEET YOUR REQUIREMENTS, OR
OR-FREE. FURTHERMORE, MTI DOES NOT MAKE ANY REPRESENTATIONS
RMS OF ITS CORRECTNESS, ACCURACY, RELIABILITY, OR OTHERWISE. THE
MAINS WITH YOU. IN NO EVENT SHALL MTI, ITS AFFILIATED COMPANIES OR
Print
lation directory. By clicking Decline, you will need to acquire and configure a
Accept
Decline
< Back
Next>
Cancel

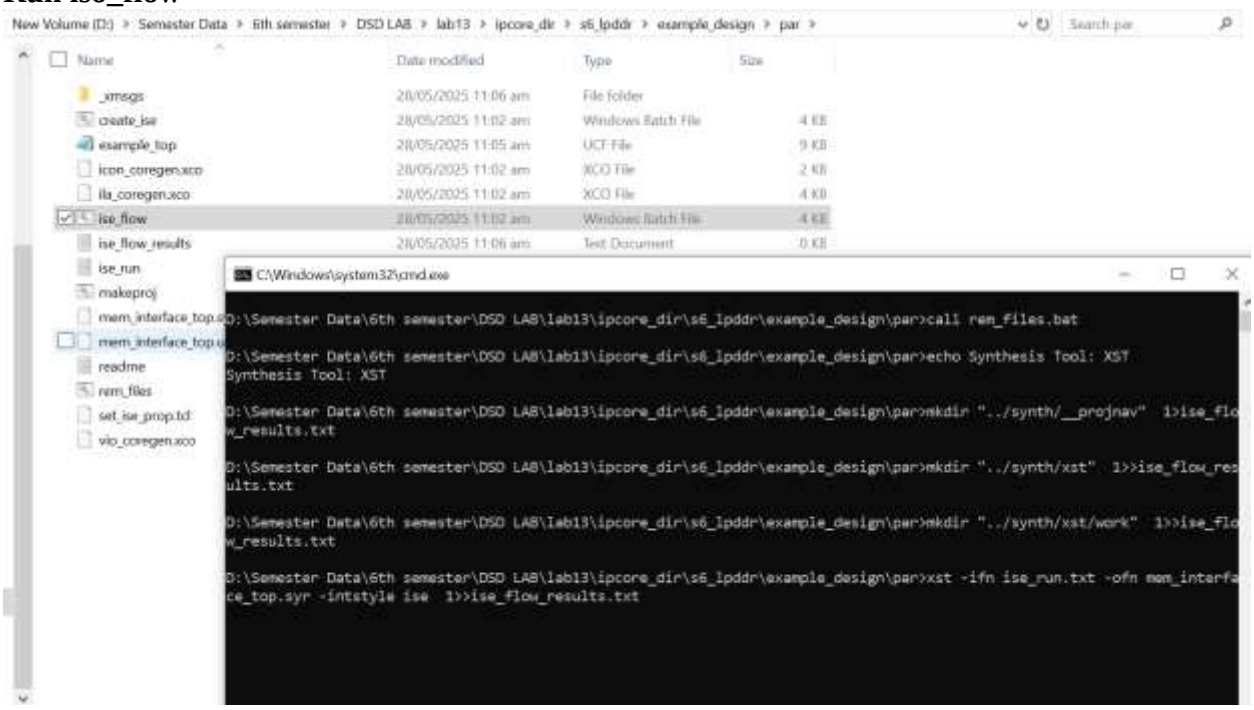
Change example_top

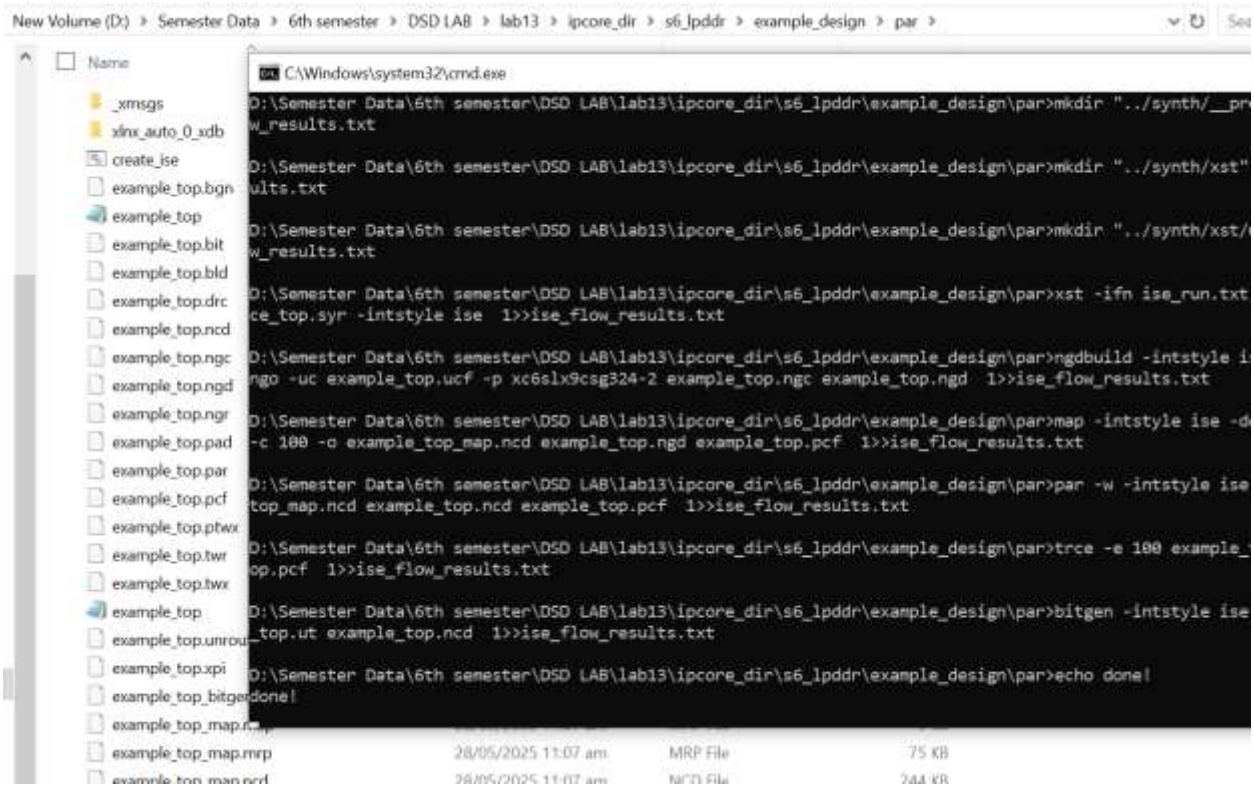


Change mem_interface_top.ut



Run iso_flow


New Volume (D:) > Semester Data > 6th semester > DSD LAB > lab13 > ipcore_dir > s6_lpddr > example_design > par >
Name
Date modified
Type
Size
_xmsgs
create_ise
example_top
icon_coregen.xco
ila_coregen.xco
ise_flow
ise_flow_results
ise_run
makeproj
mem_interface_top.s
mem_interface_top.u
readme
rem_files
set_ise_prop.tcl
vio_coregen.xco
C:\Windows\system32\cmd.exe
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>call rem_files.bat
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>echo Synthesis Tool: XST
Synthesis Tool: XST
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>mkdir "../synth/__projnav" 1>ise_flo
w_results.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>mkdir "../synth/xst" 1>>ise_flow_res
ults.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>mkdir "../synth/xst/work" 1>>ise_flo
w_results.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>xst -ifn ise_run.txt -ofn mem_interfa
ce_top.syr -intstyle ise 1>>ise_flow_results.txt


New Volume (D:) > Semester Data > 6th semester > DSD LAB > lab13 > ipcore_dir > s6_lpddr > example_design > par >
Name
_xmsgs
xlnx_auto_0_xdb
create_ise
example_top.bgn
example_top
example_top.bit
example_top.bld
example_top.drc
example_top.ncd
example_top.ngc
example_top.ngd
example_top.ngr
example_top.pad
example_top.par
example_top.pcf
example_top.ptwx
example_top.twr
example_top.twx
example_top
example_top.unrou
example_top.xpi
example_top_bitge
example_top_map.n
example_top_map.mrp
example_top_map.ncd
28/05/2025 11:07 am
MRP File
75 KB
C:\Windows\system32\cmd.exe
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>mkdir "../synth/__pr
w_results.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>mkdir "../synth/xst"
ults.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>mkdir "../synth/xst/
w_results.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>xst -ifn ise_run.txt
ce_top.syr -intstyle ise 1>>ise_flow_results.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>ngdbuild -intstyle i
ngo -uc example_top.ucf -p xc6slx9csg324-2 example_top.ngc example_top.ngd 1>>ise_flow_results.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>map -intstyle ise -d
-c 100 -o example_top_map.ncd example_top.ngd example_top.pcf 1>>ise_flow_results.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>par -w -intstyle ise
top_map.ncd example_top.ncd example_top.pcf 1>>ise_flow_results.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>trce -e 100 example_
op.pcf 1>>ise_flow_results.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>bitgen -intstyle ise
_top.ut example_top.ncd 1>>ise_flow_results.txt
D:\Semester Data\6th semester\DSD LAB\lab13\ipcore_dir\s6_lpddr\example_design\par>echo done!
done!

Output: