

## **Lab 05**

### **BCD to Seven Segment Decoder**



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Class Section: **A**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

A handwritten signature in black ink, reading "Mohsin Sajjad".

Student Signature: \_\_\_\_\_

Submitted to:

**Engr. Faheem Jan**

Month Day, Year (23 03, 2025)

Department of Computer Systems Engineering  
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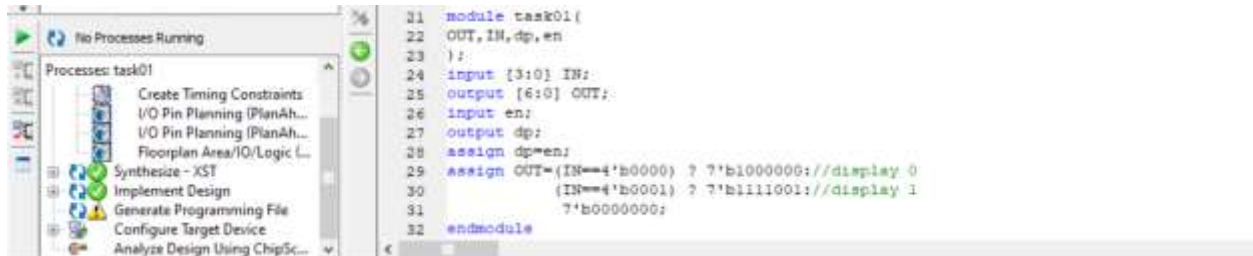
## **Objective:**

To implement a BCD to Seven Segment Decoder on Spartan 6 board.

## **Lab Task:**

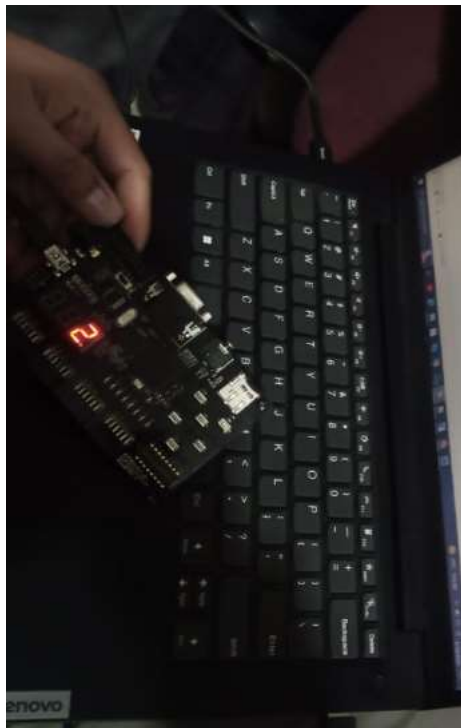
- 1- Using switches enter a BCD number and show the resulting number on the seven segment display.

## **CODE:**



```
31 module task01(  
32 OUT, IN, dp, en  
33 ):  
34 input [3:0] IN;  
35 output [6:0] OUT;  
36 input en;  
37 output dp;  
38 assign dp=en;  
39 assign OUT=(IN==4'b0000) ? 7'b1000000://display 0  
40             (IN==4'b0001) ? 7'b1111001://display 1  
41             7'b0000000;  
42 endmodule
```

## **OUTPUT:**



## **Conclusion:**

This Verilog module takes a 4-bit binary input (IN) and displays the corresponding decimal number on a seven-segment display. It currently supports only 0 and 1, with other values turning the display off (7'b0000000). The dp (decimal point) is controlled by the en signal.

## **TASK 02:**

Connect the output of your lab 02 (4 bit adder) to the seven segment display. Note that number above 1001 are not valid BCD numbers. In this situation keep the seven segment display off and just the dp on.

ISE Project Navigator (P.20131013) - D:\Semester Data\6th semester\DS LAB\lab03\lab05\lab05.xise - [task01.v]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Hierarchy

- lab05
  - xc6slx9-2csg324
    - task2 (task01.v)
      - BCDA.ucf

No Processes Running

Processes: task2

- Create Timing Constraints
- I/O Pin Planning (PlanAh...
- I/O Pin Planning (PlanAh...
- Floorplan Area/IQ/Logic L...
- Synthesize - XST
- Implement Design
- Generate Programming File
- Configure Target Device

```

18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21 module task2 (OUT,A,B,dp,en):
22   input [3:0] A;
23   input [3:0] B;
24   output [6:0] OUT;
25   wire [3:0] SUM;
26   input en;
27   output dp;
28   assign SUM=A+B;
29   assign dp=en;
30   assign OUT=(SUM==4'b0000) ? 7'b1000000:
31               (SUM==4'b0001) ? 7'b1111001:
32               (SUM==4'b0010) ? 7'b0100100:
33               (SUM==4'b0011) ? 7'b0110000:
34               (SUM==4'b0100) ? 7'b0011001:
35               (SUM==4'b0101) ? 7'b0010010:
36               (SUM==4'b0110) ? 7'b0000010:
37               (SUM==4'b0111) ? 7'b1110010:
38               (SUM==4'b1000) ? 7'b0000000:
39               (SUM==4'b1001) ? 7'b0010000:
40               7'b1111111;
41 endmodule
42

```

OUTPUT:





## Conclusion:

This Verilog module adds two 4-bit binary numbers ( $A$  and  $B$ ) and displays the result on a seven-segment display. The output ( $OUT$ ) lights up the correct segments to show the sum in decimal (0-9). The  $dp$  (decimal point) is controlled by the  $en$  signal, but it isn't essential for basic operation. If the sum exceeds 9, the display shows all segments off (7'b1111111).