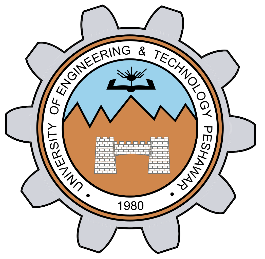
**Lab 07**

**Implementation of a 3 bit up and down counter using FPGA’s source clock and Clock Divider**



**Spring 2025**

Submitted by: **Mohsin Sajjad**

Registration No: **22pwsce2149**

Class Section: **A**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”



Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

**Engr. Faheem Jan**

Month Day, Year (20 04, 2025)

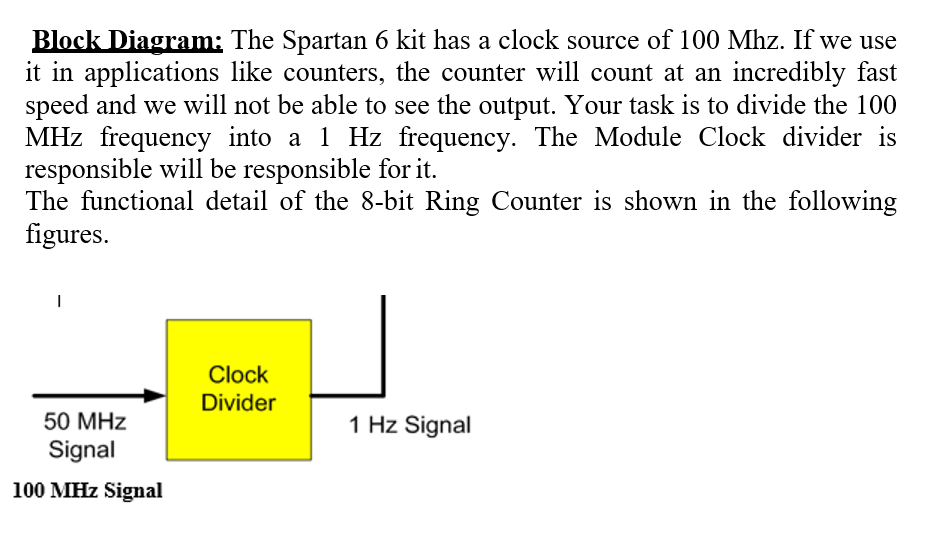
Department of Computer Systems Engineering

University of Engineering and Technology, Peshawar

**Implementation of a 3 bit up and down counter using FPGA’s source clock and Clock Divider**

**Objective:**

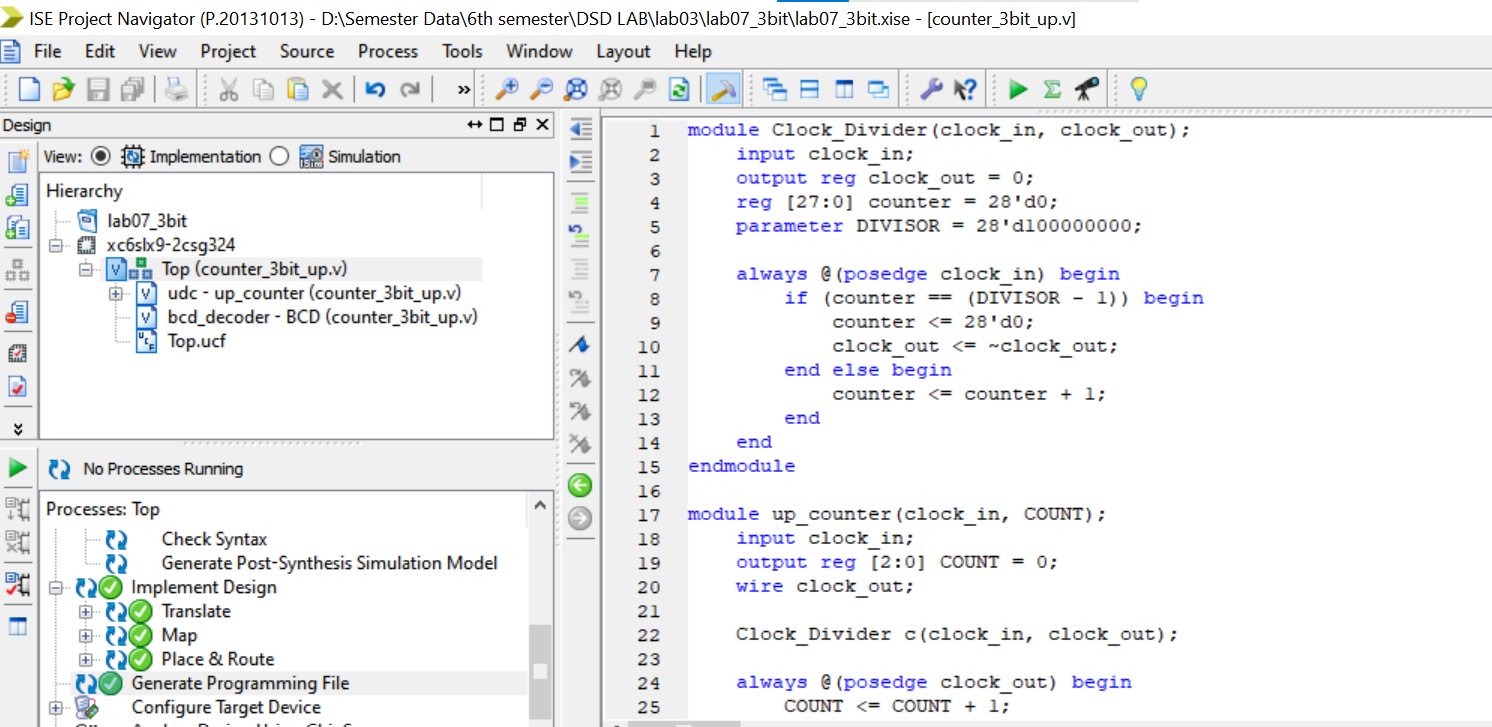
* To become familiarized with behavior level modeling
* To be able to implement sequential circuits using Verilog
* To Implement an 8 Bit Ring Counter on Spartan 6 FPGA starter kit.

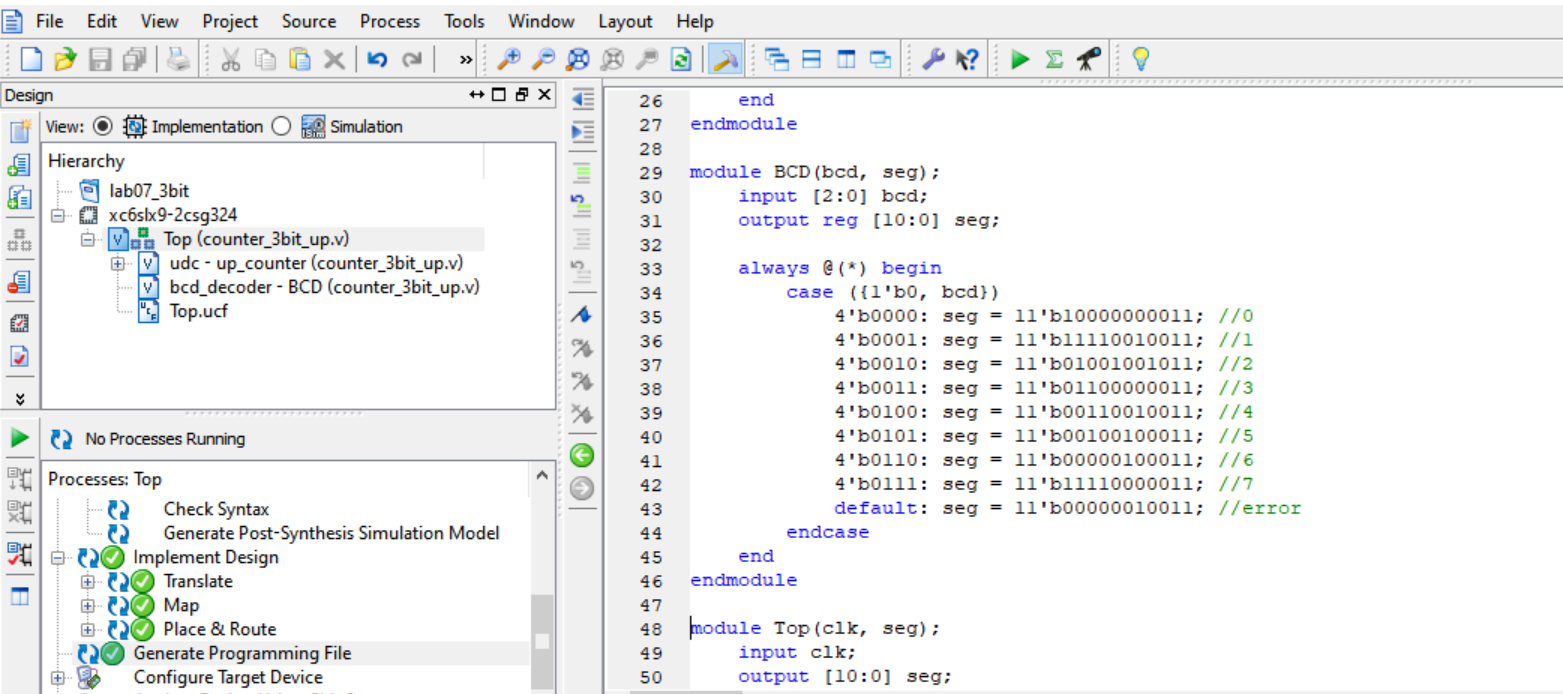
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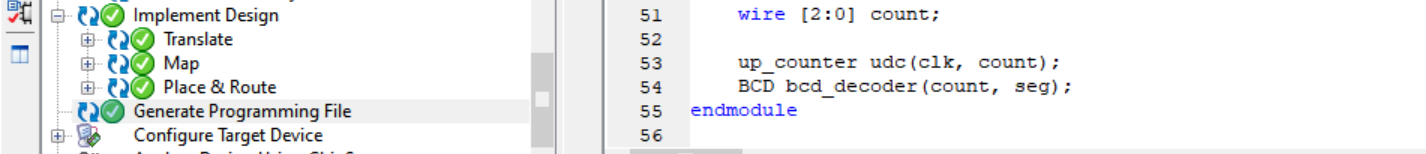
**Lab Task:**

1-Implement 3 bit Up Counter using FPGA’s clock source and clock divider

**CODE:**

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**OUTPUT:**

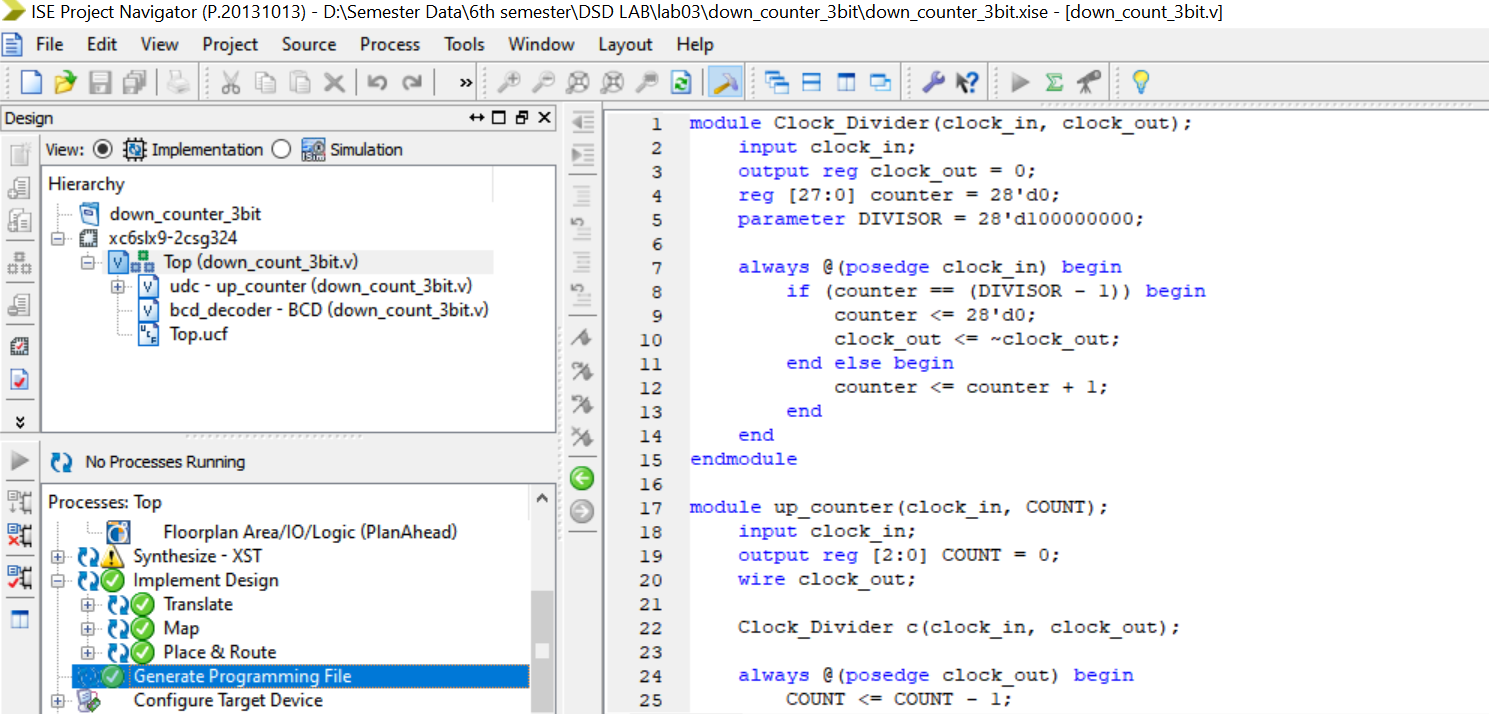
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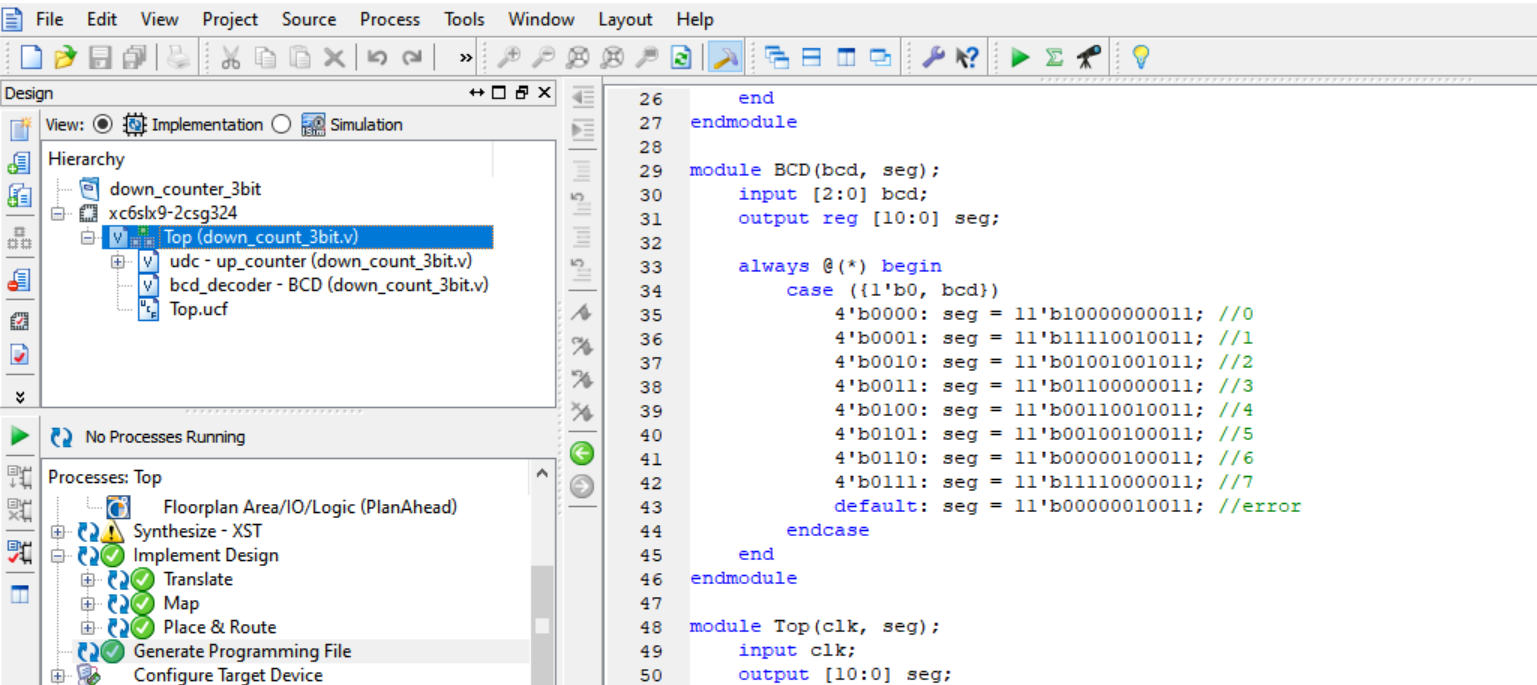
**Conclusion:**

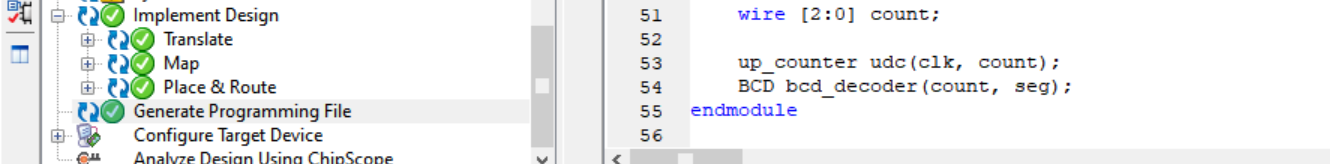
This Verilog code implements a simple digital system that counts from 0 to 7 using a clock divider and displays the count on a 7-segment display. The Clock\_Divider module reduces the input clock frequency, the up\_counter module increments the 3-bit count, and the BCD module decodes this count to drive the display. The Top module connects all components together.

**TASK 02:**

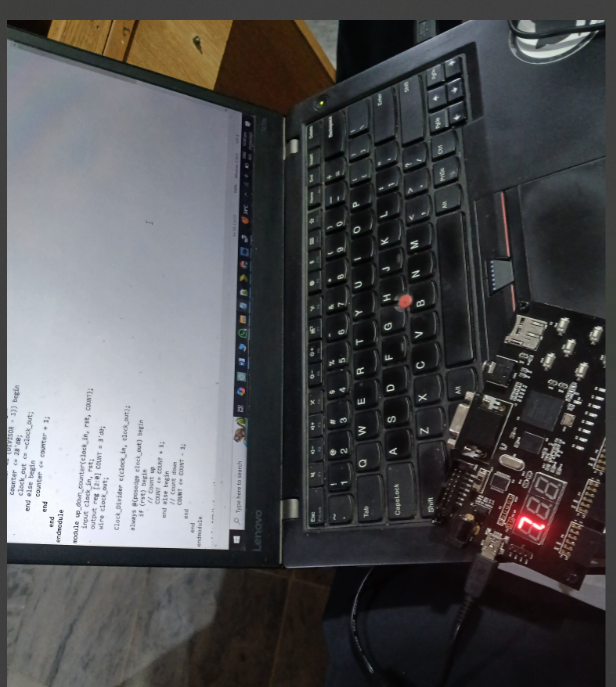
Implement 3-bit Down Counter using FPGA’s clock source and clock divider  
**CODE:**







**OUTPUT:**

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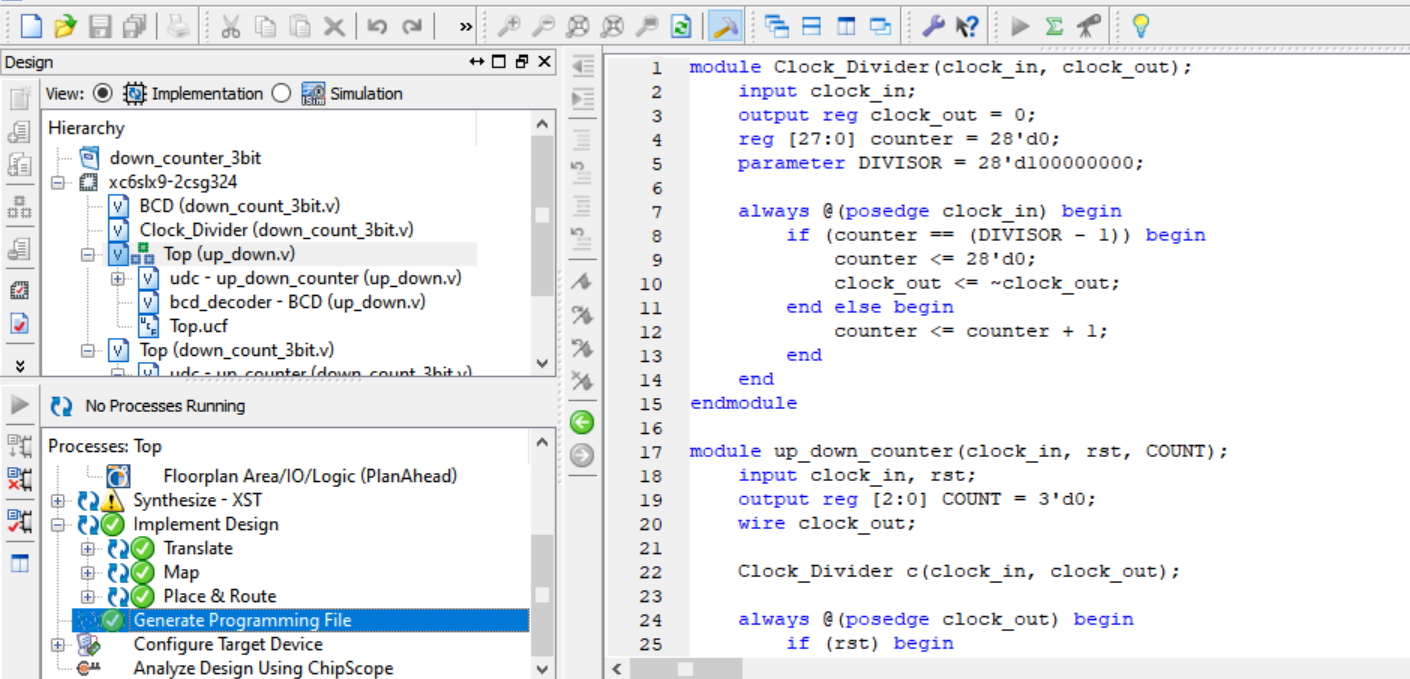
**Conclusion:**

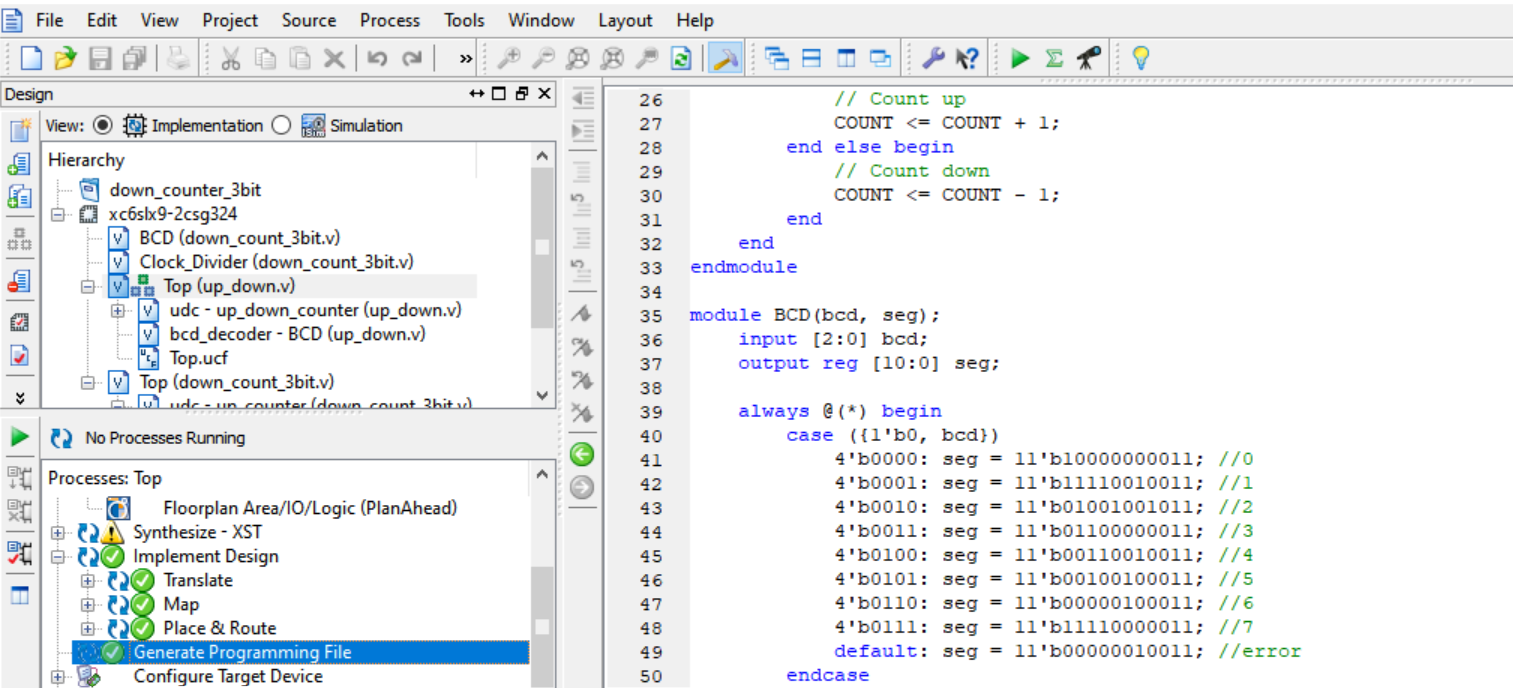
This updated Verilog design implements a **down counter** that counts from 7 to 0 repeatedly. It uses a Clock\_Divider to slow the input clock, an up\_counter module (actually counting down), and a BCD module to display the count on a 7-segment display. The Top module integrates all components into one system.

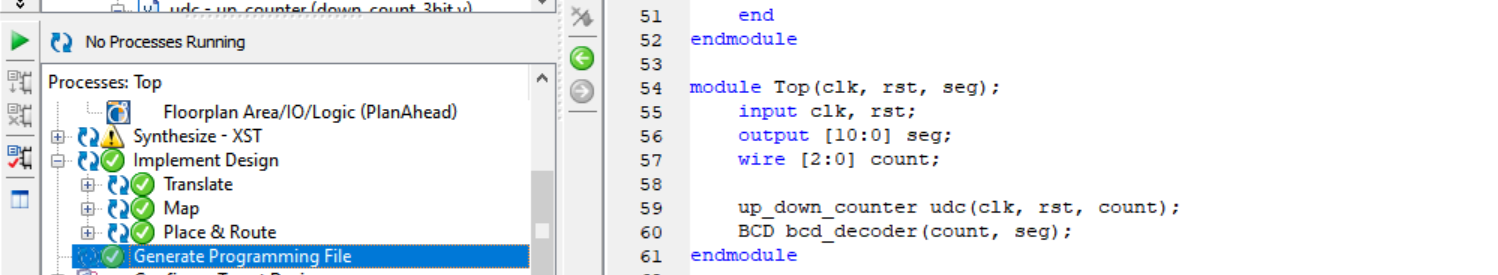
**TASK 03:**

Implement 3-bit Up and Down Counter using RST if the RST is high it should Count Up if it is low it should Count Down and display the count in the seven segment display.

**CODE:**

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**Output:**

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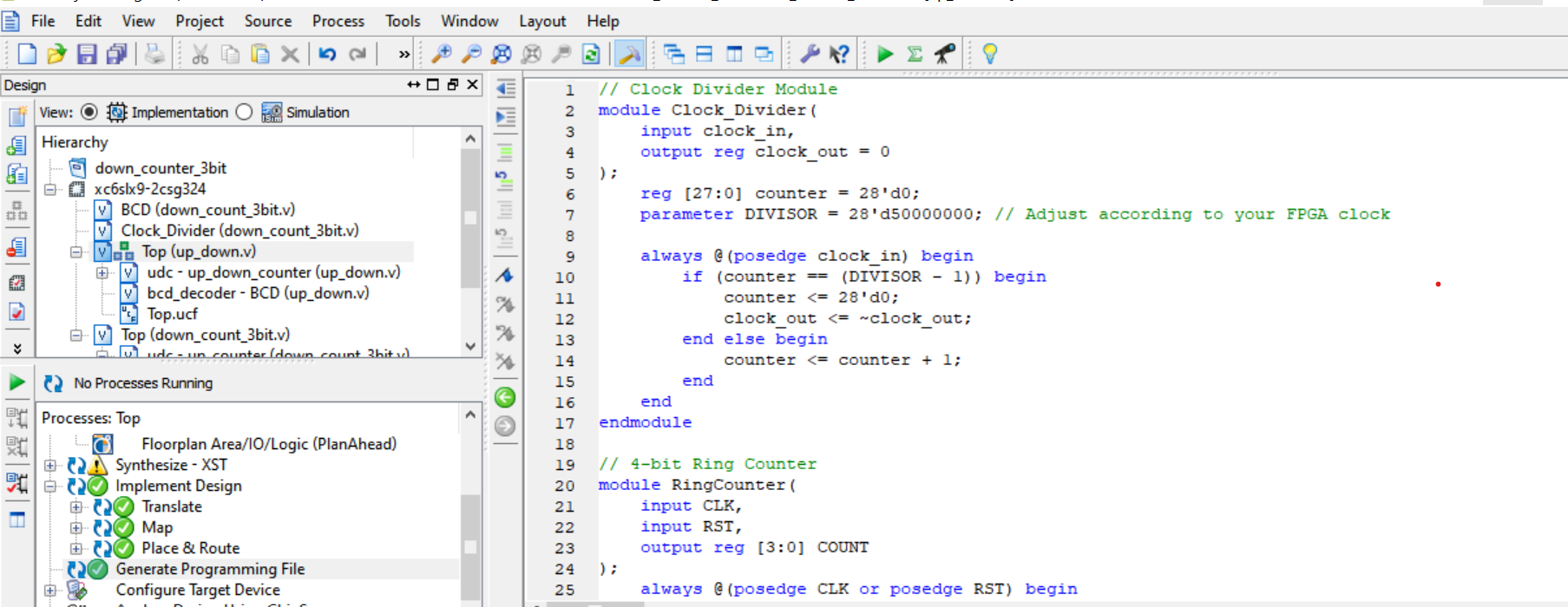
**Conclusion:**

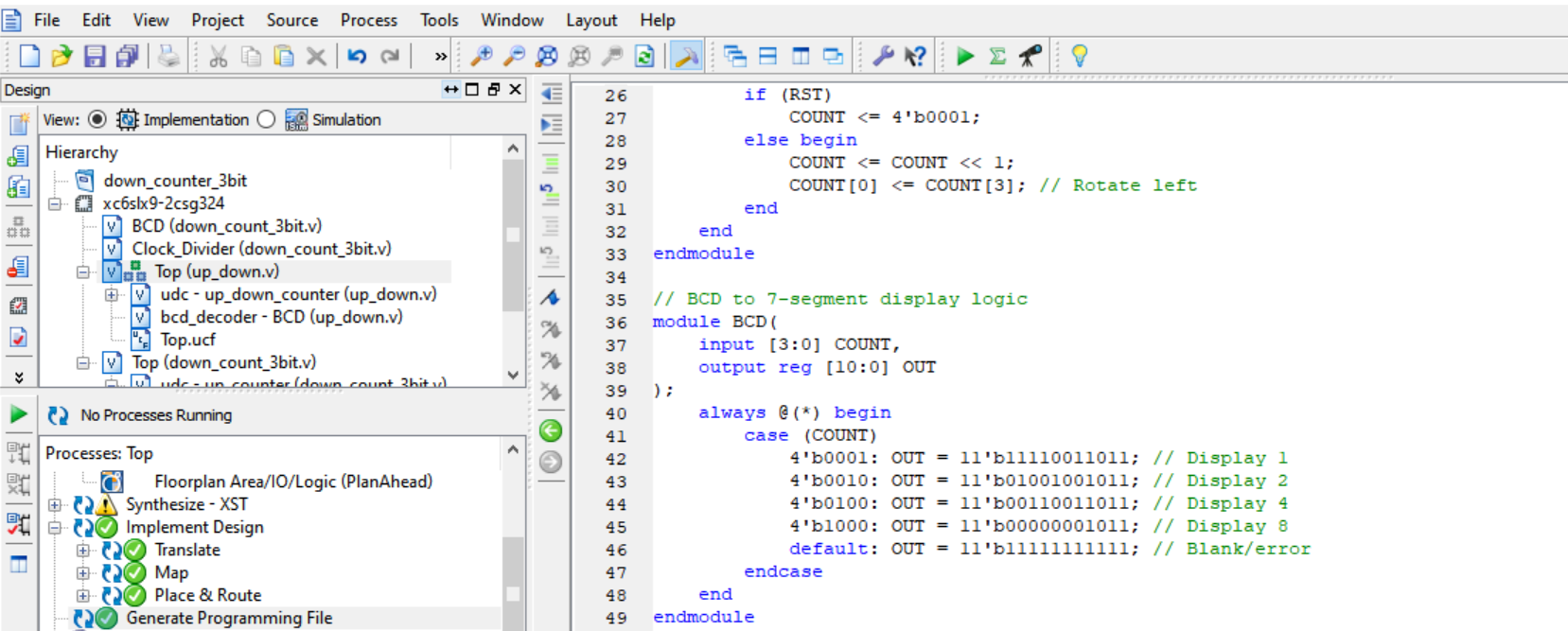
This Verilog code implements a 3-bit **up/down counter system** with display. A Clock\_Divider slows the clock signal, and the up\_down\_counter counts **up when rst is high** and **down when rst is low**. The BCD module decodes the count to a 7-segment format. The Top module integrates all components, making the count direction controllable by the rst input.

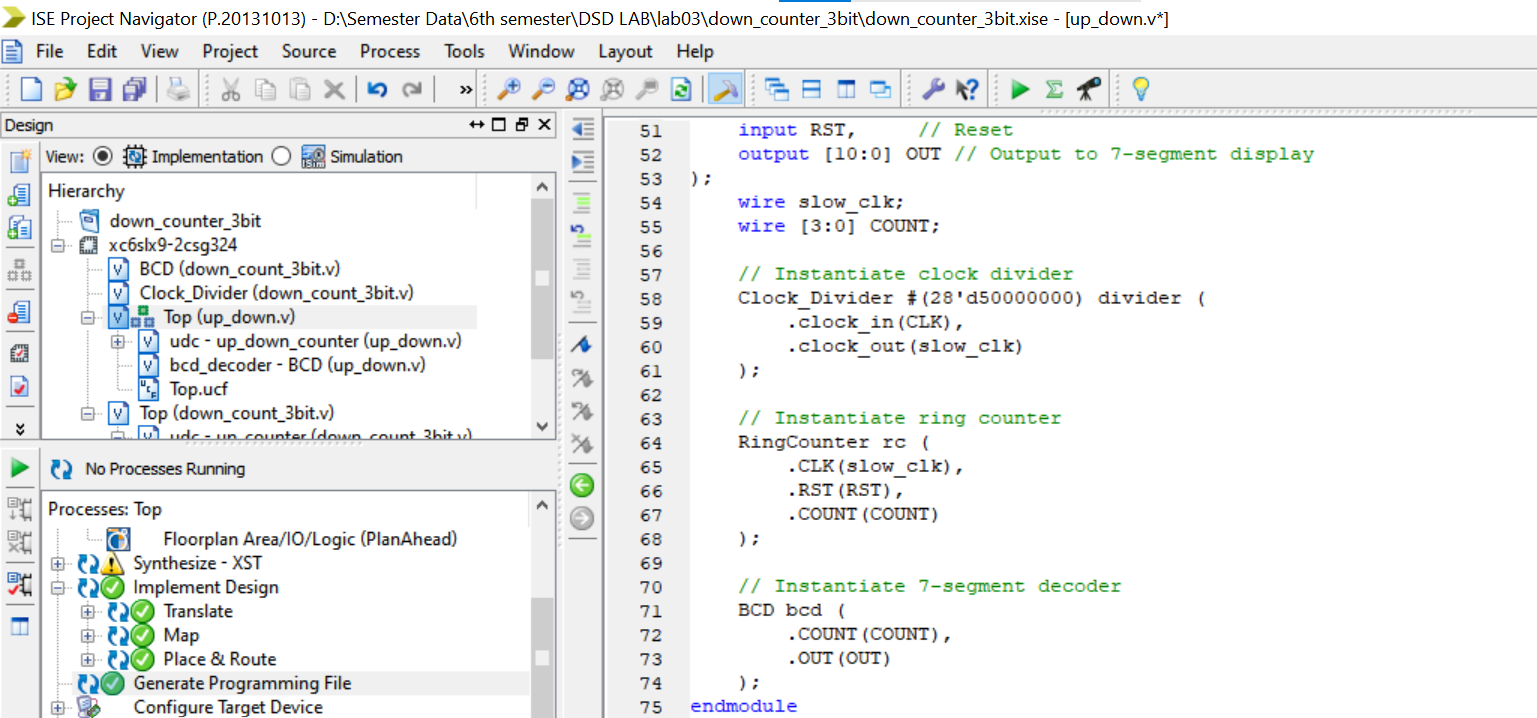
**Task 04:**

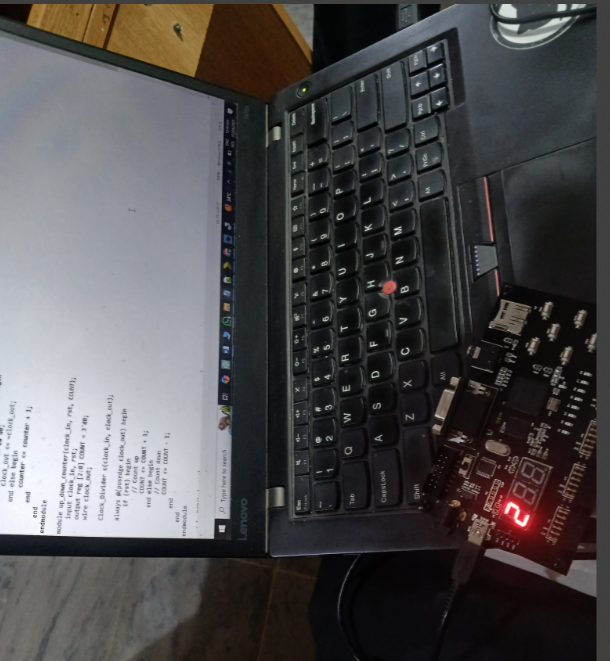
Implement Lab 6 using FPGA’s clock source.

**CODE:**

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**Output:  
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**Conclusion:**

This Verilog design creates a **4-bit ring counter system** using a Clock\_Divider to slow down the input clock, a RingCounter that shifts a single high bit through 4 positions (rotating left), and a BCD module that converts the counter output into a 7-segment display pattern. The Top module ties everything together, and the count resets to 0001 when RST is high.