



Department of Computer Systems Engineering
University of Engineering & Technology Peshawar
6th Semester Final-term Examination, Spring 2024

Course Title: Technical Writing

Course Code: CSE311

Total Marks: 50

Maximum Weightage: 50%

Time allowed: 02 Hours

Name: Umer Hayat

Reg #: _____

- Attempt all five questions; the marks for each part of the question are written there in parenthesis.
- Do not write anything on this question paper except your name and registration number.
- Electronic gadgets are strictly prohibited.

✓ Q1 – What is a skill (2)? Is interviewing a skill (1)? If yes, how can you improve it (1)? Pick a job/title of your choice in an organization of your choice. What are the skills and competencies that make you best fit for this job (3)? What is the STAR method used for improving interviewing skills (3)?

Affective-2 (Responding)

✓ Q2 – What is plagiarism (2)? Why do people plagiarize (2)? In your candid opinion, how can Generative AI tools be used in an ethical and responsible manner (3)? With respect to the Generative AI tools, devise a process for encouraging creativity and critical thinking (3).

✓ Q3 – What is Latex and why do the people in scientific community usually prefer it over MS Word (2)? Why do we read research papers (2)? Where can we find relevant and quality research papers (2)? What are the ingredients of a quality research paper (4)?

Affective-3 (Valuing)

✓ Q4 – Write guidelines for writing a good quality

- a) Title (2)
- b) Abstract (2)
- c) Introduction (3)
- d) Literature Review (3)

✓ Q5 – What are the essential ingredients of a good proposal? Explain/Justify with the help of your own FYP proposal that you wrote as an assignment for this course. (10)

Affective-4 (Organization)



Department of Computer Systems Engineering
University of Engineering & Technology Peshawar
6th Semester Mid-term Examination, spring 2024

Course Title: Technical Writing

Course Code: CSE311

Total Marks: 30

Maximum Weightage: 30%

Time allowed: 02 Hours

Name: _____

Reg #: _____

- Attempt all three questions on the answer sheet provided separately.
- Do not write anything on this question paper except your name and registration number.
- Electronic gadgets are strictly prohibited.

Q1 –

CLO1: Affective-2 (Responding)

(10)

Computer Society UET Peshawar is planning to organize a technical event named IGNITE'24 in May this year. You have been tasked by the president to make liaison with other universities for promoting the same. Write an effective letter to the relevant authorities of the targeted universities to seek their permission for promoting the event at their premises.

Q2 –

CLO1: Affective-2 (Responding)

(5+5)

You are applying for an open position titled "Assistant Manager – Technical" in a reputed multinational company that is well known for manufacturing Quantum Computers.

Resume = Spec
Pas

- a. Prepare your CV/Resume to pen your own picture for the same (don't copy paste).
- b. Besides your CV/Resume, what other letter would you submit to show your motivation for the job? What would you write in that letter?

CV –

CV = overa
acade
Infor

Q3 –

What type of a document is the following? Point out and correct the mistakes (if any) in the document given below. You don't need to reproduce the entire document.

(2+8)

Dear Secretary,

ABC is the outstanding engineer, with multidisciplinary work experience. Her achievement in academic as well as professional carrier make him highly suitable for study a Master of Science leading to PhD at the University of XYZ. She exhibit entrepreneurship behavior in his activity. She lead, inventive initiatives and believes strongly in bringing a positive changes to sociology through effective technology policies. She has represent the country at national and international forum? I have found her English proficiencies none less than a native speaker. Her excellent skill of writing grant proposals and devising strategies has helped us win generous grants at local and international levels at the University. Her interest in integrating academia in the policy realm have led her initiate University agreements with policy think tanks. I strongly recommended her for MSc leading to PhD in Science & Technology Policy at XYZ University, as she was academically and professionally capable to undertake the course, rather she will surpassing a lot of other students.

Letter
of
Recom
datio

Feel free to contact if any further info was required about her.

1

To, HR Manager



Department of Computer Systems Engineering,
University of Engineering and Technology, Peshawar,
Pakistan

Midterm Exam (Spring 2024)

Time: 1 Hour 40 Minutes (Part B)

Paper: CSE-403 Database Management System
Marks: 70

Note: Write short and precise answers.

QII: Draw an E-R Diagram for each of the following scenario. Ensure that all entities, attributes, relationships, degree of relationships, types of relationship, cardinalities, constraints e.g., completeness/disjointness (where applicable) and the given business rules are correctly depicted with appropriate notations in the ERD. If you believe that you need to make additional assumptions, clearly state them for each situation. (Marks: 70, CLO2)

- a) For keeping track of the exploits of your favorite sports team. You should store the matches played, the scores in each match, the players in each match and individual player statistics for each match. Summary statistics should be modeled as derived attributes.
- b) A car-insurance company whose customers own one or more cars each. Each car has associated with it zero to any number of recorded accidents.
- c) A hospital with a set of patients and a set of medical doctors. Associate with each patient a log of the various tests and examinations conducted.
- d) For a university registrar's office which maintains data about the following entities: (1) courses, including number, title, credits, syllabus, and prerequisites; (2) course offerings, including course number, year, semester, section number, instructor(s), timings, and classroom; (3) students, including student-id, name, and program; and (4) instructors, including identification number, name, department, and title. Further, the enrollment of students in courses and grades awarded to students in each course they are enrolled for must be appropriately modeled.
- e) UPS prides itself on having up-to-date information on the processing and current location of each shipped item. To do this, UPS relies on a company-wide information system. Shipped items can be characterized by item number (unique), weight, dimensions, insurance amount, destination, and final delivery date. Shipped items are received into the UPS system at a single retail center. Retail centers are characterized by their type, uniqueID, and address. Shipped items make their way to their destination via one or more standard UPS transportation events (i.e., flights, truck

deliveries). These transportation events are characterized by a unique scheduleNumber, a type (e.g., flight, truck), and a deliveryRoute.

- D) A manufacturing company has several assembly plants in different cities. Each plant produces one product which requires certain parts in its assembly. The parts are from appropriate suppliers, located in different cities. Obtained in bulk amounts, certain parts may be used in more than one product.

- g) There are three types of persons: employees, alumni, and students. A person can belong to one, two, or all three of these types. Each person has a name, SSN, sex, address, and birth date. Every employee has a salary, and there are three types of employees: faculty, staff, and student assistants. Each employee belongs to exactly one of these types. For each alumnus, a record of the degree or degrees that he or she earned at the university is kept, including the name of the degree, the year granted, and the major department. Each student has a major department. Each faculty has a rank, whereas each staff member has a staff position. Student assistants are classified further as either research assistants or teaching assistants, and the percent of time that they work is recorded in the database. Research assistants have their research project stored, whereas teaching assistants have the current course they work on.
- Students are further classified as either graduate or undergraduate, with the specific attributes degree program (M.S., Ph.D., M.B.A., and so on) for graduate students and class (freshman, sophomore, and so on) for undergraduates.

*Name: Umer Hayat Khan
*Registration: 21puces 1976

**Department of Computer Systems Engineering
University of Engineering & Technology Peshawar**

**Digital System Design
CSE 308**

**Midterm Examination Spring 2024
4 April 2024, Duration: 120 Minutes**

****Exam Rules****

Please read carefully before proceeding.

1- This exam is closed books/notes/Internet.

2- Answer all problems on the answer sheet.

3- Problems will not be interpreted during the exam.

Good Luck!

Problem 1. (25 pts.)

Below is a dataflow description for a circuit.

```
module DATAFLOW_CIRCUIT (a, b, c, en, d);

    input a, b, c, en;
    output [0:7] d;

    wire na, nb, nc;

    assign na = !a;
    assign nb = !b;
    assign nc = !c;
    assign d[0] = na && nb && nc && en;
    assign d[1] = na && nb && c && en;
    assign d[2] = na && b && nc && en;
    assign d[3] = na && b && c && en;
    assign d[4] = a && nb && nc && en;
    assign d[5] = a && nb && c && en;
    assign d[6] = a && b && nc && en;
    assign d[7] = a && b && c && en;

endmodule
```

(a) (3 pts., CLO-1)

Give a Verilog statement that instantiates the above DATAFLOW_CIRCUIT, with the instance name MID. When you instantiate the circuit, use the same names for wires as is used in the module port list.

DATAFLOW-CIRCUIT MID (a,b,c,en,d)

(b) (6 pts., CLO-1)

Rewrite the DATAFLOW_CIRCUIT using Verilog built-in primitives and structural Verilog. Part of the module is done for you.

```
module STRUCT_CIRCUIT (a, b, c, en, d);

    input a, b, c, en;
    output [0:7] d;
    //Write your code here

endmodule
```

(c) (3 pts., CLO-1)

Draw a gate-level circuit for your module in (b). Label all nets on the circuit.

(d) (6 pts., CLO-1)

Rewrite the DATAFLOW_CIRCUIT using behavioral Verilog. Part of the module is done for you.

```

module BEHAV_CIRCUIT (a, b, c, en, d);
    input a, b, c, en;
    output [0:7] d;
    //Write your code here

endmodule

```

(e) (7 pts., CLO-1)

Write the output of DATAFLOW_CIRCUIT for the following test bench.

```

//Test Bench for DATAFLOW_CIRCUIT
module TB_DATAFLOW_CIRCUIT;

reg a, b, c, en;
wire [0:7] d;
DATAFLOW_CIRCUIT DF (a, b, c, en, d);

initial
begin
    a = 1; b = 1; c = 1; en = 0;
    #5 a = 0; b = 1; c = 1; en = 1;
    #5 a = 1; b = 0; c = 1; en = 1;
    #5 a = 0; b = 1; c = 0; en = 1;
    #5 a = 1; b = 1; c = 0; en = 0;
    #5 a = 0; b = 0; c = 1; en = 1;
    #5 a = 0; b = 0; c = 0; en = 1;
end

initial
$monitor ($time, " OUT = %b", d);

endmodule

```

0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

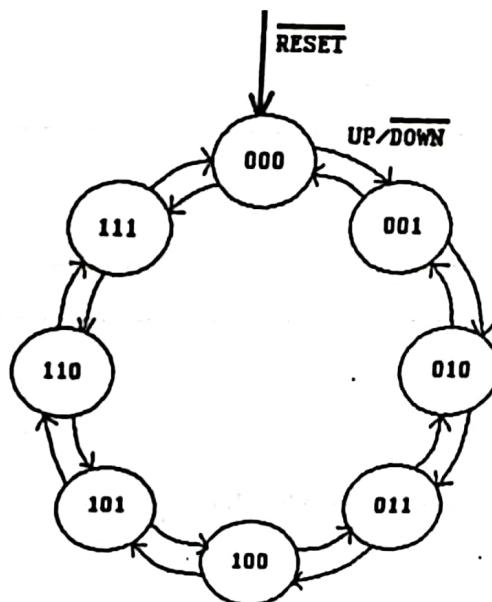
Problem 2. (40 pts.)

This problem involves creating several Verilog designs. Three lower-level modules are written and then two of these are combined to create a top-level design.

For each module, write a complete Verilog description with correct declaration, etc. A completely correct solution will receive the number of points indicated in parentheses. Partially correct solutions will receive partial credit.

(a) Module 1: 3-bit Up/Down Counter. (10 pts., CLO-2)

In this module, design a 3-bit up/down counter, a counter that counts in both up and down directions. The state transition diagram is shown in Figure 1.

**Figure 1.** The state transition diagram of the 3-bit up/down counter

The following are the ports of the module:

CLK	1-bit clock input, all actions must be on the rising edge
RESET	1-bit reset input, causes reset on the rising edge
UP_DN	1-bit input (if 1, then count up, if 0, then count down)
COUNT	3-bit output

The skeleton file for the counter has been written below.

```

module COUNTER (CLK, RESET, UP_DN, COUNT);
    //Write your code here
endmodule
  
```

(b) Module 2: 8-to-1 Multiplexer. (10 pts., CLO-1)

In this module, design a byte-wide 8-to-1 multiplexer. In this case, the value on the 3-bit select line will route 1 of 8 inputs to the output. This module is purely combinatorial.

The following are the ports of the module:

SEL	3-bit select line
D0, D1, D2, D3, D4, D5, D6, and D7	8-bit data inputs
OUT	8-bit output

The skeleton file for the multiplexer has been written below.

```
module MUX81 (SEL, D0, D1, D2, D3, D4, D5, D6, D7, OUT);
    //Write your code here

endmodule
```

(c) Module 3: Parallel-in, Serial-out Shift Register. (10 pts., CLO-2)

In this module, create a register that loads data in parallel but shifts data out serially, MSB first.

The following are the ports of the module:

CLK	1-bit clock, all operations must be on the falling edge
PI	8-bit parallel data input
SO	1-bit serial output
LD	1-bit input, when high, PI is loaded into the shift register
SHIFT	1-bit shift enable input, when high, contents of the shift register are shifted out on to the serial output SO

The skeleton file for the register has been written below.

```
module PISO (CLK, PI, SO, LD, SHIFT);
    //Write your code here

endmodule
```

✓(d) Module 4: Top-level Design. (10 pts., CLO-2)

For this design, combine the 3-bit up/down counter (Module 1) with the 8-to-1 multiplexer (Module 2) to create a circuit such that the output of the counter controls the select lines of the multiplexer.

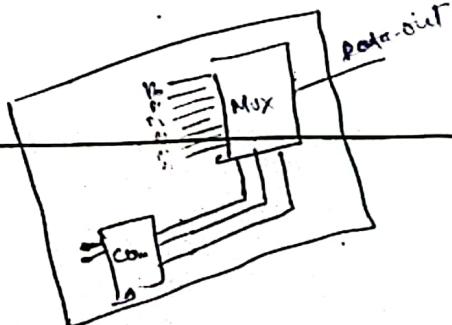
This top-level design has the following port definitions:

CLOCK	1-bit clock
CLR	1-bit reset line
UD	1-bit input (if 1, the counter counts up, if 0, the counter counts down)
I0, I1, I2, I3, I4, I5, I6, and I7	8-bit data inputs
DATA_OUT	8-bit data output

The skeleton file for the top-level design has been written below.

```
module TOP (CLOCK, CLR, UD, I0, I1, I2, I3, I4, I5, I6, I7, DATA_OUT);
    //Write your code here

endmodule
```





Umer Hayat

**Department of Computer Systems Engineering,
University of Engineering and Technology, Peshawar,
Pakistan**

Final Exam (Spring 2024)
Time: 2 Hours (6th Semester)

Note: Attempt all questions on the answer sheet.

Question No. 1

a). Convert the following ERD to relations showing referential integrity constraints.

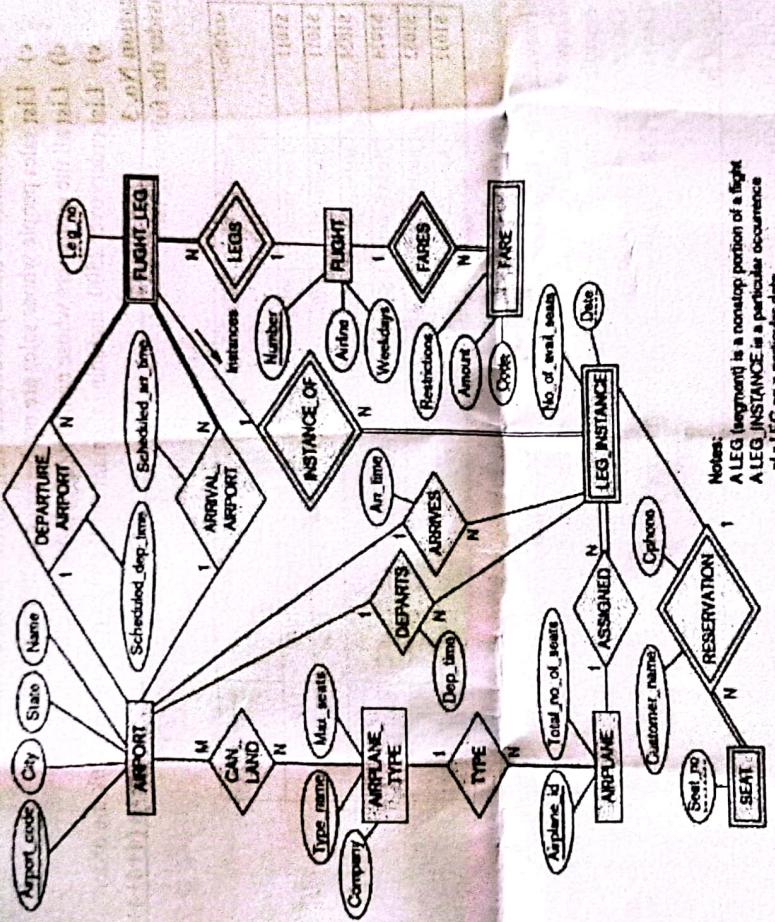


Figure 1: E-R Diagram for an Airline Booking Application

b). Identify the functional and transitive dependencies in the following relation and convert it to 2nd and 3rd Normal form. (Identify/assume appropriate primary/foreign keys)

Product_Sales (Order_ID, Product_ID, Product_Name, Customer_ID)

Customer (Name, Quantity, Price, Total_Amount)

REGISTRATION_CARD (Student-ID, S-Name, HomeAddr, Advisor, Ofc-Phone, Course-ID, Course-Days/Time, Credit-hours, Room/Bldg, Instructor, Email, Phone, RegisDate, TotalFees, FeesPaid)

LIBRARY_CHECKOUT (Checkout_ID, Book_ID, Book_Title, Author, Member_ID, Member_Name, Checkout_Date, Due_Date, Fine_Amount)

Patient_Records (Patient_ID, Patient_Name, Age, Gender, Date_Admitted, Doctor_ID, Doctor_Name, Department, Diagnosis, Medication, Dosage)

Question No. 2

SalesRep (SalRepId, SalesPersonName, OfficelId, ProductId, Qty, Amount, SalRepId, Date)

Consider the following tables:

Order (OrderId, CustomerId, ProductId, Title, Age, HireDate, Manager, Quota, Sales)

Office (OfficelD, City, Region, Target, Sales)

Customer (CustomerId, customerName, Company, CreditLimit, Address, salRepId)

Product (ProductId, Description, Price, Manufacturer, Qty_On_Hand)

Write the SQL statements for the following queries:

- List the name and hire date of anyone with sales over 50000
- List the names of Sales persons and their corresponding Customer names
- List sales people whose sales are not between 50000 to 80000
- List all the customers whose name starts with 'A' or 'a'
- List orders over 2500, including the name of the sales person who took the order

Marks (4+4+4+4+4)

Consider the following table:

VisitNo	dentistName	patientNo	patientName	appointment	surgeryNo
				date	time
S1011	Tony Smith	P100	Gillian White	12-Aug-03	10:00
S1011	Tony Smith	P105	Jill Bell	13-Aug-03	12:00
S1024	Helen Pearson	P108	Ian Mackay	12-Sep-03	10:00
S1024	Helen Pearson	P108	Ian Mackay	14-Sep-03	10:00
S1032	Robin Plevin	P105	Jill Bell	14-Oct-03	16:30
S1032	Robin Plevin	P110	John Walker	15-Oct-03	18:00
					S13

- Provide examples of Insertion, Deletion and Modification anomalies in the table.
- Draw a dependency diagram that shows all functional dependencies in the relation, based on the sample data shown.
- Develop a set of relations in third normal form.
- Develop an E-R diagram with the appropriate cardinality notations.

Question No. 4

(Marks=4+4)

Consider the following table:

Trans_ID	Date	Product_ID	Product_Name	Category	Supplier_ID	Supplier_Name	Quantity_Sold	Unit_Price	Total_Price	Stock_Quantity	Quota	Reorder_Level
1	2024-05-01	101	Laptop	Electroni	501	ABC Electroni	5	1200	6000	10	5	
2	2024-05-02	102	Smartphone	Electroni	502	XYZ Tech	8	800	6400	15	5	
3	2024-05-03	103	Shirt	Apparel	503	Fashion Store	10	300	3000	50	20	

- Diagram the functional dependencies and determine the normal form of the above table.
- Convert the given table to 3rd normal form, and identify referential integrity constraints.

Question No. 5 a). How the three application logics (Presentation, Processing and storage) are distributed in a three-tier architecture?
b). What are the possible threats to Data Security in a Database Environment?



Department of Computer Systems Engineering,
University of Engineering and Technology Peshawar,
Pakistan

Finalterm Exam (6th Semester, Spring 2024)

Paper: MBSD
Marks: 80

Time: 2 Hours

Note: Attempt all questions on the answer sheet.

Question No. 1 (Marks=10+5+5) (CLO-2)

- ✓ 1. Design an efficient assembly language program to generate a 500 Hz signal on P1.0 using Timer 0. The waveform should have a 30% duty cycle (duty ~~Cycle~~ ~~high-time~~ period).
✓ 2. Assuming that XTAL = 11.0592 MHz, indicate when the TF0 flag is raised for the following program.

```
MOV TMOD, #01
MOV TL0, #12H
MOV TH0, #1CH
SETB TR0
```

✓ 3. Who provides clock pulses to 8051 timers if C/T = 0?

Question No. 2 (Marks=10+10)

- ✓ 1. For XTAL = 11.0592 MHz, find the TH1 value (in both decimal and hex) for each of the following baud rates. ~~0 FD~~ -6 0 FA → 92 → 40H
(a) 9,600 → (b) 4,800 (c) 150
✓ 2. Write a program for the 8051 to transfer "YES" serially at 9600 baud, 8-bit data, 1 stop bit, do this continuously.

Question No. 3 (Marks=10+10)(CLO-1)

- ✓ 1. Describe Interrupts Vs Polling, Interrupt Service Routing, Steps in executing an Interrupt, six interrupts in the 8051, Enabling and Disabling an interrupt, steps in enabling an interrupt.
✓ 2. Comment each line of the following program and describe its purpose/output if LED is connected to pin P1.3 of the 8051 microcontroller.

```
ORG 0000H
LJMP MAIN
ORG 0013
SETB P1.3
MOV R3, #255
DJNZ R3, BACK
CLR P1.3
RETI
ORG 30H
MOV IE, #10000100B
SJMP HERE
END
```

MAIN:
HERE:

Question No. 4 (Marks=20)(CLO-3)

- Assuming that we need an 8031 system with 16KB of program space, 16KB of data ROM starting at 0000H, and 16k NV-RAM starting at 8000H. show the design using a ~~74LS138~~ for the address decoder. (Note: write and comment the address map, describe the design and its implementation)