Name: _____

Registration: _____

(10 pts.) Given the following partial module for a 128Kx32 RAM chip, fill in the blanks to complete the module.

```
module RAM (adr, CS, RW, di, do);

     input CS, RW;
     input [16:0] adr;
     input [31:0] di;
     output [31:0] do;
     reg [31:0] d_out;
     reg [31:0] Mem1 [0:131071];

     assign do = (CS && RW)?d_out:32'bz;

     always @(adr or di or CS or RW)
          if (CS && !RW)
               Mem1 [adr] = di;
     always @(adr or CS or RW)
          if (CS && RW)
               d_out = Mem1 [adr];

     initial
          $readmemh ("memory1.dat", Mem1);

endmodule
```