Practice Quiz 1 + Solution

Q1.
Give the result (in binary) of Verilog expression A+(B|C) for the following inputs: A=4'b1100, B=3'b100 and C=3'b010. Assume A is a 4-bit wire and B and C are each 3-bit wires. Show your result using Verilog notation, such as 3'b101.

****Solution****

```
4'b0010
//| = Bitwise OR
//+ = Addition
```

Q2.
Give the result (in binary) of Verilog expression (A==B)?B:C for the following inputs: A=4'b1100, B=3'b100 and C=3'b010. Assume A is a 4-bit wire and B and C are each 3-bit wires. Show your result using Verilog notation, such as 3'b101.

****Solution****

```
3'b010
//Conditional Statement
```

Q3.
Give the result (in binary) of Verilog expression ~&A for the following input: A=4'b1100. Assume A is a 4-bit wire. Show your result using Verilog notation, such as 3'b101.

****Solution****

```
1'b1
//Reduction Operator ~&. Operates on all the bits within a word.
//Accepts a single word operand and produces a single bit as output.
```

Q4.
Write Verilog code that declares a 16-bit register, R_H1402, and initially assigns it the hexadecimal value 1402.

****Solution****

```
reg [15:0] R_H1402;
initial R_H1402 = 16'h1402;
```

Q5.
What advantage is there to connecting ports by name, rather than position?

****Solution****

Many solutions accepted, but the primary reason is that it is more likely that wires will be connected to the correct port (i.e. it is harder to make a mistake).

Q6.
Write the hardware description of a 5-bit mod-22 counter. The suggested skeleton file has been written below:

```
module mod22Cntr (O, ck, rst);
     input ck, rst;
     output [4:0] O;
     //WRITE YOUR CODE HERE



endmodule
```

****Solution****

```
module mod22Cntr(O, ck, rst);
     input ck, rst;
     output [4:0] O;
     //WRITE YOUR CODE HERE
     reg [4:0] O;

     always @ (posedge ck)
          if (~rst)
               if (O == 5'b10101)
                    O <= 5'b00000;
               else
                    O <= O+1;
     always @ (posedge rst)
          O <= 5'b00000;
endmodule
```