# Lab 05

## BCD to Seven Segment Decoder

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"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

Student Signature: _____

Submitted to:

**Engr. Faheem Jan**

Month Day, Year (23 03, 2025)


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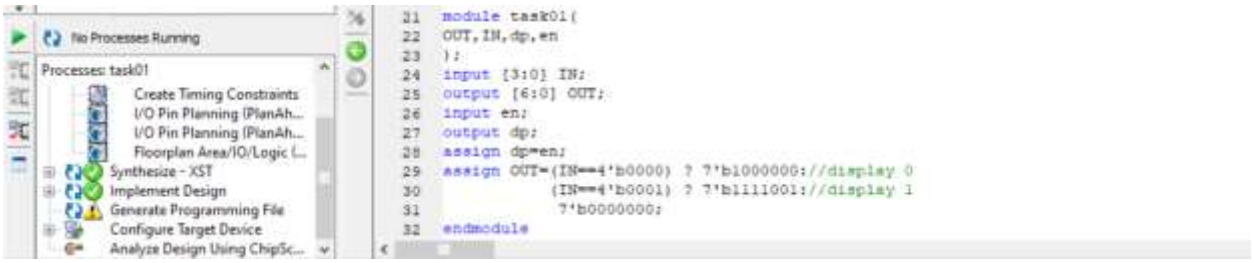
## Objective:

To implement a BCD to Seven Segment Decoder on Spartan 6 board.

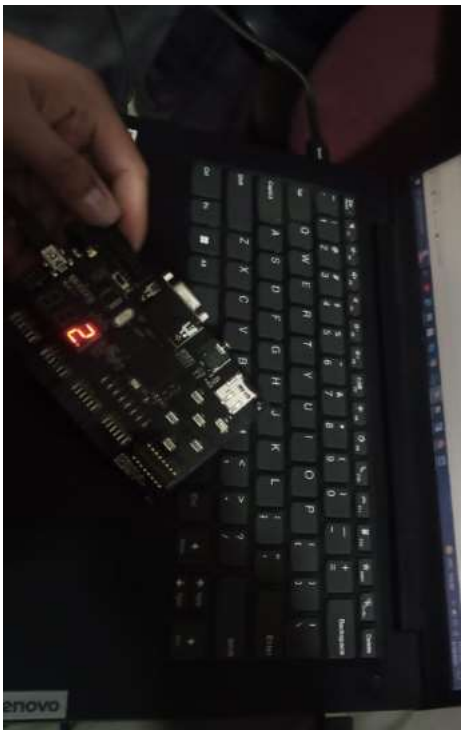
## Lab Task:

1- Using switches enter a BCD number and show the resulting number on the seven segment display.

**CODE:**




**OUTPUT:**

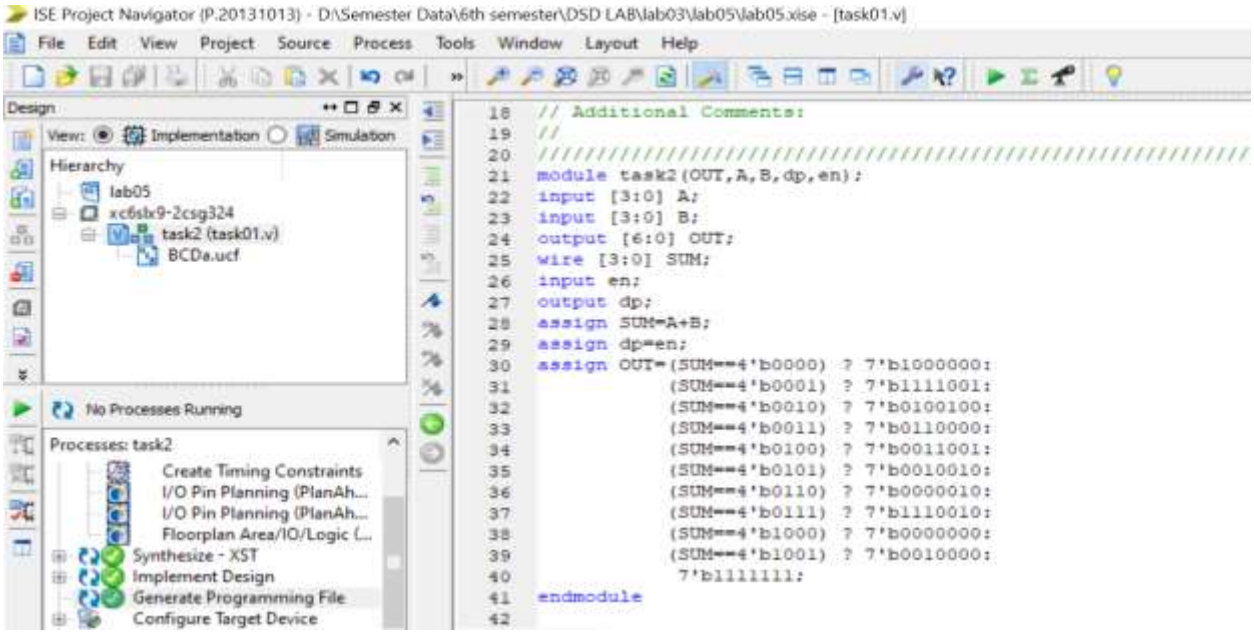


## Conclusion:

This Verilog module takes a 4-bit binary input (`IN`) and displays the corresponding decimal number on a seven-segment display. It currently supports only `0` and `1`, with other values turning the display off (`7'b0000000`). The `dp` (decimal point) is controlled by the `en` signal.

**TASK 02:**

Connect the output of your lab 02 (4 bit adder) to the seven segment display. Note that number above 1001 are not valid BCD numbers. In this situation keep the seven segment display off and just the dp on.




**OUTPUT:**


## Conclusion:

This Verilog module adds two 4-bit binary numbers (`A` and `B`) and displays the result on a seven-segment display. The output (`OUT`) lights up the correct segments to show the sum in decimal (0-9). The `dp` (decimal point) is controlled by the `en` signal, but it isn't essential for basic operation. If the sum exceeds 9, the display shows all segments off (`7'b1111111`).