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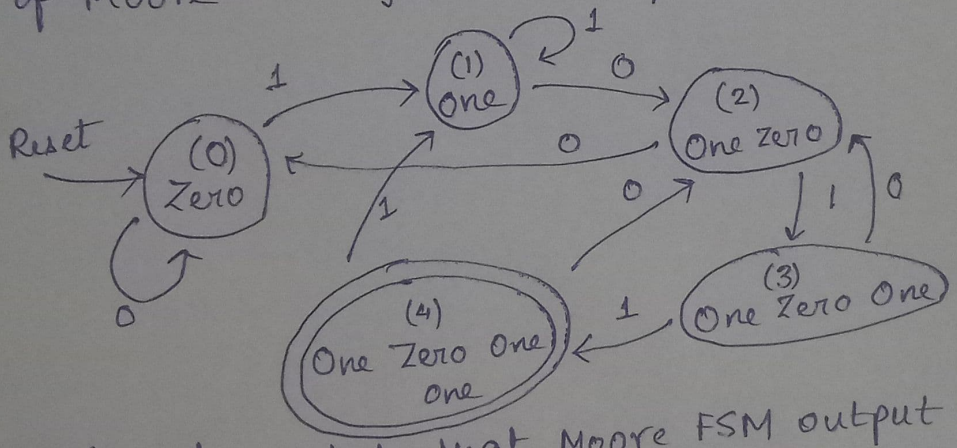
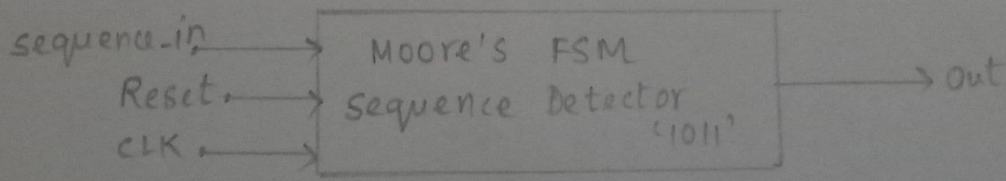
EXPERIMENT-14

- **Title:** Moore FSM sequence detector.
- **Objective:** Implementation of sequence detector
- **Course Outcome:** CO5
- **Bloom's Level:** Knowledge
- **Problem Statement:** The Moore FSM keeps detecting a binary sequence from a ~~binary~~ digital input and output of the FSM goes high only when a '1011' sequence is detected. Write a verilog code to design and test the FSM circuit.
- **Theory:** The Moore FSM keeps detecting a binary sequence from a digital input and output of the FSM goes high only when '1011' sequence is detected. The state diagram of Moore FSM for '1011' sequence is show here –



It is only noted that Moore FSM output only depends on the current state of the FSM.

- **Logic Diagram:**



Function Table :

CLOCK PULSE	SEQUENCE IN	DETECTOR OUT
↑	L	L
↑	H	L
↑	L	L
↑	H	L
↑	H	H
↑	L	L
↑	H	L
↑	H	H

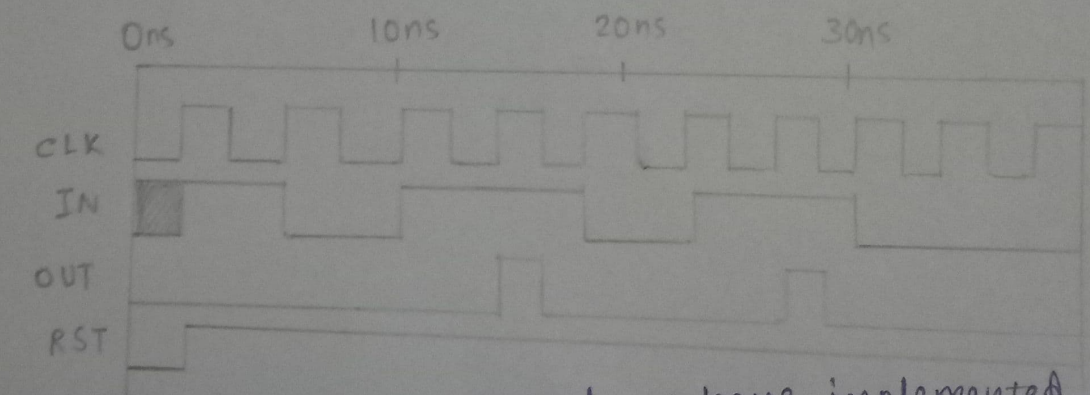
Design Code:

```
module sequence_detector (input in, output out, input clk,
                                                input rst);
    reg [2:0] current = 0;
    reg out = 0;
    always @ (posedge rst) begin
        current <= 0;
        out = 0;
    end
    always @(posedge clk) begin
        case (current)
            0: if (in==1) begin
                current <= 1; end
            1: if (in==0) begin
                current <= 2; end
            2: if (in==0) begin
                current <= 0; end
               else
                begin
                current <= 3; end
            3: if (in==0) begin
                current <= 2; end
               else begin
                current <= 4;
                out <= 1; #2 out <= 0; end
            4: if (in==0) begin
                current <= 2; end
               else
                begin
                current <= 1; end
            default: current <= 0;
        endcase
    end
endmodule
```

□ Testbench Code:

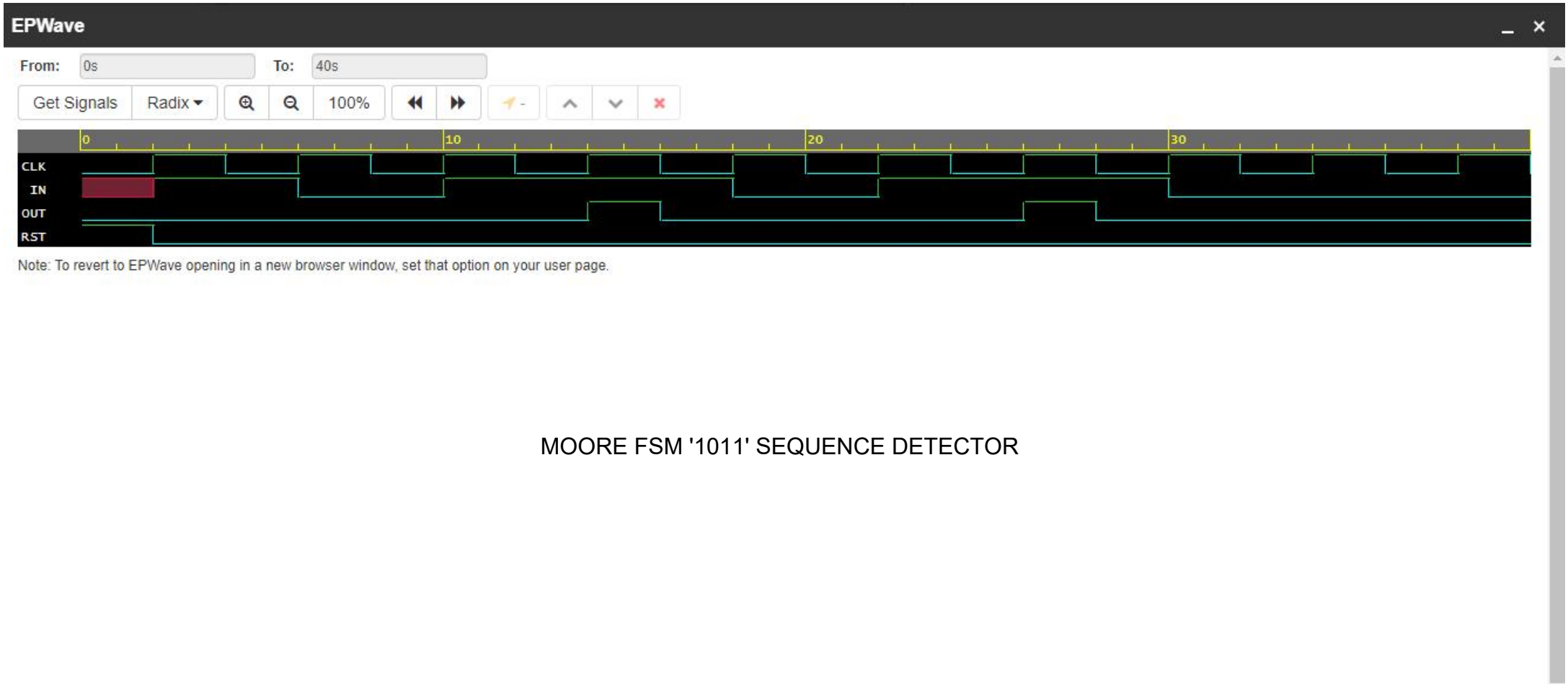
```
module sequence_detector_tb();
    reg IN; reg CLK; reg RST;
    wire OUT;
    sequence_detector uut(.in(IN),.out(OUT),.clk(CLK),.rst(RST));
    initial begin
            $dumpfile("dump.vcd"); $dumpvars(1);
            CLK=0;
            RST=1; #2;
            RST=0;
            IN=1; #4;
            IN=0; #4;
            IN=1; #4;
            IN=1; #4;
            IN=0; #4;
            IN=1; #4;
            IN=1; #4;
            IN=0; #10;
            $finish;
    end
    always #2 CLK=~CLK;
endmodule
```

□ Timing Diagram:



□ Discussion: In this experiment, we have implemented a FSM sequence detector which can detect a sequence of 1011. We came to know that this sequence detector can be used in many real life situations. With this, we have learned various HDL terms also.

- Justification of CO: In this experiment, we have implemented a FSM sequence detector, which was basically a little bit unknown and new problem to us. We also have tested the feasibility and functionality of this circuit, using verilog HDL code, which fulfils the conditions of COs. Hence, CO5 is justified.



MOORE FSM '1011' SEQUENCE DETECTOR