Full Adder Report

For the Simulation of the Full adder, a project in Model Sim is created. In the project directory, the “full\_adder.v” and “full\_adder\_tb.v” Verilog files was included and then compiled . The library now contains all of our files, and we can Start the Simulation by clicking “full\_adder\_tb.v” under work directory. After dragging the object components to the Wave panel in ModelSim we can finally start the Simulation. The wave was formed like it is shown in Fig 1.

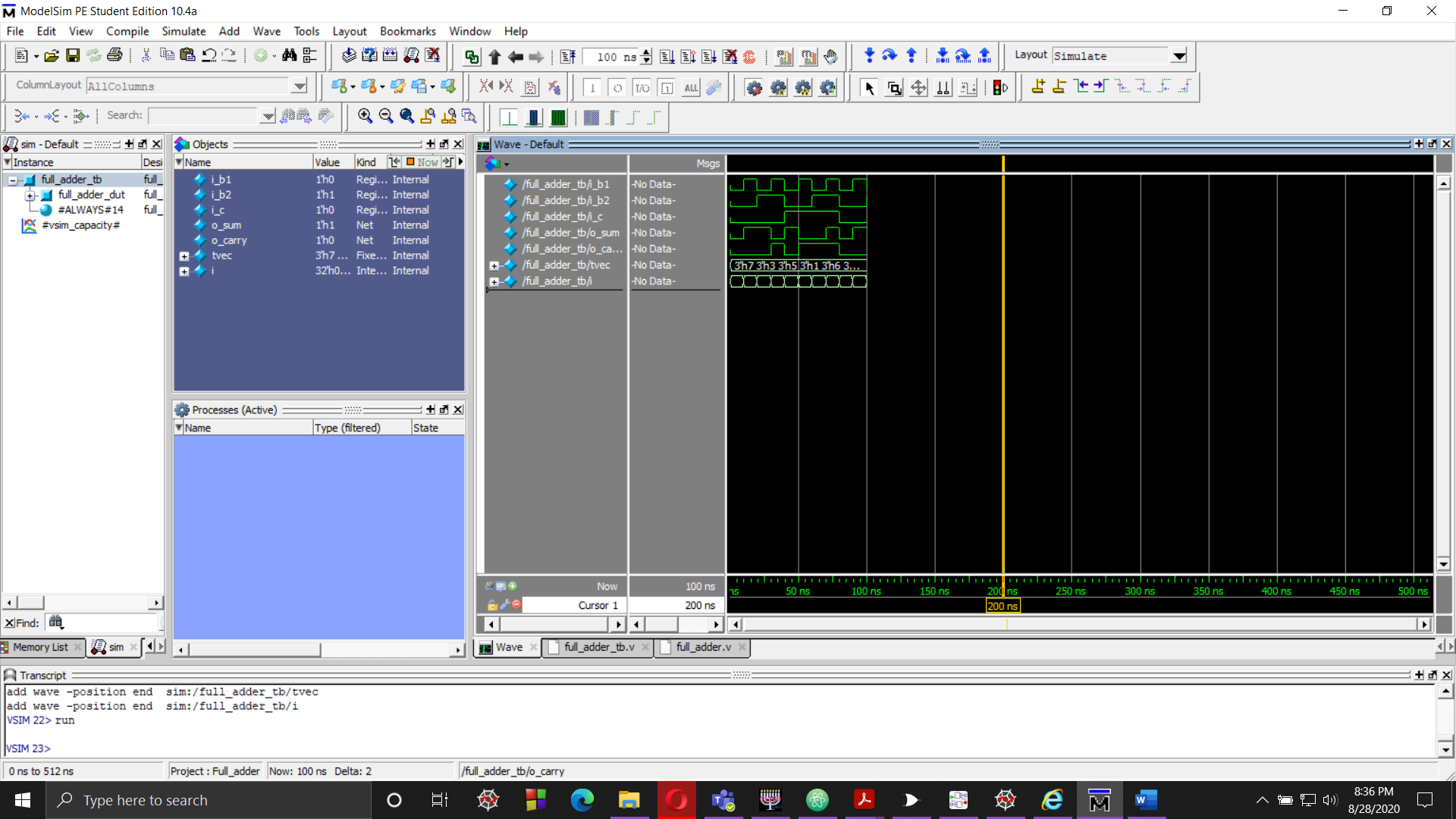


Fig 1

To observe the waves and how the Test bench file,”full\_adder\_tb.v”, worked.   
The test bench file reads a “FAT.tv” file, which has the inputs on “i\_bit1”, “i\_bit1” and “i\_carry” in a format of like Fig 2.

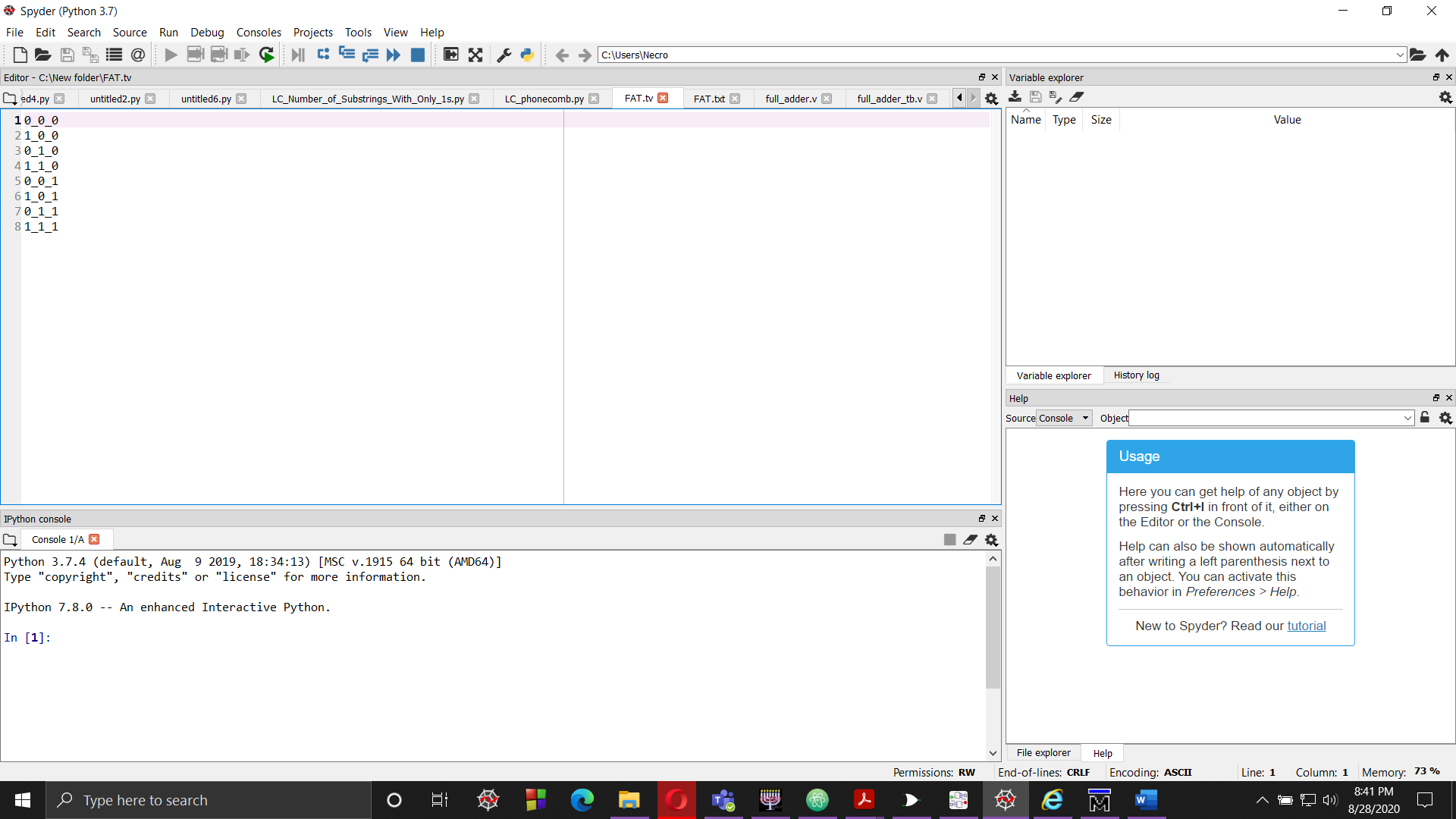
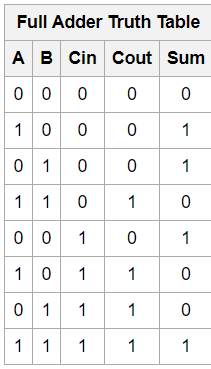


Fig 2

The test bench file then puts it in the “tvec” array and loops through it.

The truth table of Full Adder is shown below.



We will use the Truth table to verify how the “Cout” and “Sum” bits will result after the Input 1 A, Input 2 “B”, and carry “Cin” is given.

After the Wave is formed in the Wave panel. We can see how the inputs worked and get to check the output carry bits, the “o\_carry” bits and output sum bits, the “o\_sum bits”.

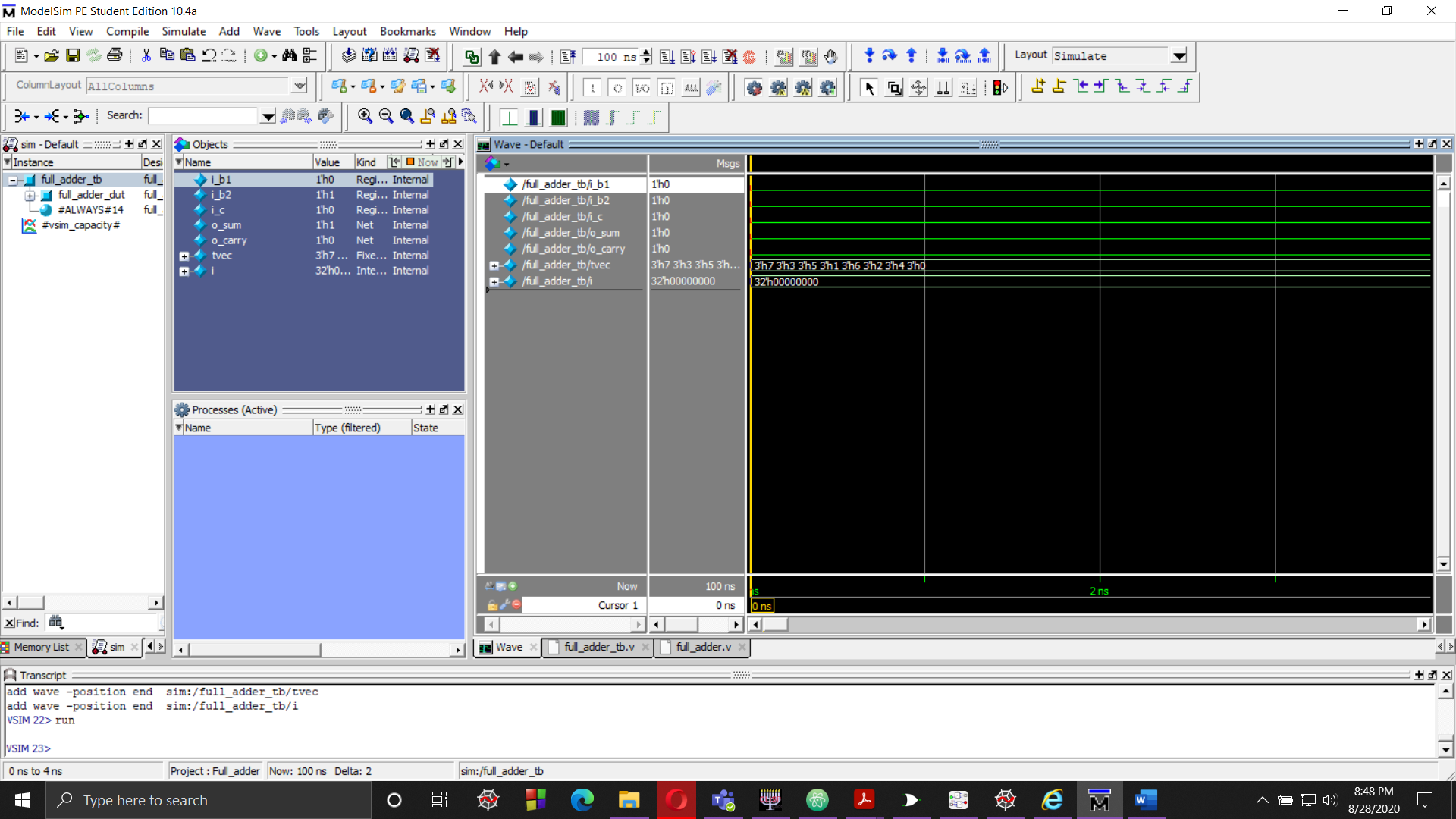


Fig 3

In Fig 3 , we can see in the “full\_adder\_tb.v” file that ,“i\_b1” , “i\_b2” and “i\_c” is set to 0, 0 and 0 , respectively. Giving us the “o\_sum” and “o\_carry” bits as 0.

Rest of the wave simulation is displayed below.

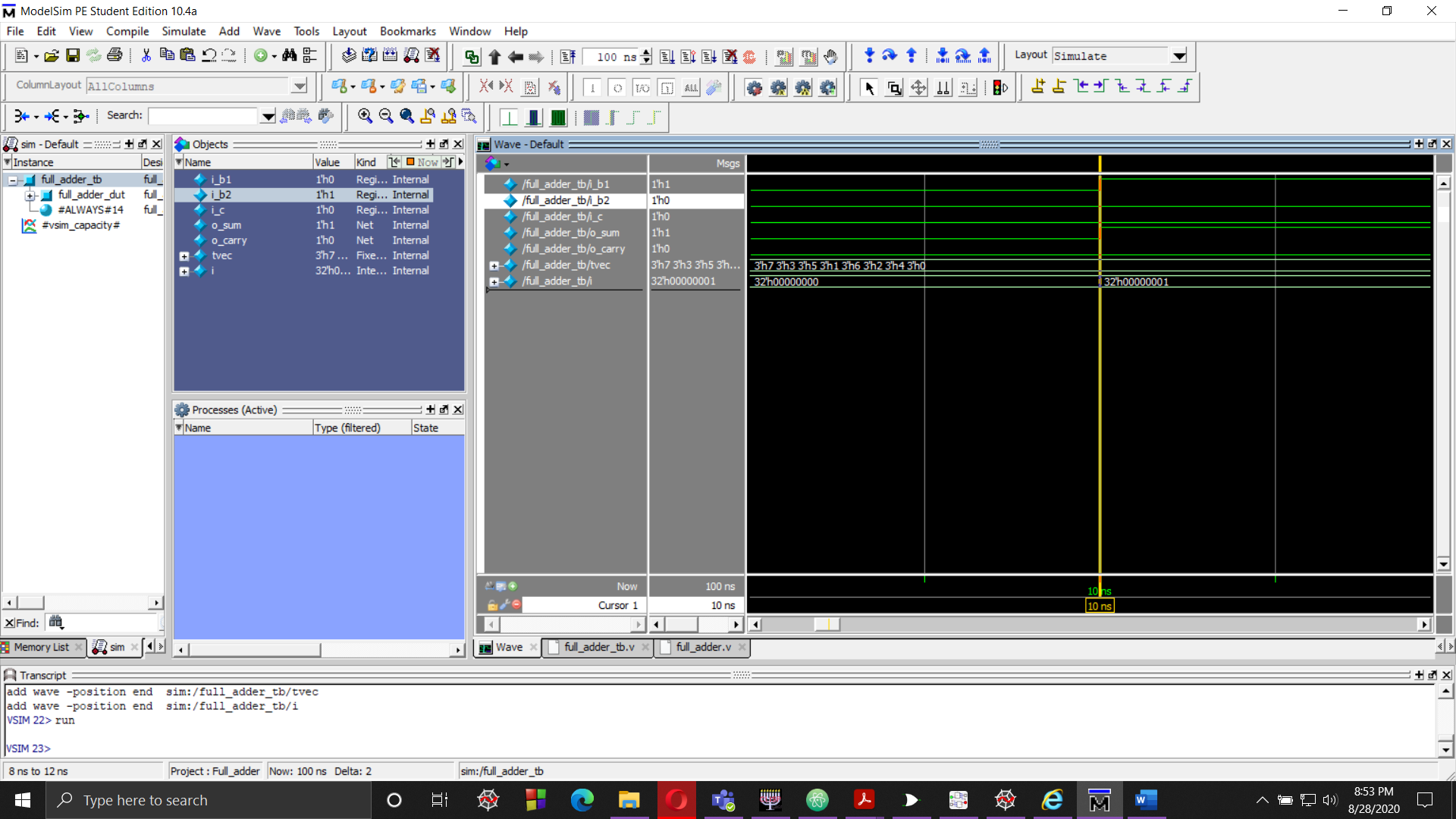


Fig 4

In Fig 4, the “i\_b1” , “i\_b2” and “i\_c” is set to 1, 0 and 0 , respectively. Giving us the “o\_sum” bits as 1 and “o\_carry” bits as 0.

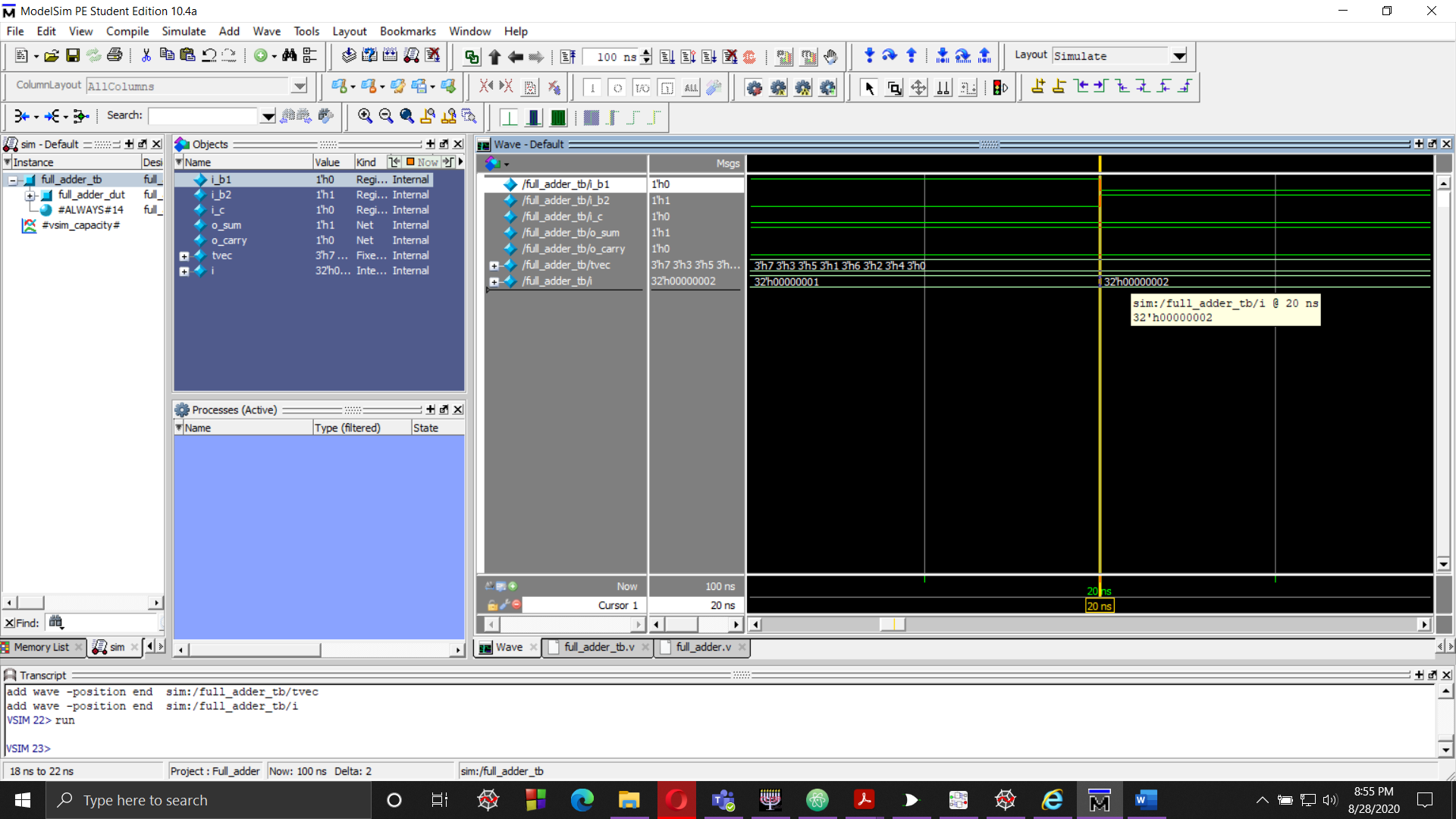


Fig 5

In Fig 5, the “i\_b1” , “i\_b2” and “i\_c” is set to 0, 1 and 0 , respectively. Giving us the “o\_sum” bits as 1 and “o\_carry” bits as 0.

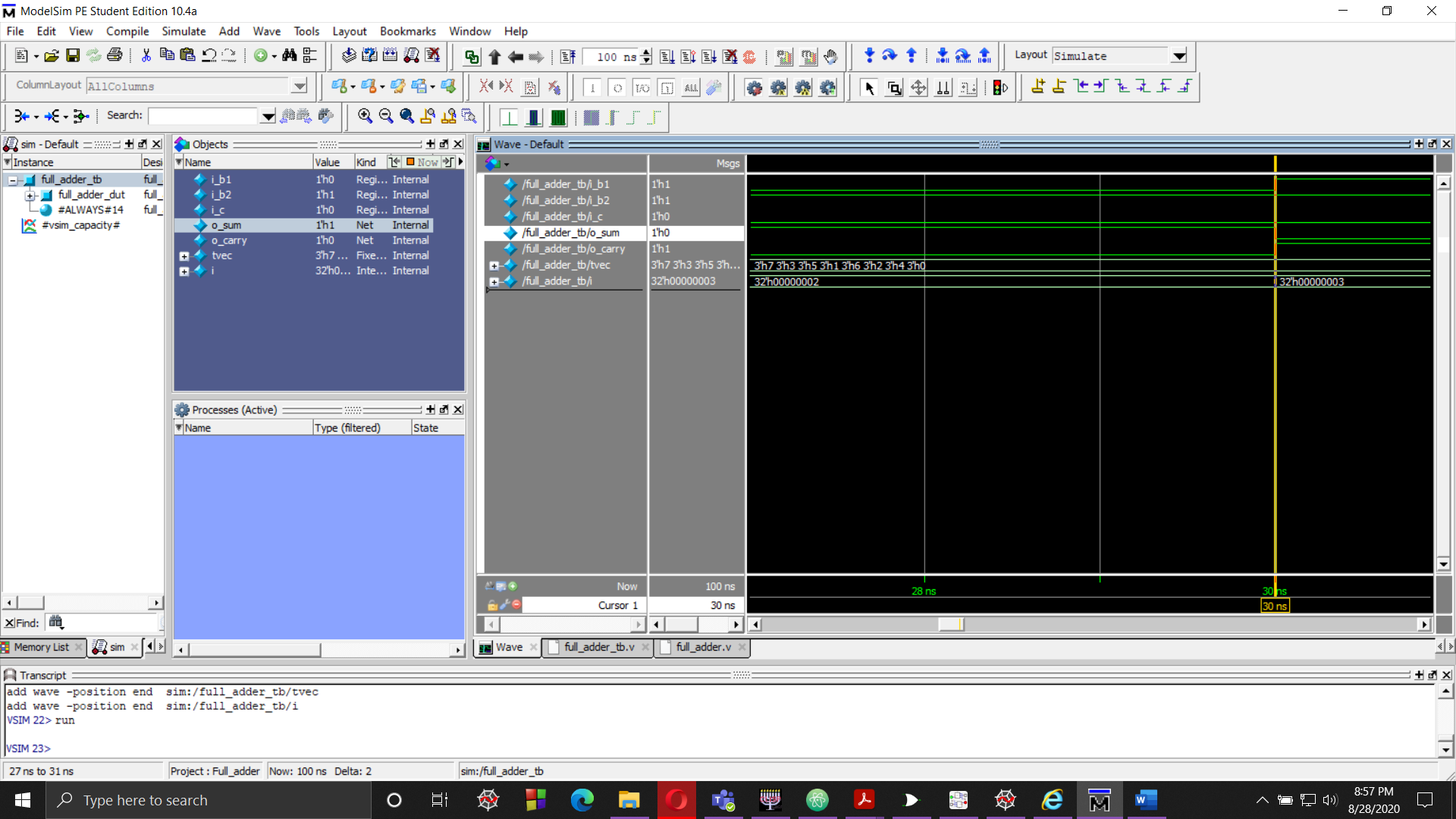


Fig 6

In Fig 6, the “i\_b1” , “i\_b2” and “i\_c” is set to 1, 1 and 0 , respectively. Giving us the “o\_sum” bits as 0 and “o\_carry” bits as 1.

By visualizing the intervals in the waves panel, we can see how the output sum and output carry bits behaves when input 1, input 2 and carry bits are applied.

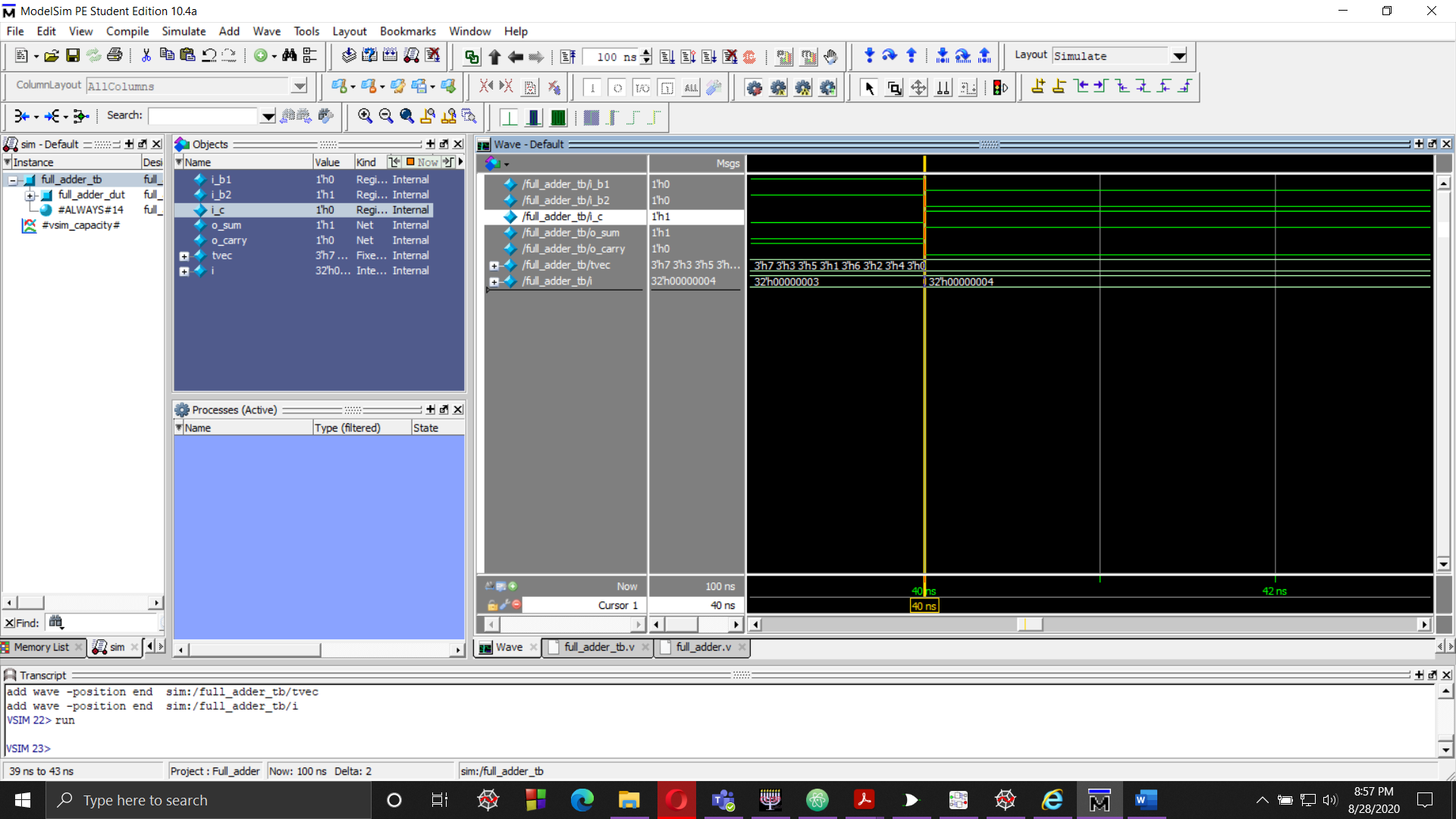


Fig 7

In Fig 7, the “i\_b1” , “i\_b2” and “i\_c” is set to 0, 0 and 1 , respectively. Giving us the “o\_sum” bits as 1 and “o\_carry” bits as 0.

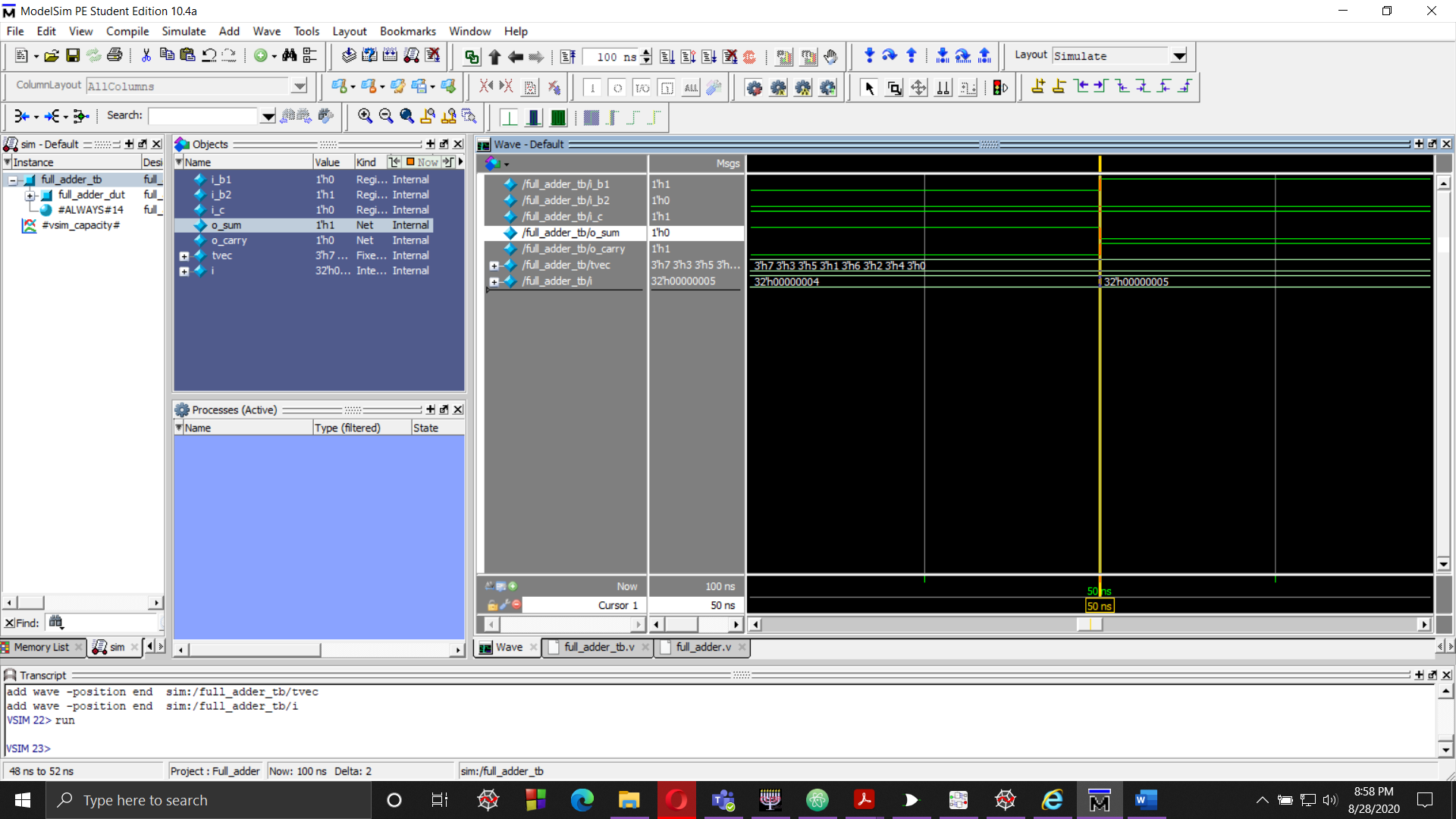


Fig 8

In Fig 8, the “i\_b1” , “i\_b2” and “i\_c” is set to 1, 0 and 1 , respectively. Giving us the “o\_sum” bits as 0 and “o\_carry” bits as 1.

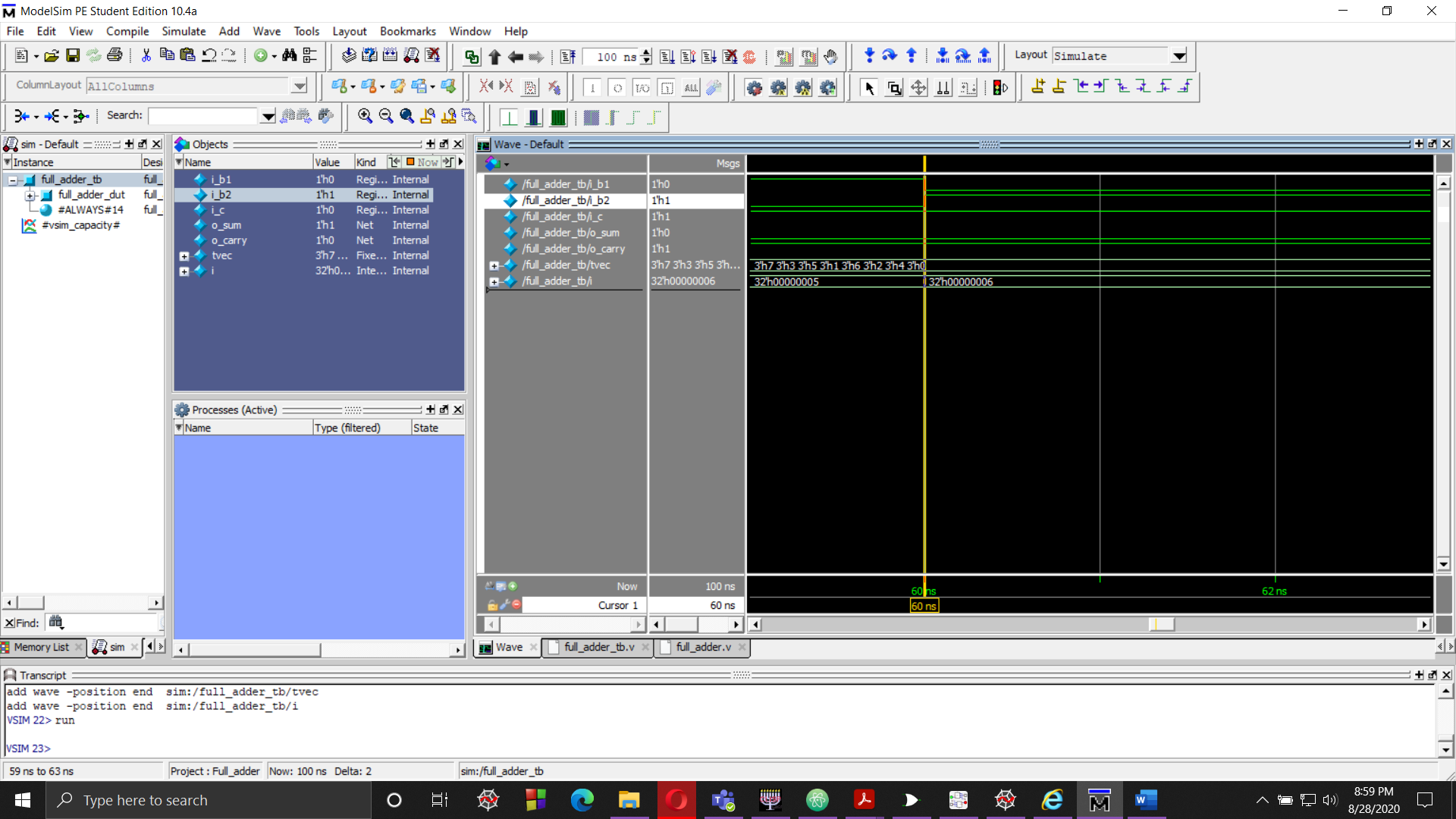


Fig 9

In Fig 9, the “i\_b1” , “i\_b2” and “i\_c” is set to 0, 1 and 1 , respectively. Giving us the “o\_sum” bits as 0 and “o\_carry” bits as 1.

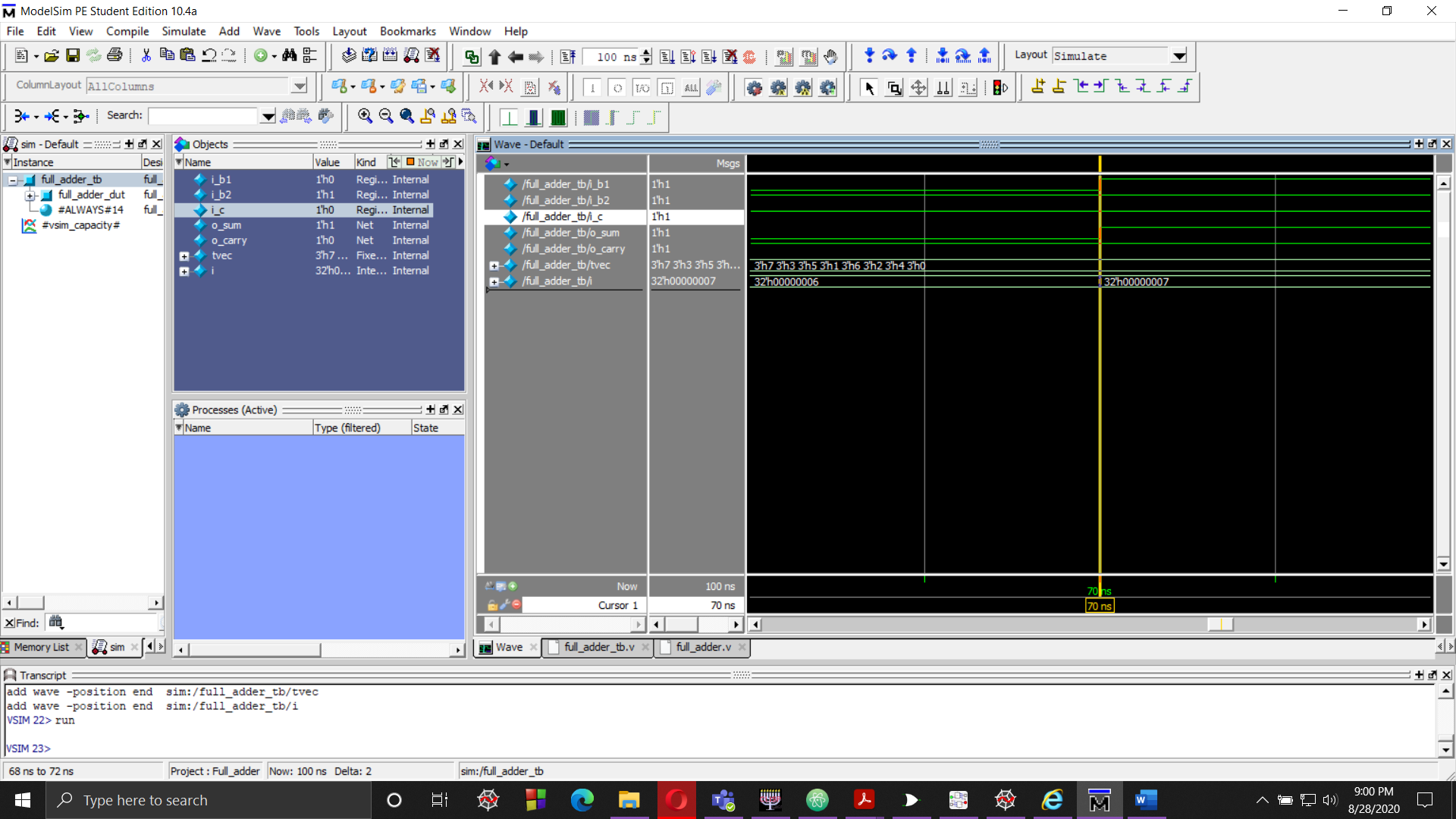


Fig 10

In Fig 10, the “i\_b1” , “i\_b2” and “i\_c” is set to 1, 1 and 1 , respectively. Giving us the “o\_sum” bits as 1 and “o\_carry” bits as 1.