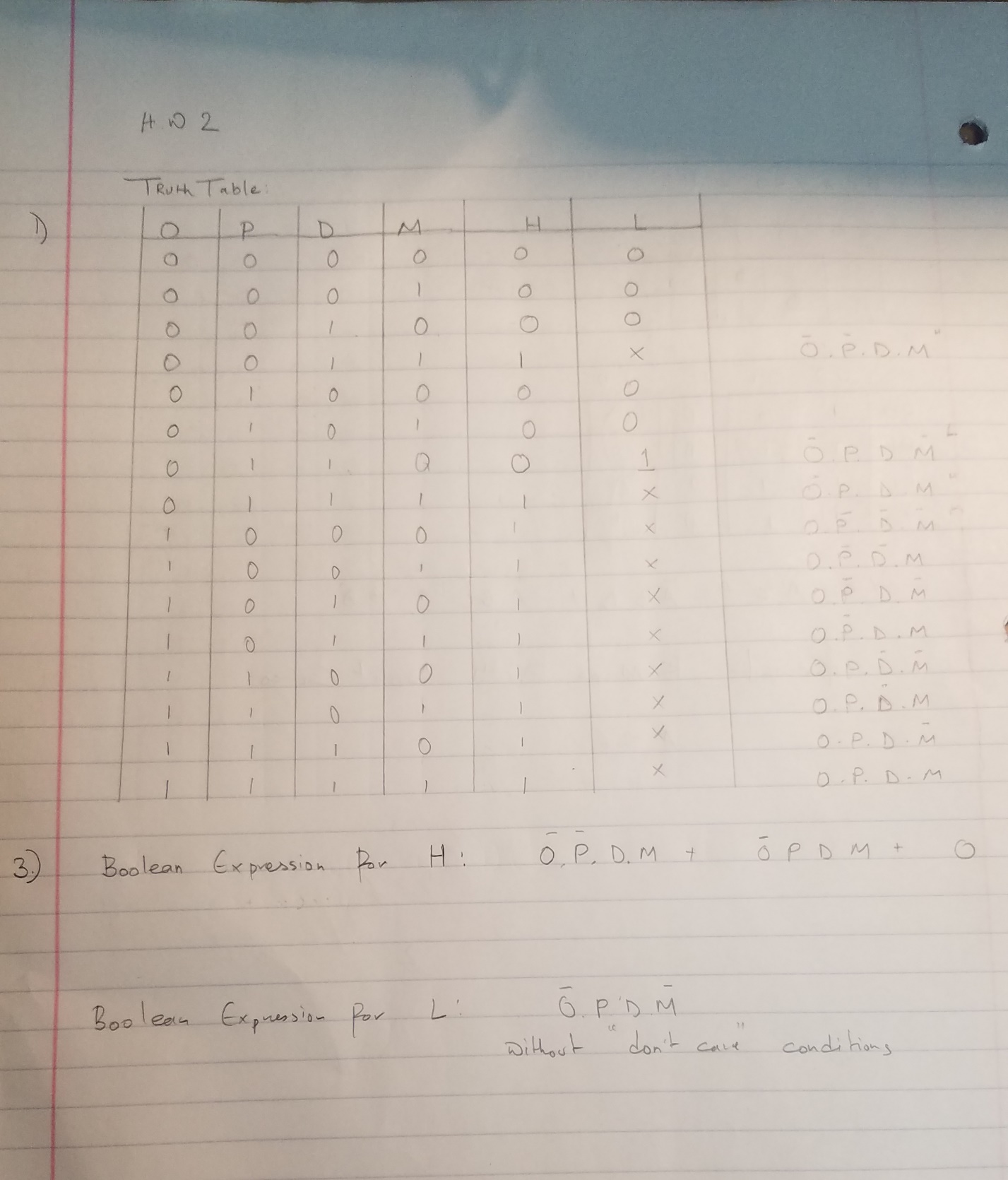
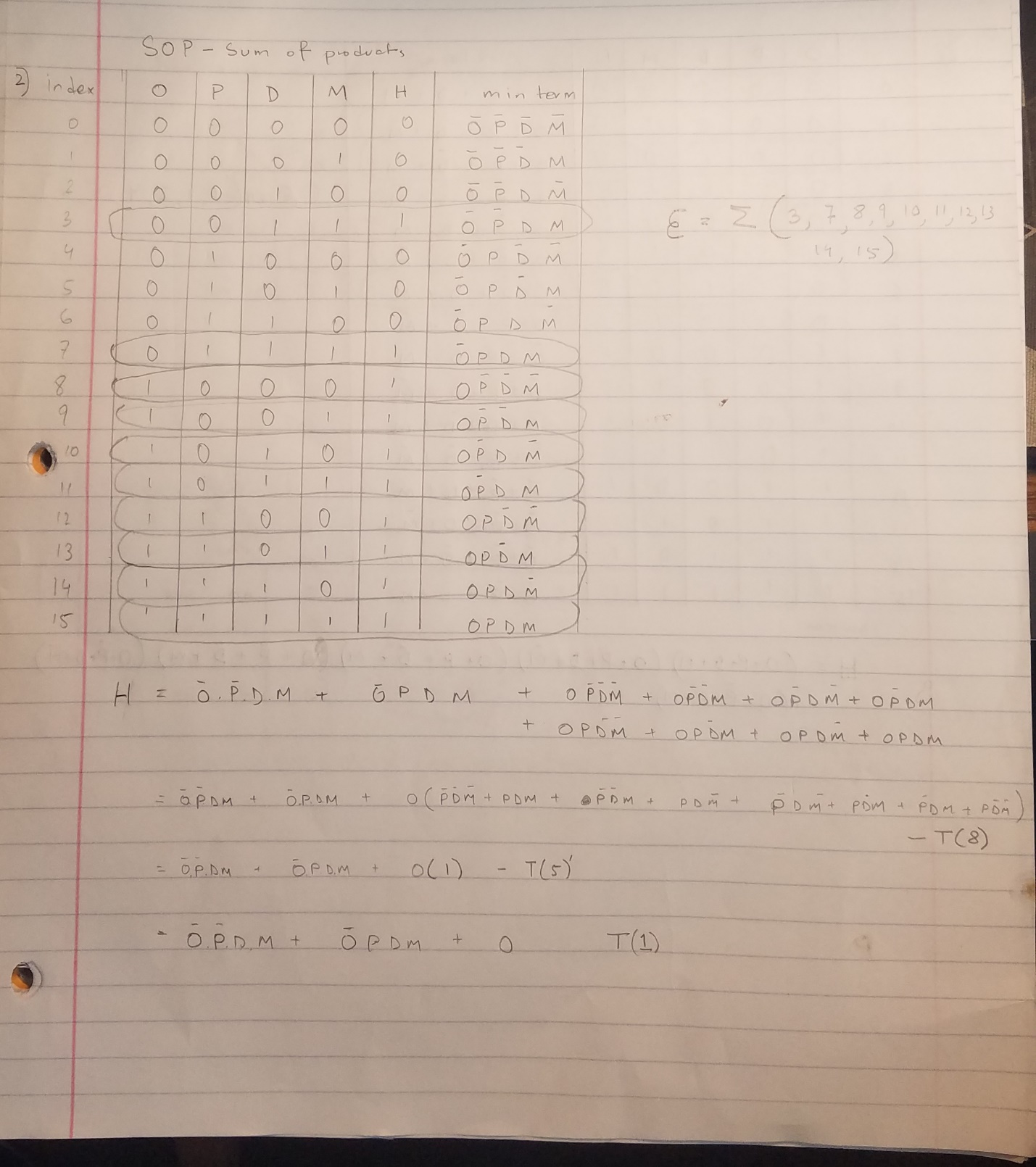
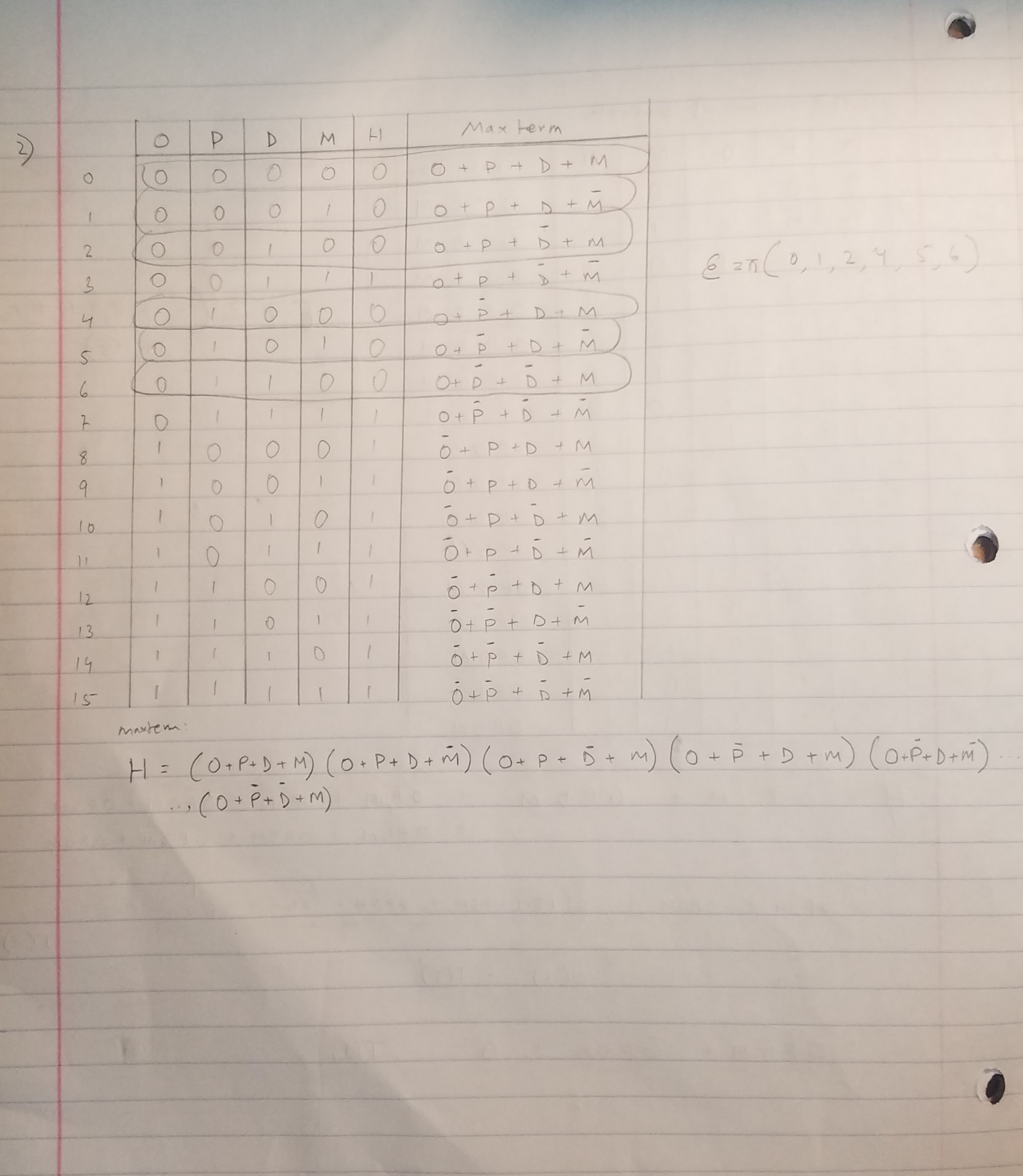
CS 4341.001  
Mxa166030

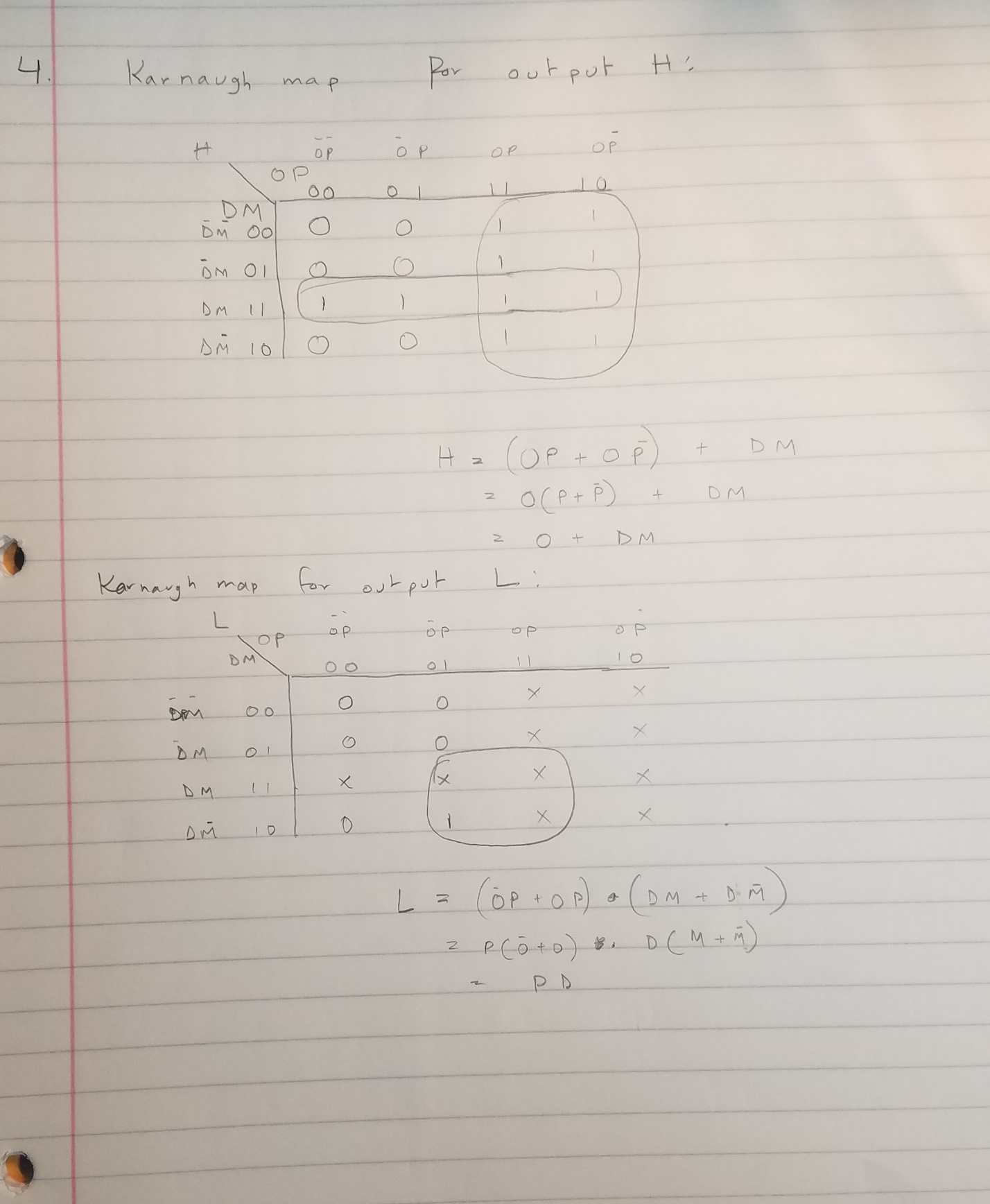
Moin Ahmed

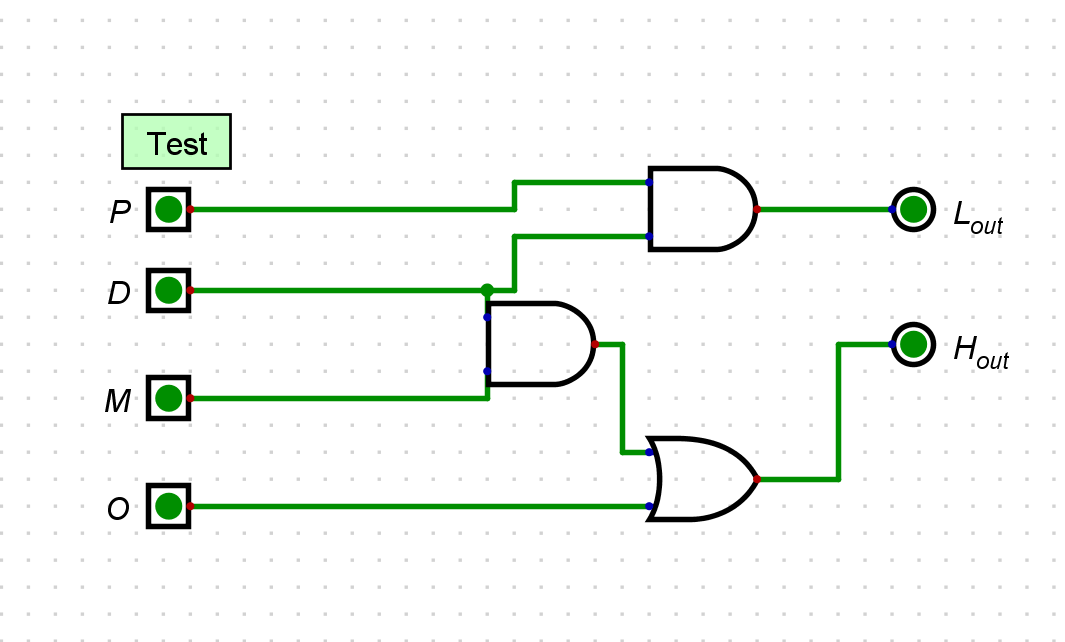
Homework 2



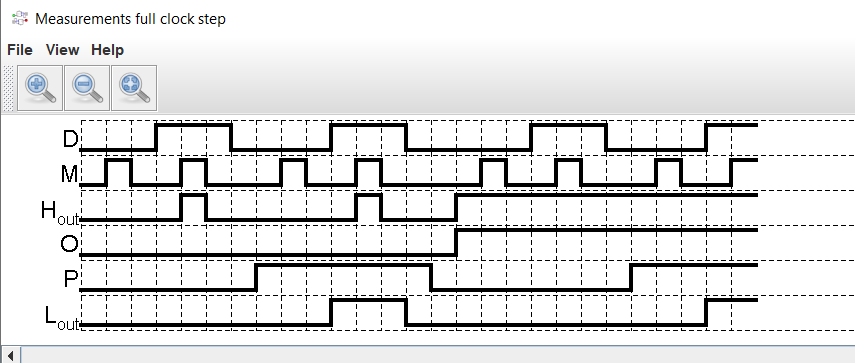




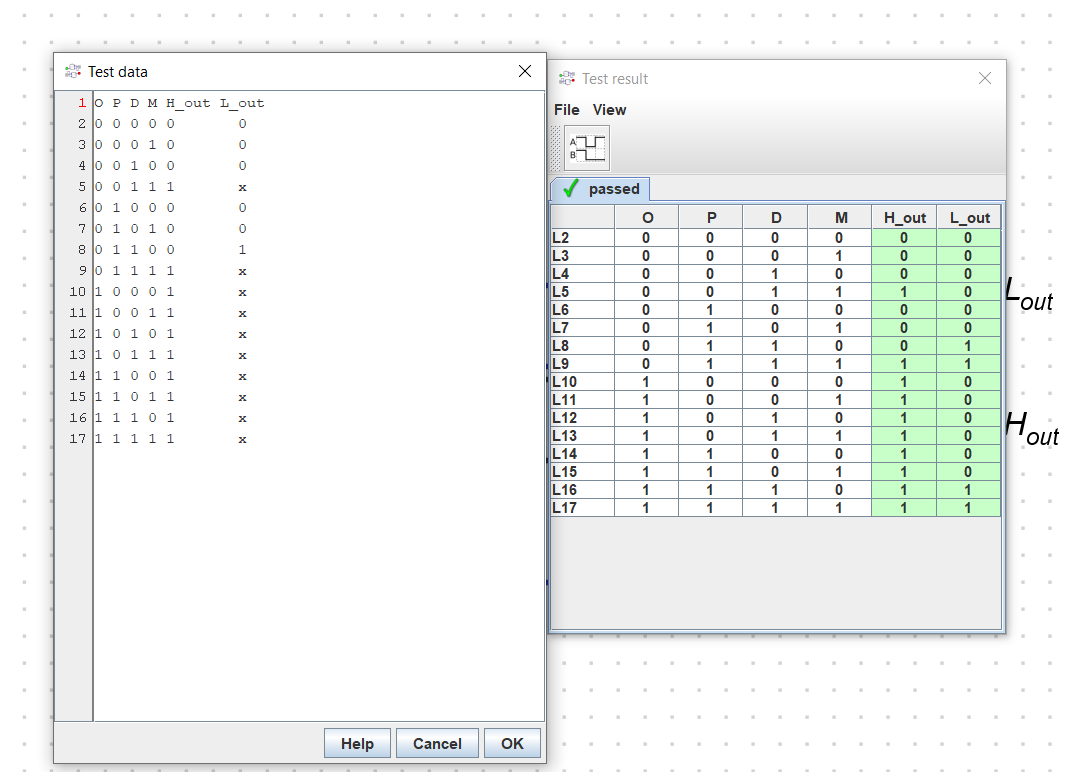


5. The schematic of the circuit:

Manual verification:



6.Test results:



7.verilog code:

(Opdm\_main.v )

module opdm

(

i\_O,

i\_P,

i\_D,

i\_M,

o\_H,

o\_L

);

input i\_O;

input i\_P;

input i\_D;

input i\_M;

output o\_H;

output o\_L;

wire w\_WIRE\_1;

wire w\_WIRE\_2;

wire w\_WIRE\_3;

assign w\_WIRE\_1 = i\_P & i\_D;

assign w\_WIRE\_2 = i\_D & i\_M;

assign w\_WIRE\_3 = i\_O | w\_WIRE\_2;

assign o\_L = w\_WIRE\_1;

assign o\_H = w\_WIRE\_3;

endmodule

(opdm\_testbench)

module opdm\_tb();

reg i\_o,i\_p,i\_d,i\_m;

wire o\_h,o\_l;

reg [3:0] A [15:0];

integer i;

opdm opdm\_dut(.i\_O(i\_o), .i\_P(i\_p), .i\_D(i\_d), .i\_M(i\_m), .o\_H(o\_h), .o\_L(o\_l));

initial begin

$monitor("Value of O=$b,P=$b,D=$b,M=$b,H=$b,L=$b",i\_o ,i\_p ,i\_d ,i\_m ,o\_h ,o\_l);

i\_o= 0; i\_p=0; i\_d=0; i\_m=0;

#50 i\_o= 0; i\_p=0; i\_d=0; i\_m=1;

#50 i\_o= 0; i\_p=0; i\_d=1; i\_m=0;

#50 i\_o= 0; i\_p=0; i\_d=1; i\_m=1;

#50 i\_o= 0; i\_p=1; i\_d=0; i\_m=0;

#50 i\_o= 0; i\_p=1; i\_d=0; i\_m=1;

#50 i\_o= 0; i\_p=1; i\_d=1; i\_m=0;

#50 i\_o= 0; i\_p=1; i\_d=1; i\_m=1;

#50 i\_o= 1; i\_p=0; i\_d=0; i\_m=0;

#50 i\_o= 1; i\_p=0; i\_d=0; i\_m=1;

#50 i\_o= 1; i\_p=0; i\_d=1; i\_m=0;

#50 i\_o= 1; i\_p=0; i\_d=1; i\_m=1;

#50 i\_o= 1; i\_p=1; i\_d=0; i\_m=0;

#50 i\_o= 1; i\_p=1; i\_d=0; i\_m=1;

#50 i\_o= 1; i\_p=1; i\_d=1; i\_m=0;

#50 i\_o= 1; i\_p=1; i\_d=1; i\_m=1;

end

endmodule

Waveform graph from ModelSim:

