Documentation

Description of the model of the

SMA Sunny Central

solar (and storage) inverters for power flow and stability studies in PSS®E

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Model Generation G
Document Revision 110
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Note

The inverter model "SMASC" described in this document replaces all former revisions of the model "SMASCI" that were issued between November 2009 and February 2011 by SMA Solar Technology AG for simulation of the Sunny Central HE and/or CP(-US) line.
Models of other inverter types are not affected and are not covered by SMASC.
Please replace all relevant SMASCI models in your simulations with the SMASC model.

The following PSS®E versions are currently supported:

- version 32 compiled with Intel Visual Fortran Compiler Revision 11.1,
- version 33 compiled with Intel Visual Fortran Compiler Revision 11.1,
- versions 34 and 35 compiled with Intel Visual Fortran Compiler Revisions 11.1 and 15.0 (x86).

Please contact SMA if models for other simulation platforms are required. Currently, SMA supports

- DIgSILENT PowerFactory (rms models)
- Siemens Power Technologies International PSS®E (rms models)
- General Electric International PSLF (rms models)
- Manitoba Hydro International Ltd. PSCAD® (instantaneous value models)
- ATP-EMTP (instantaneous value models)
- The Mathworks Matlab/Simulink® (rms and instantaneous value models, SMA internal only)

SMA model support

In case you require support from SMA Solar Technology AG regarding questions of model handling, model parameterization, or interpretation of simulation results, please send all relevant files to SMA including:

- The models you were using, or a reference to the model versions,
- the network in *.raw or *.sav format,
- the dyr file,
- simulation scripts in *.idv or *.py (Python) format that exactly replicate the relevant scenario,
- information on the PSS/E version.

Model history

SMASC_*GR_P*_Cc.obj is the model object file of SMASC, where *G* is the model generation, *R* is model revision, *P* is the PSS®E version for which the model was built, *C* is the compiler type, *c* is the compiler revision. (e.g. SMASC_C112_32_IVF111.obj is model generation C in revision 1.12 for PSS®E version 32, compiled with Intel Visual Fortran Compiler 11.1).

Model version		**Description**
C1.12	SMASC _C112_ *P*_Cc.obj	First release of SMASC generation C model
C1.14	SMASC _C114_ *P*_Cc.obj	Correction of a bug, relevant only if being used with pssecmd32.exe or pssecmd33.exe
C1.15	SMASC _C115_ *P*_Cc.obj	Initialization bug corrected; DGS "partial" mode revised
C1.16	SMASC _C116_ *P*_Cc.obj	Parameter FRTSwOffTm introduced – this parameter was set to 0.5 s (fixed) in earlier versions
C1.17	SMASC _C117_ *P*_Cc.obj	Over-/undervoltage and over-/underfrequency detection corrected
C1.18	SMASC _C118_ *P*_Cc.obj	Naming scheme of routines, subroutines and functions changed; now the routines, subroutines and functions have names with an additional designator for the model revision, e.g. former SMASC is now named to SMASC118 (see the sample dyr file, too)
C1.20	SMASC _C120_ *P*_Cc.obj	Reactive power set-point via machine variable EFD(I) ignored during fault ride-through situations
C1.21	SMASC _C121_ *P*_Cc.obj	Initialization bug corrected when GenTrpFlag = 1
C1.22	SMASC _C122_ *P*_Cc.obj	Change of revision C1.20 modified to reactive current set-point freezing in the internal control module during fault ride-through situations
C1.23	SMASC _C123_ *P*_Cc.obj	FRTPreErrVEna function implemented
C1.24	SMASC _C124_ *P*_Cc.obj	DGS "partial" behavior refined
C1.25	SMASC _C125_ *P*_Cc.obj	Apparent power limitation implemented; in earlier versions only the apparent current limitation was implemented
C1.26	SMASC _C126_ *P*_Cc.obj	DGS detection reworked for representation of SC CP firmware release 13 ("DGS limited" only); hysteresis parameters DbVolNomMaxH and DbVolNomMinH introduced; Note that the "DGS full" behavior still correlates to firmware releases below 13
C1.27	SMASC _C127_ *P*_Cc.obj	Parameter PFLim introduced for definition of reactive power capacity
C1.28	SMASC _C128_ *P*_Cc.obj	"Q on Demand" introduced

C1.29	Reserved for SC 1850-US	n/a
C1.30	Reserved for SC 1850-US	n/a
C1.31	SMASC _C131_ *P*_Cc.obj	DGSMod = 2 ("SDLWindV") characteristics corrected
C1.32	SMASC _C132_ *P*_Cc.obj	Active power priority implemented
C1.33	SMASC _C133_ *P*_Cc.obj	Pre-fault reactive current considered for active power priority; Pre-fault reactive current filtering considered in general (both priorities); Wait time for active power recovery after voltage recovery reduced for DGS "partial" mode
C1.34	SMASC _C134_ *P*_Cc.obj	Delay time calculation after "FRT partial" modified from "FRTSwOffTm+0.1" To "MAX(FRTSwOffTm,0.1)"
C1.35	SMASC _C135_ *P*_Cc.obj	Multiple generator support for plant control implemented; Reactive current filter after FRT exit implemented; Second PLL for frequency measurement implemented; First-order lag filter for frequency measurement implemented; FRT deadband hysteresis eliminated; Initialization scheme for cosφ(*P*) mode improved; Few parameter names revised (see Appendix)
C1.36	SMASC _C136_ *P*_Cc.obj	Storage inverter functionality added; Reactive current set-point filter halted during FRT; Active current set-point frozen during FRT
D1.37	SMASC _D137_ *P*_Cc.obj	Battery charge controller added
D1.38	SMASC _D138_ *P*_Cc.obj	Voltage and frequency protection stages added
D1.39	SMASC _D139_ *P*_Cc.obj	Reactive power capability at low active power increased
D1.40	SMASC _D140_ *P*_Cc.obj	Pre-fault reactive power handling after FRT corrected; FRT detection scheme revised; CON(J+112) introduced, with which writing into the file SMASCONi.txt can be suppressed (only for multiple generator support)
D1.41	SMASC _D141_ *P*_Cc.obj	Parameter QVArScale introduced for plant control response time correction (see section 4.6 Iq set-point scaling)
D1.42	SMASC _D142_ *P*_Cc.obj	Functions for simulation of SCStorage inverters added (see parameter SMASCSFlag)
D1.43	SMASC _D143_ *P*_Cc.obj	QVArScale scaling moved to setpoint signal input (EFD(I)); QVArScale initialization reworked

D1.44	SMASC _D144_ *P*_Cc.obj	Multiple generator support for plant control revised; this feature is now supported without writing SMASCONi.txt to the working directory and without using CHANGE_CON commands and writing these to the console or progress file; SMAPPC versions greater than or equal to C1.20 required for this; The obj file of SMAPPC C1.20 must also be loaded
D1.45	SMASC _D145_ *P*_Cc.obj	Initialization scheme for storage-only operation mode revised (SMASCSFlag = 1); the model can now initialize with arbitrary active power values
D1.46	SMASC _D146_ *P*_Cc.obj	Interaction with SMAPPC C1.21 enabled
E1.47	With beginning of model generation"E", the model is only provided in dll form, linked together with the PPC model and an additional ("invisible") generator set-point dispatch model necessary for multiple generator support	Multiple generator support functionality revised for compatibility with SMAPPC E1.22
E1.48		Active power recovery after fault clearance revised. The active current is now increased through a ramp function with slope parameter FRT_AmpDGra; Active power control following voltage disturbances (including fault) situations revised; Current injection spikes after fault clearance, leading to voltage spikes, mitigated through new implemented logic (uses parameter VREps – do not change this parameter without contacting SMA); FRT detection hysteresis introduced
E1.49		Active current minimum (14%) during FRT implemented; Active power control following voltage disturbances corrected (time constant during HVRT decreased by factor 3 instead factor 1/3 in revision E1.48); Voltage reference during LVRT revised – the filtered pre-disturbance voltage is used as a reference and the filter is stopped during LVRT (not HVRT). This applies only when FRTPreErrVEna = 1; Initialization with negative active power flow enabled when SMASCSFlag = 1; FRT voltage filter parameter names changed (to FRT_VolFilMod and FRT_VolDFilTm); FRT switch off/wait time parameter name changed (to FRT_WaitTm)

E1.50		FRT_AmpDGra ramp function revised (available primary power now taken into account)
E1.51	SMASC_E151_SMAPPC_E123_32_IVF111.dll SMASC_E151_SMAPPC_E123_33_IVF111.dll SMASC_E151_SMAPPC_E123_342_IVF111.dll SMASC_E151_SMAPPC_E123_342_IVF150.dll SMASC_E151_SMAPPC_E123_344_IVF111.dll SMASC_E151_SMAPPC_E123_344_IVF150.dll	Parameters FRT_AmpDLim and FRT_AmpQLim introduced
E1.52		Reactive power control as a function of grid (inverter terminal) voltage (VArCtlVol mode) implemented (please do not confuse this mode with the previously available Q(*U*) function)
E1.53		VarCtlVol mode filter only calculated when this mode is activated (avoids initialization errors when this mode is not used, but erroneously activated at model initialization)
E1.54		Parameter Frt_AmpQFilTm now available in the CON list
E1.55		Amplitude of Iq during FRT was slightly too low in model versions 1.48 – 1.53. This has been improved; Negative power flow was potentially possible when model was operated as a PV inverter model (SMASCSFlag = 0). This has been fixed; Frt_AmpDGra algorithm revised for Iq (pre-fault) < 0.1
E1.56		Various options for output of signal channel ANGLE(I) added – see description of parameter PLLFlag
E1.57		Parameter Frt_AmpQFilTm now effective
E1.58		Version compatible with SMAPPC E.127 and later, for multiple generator support when more than one SMAPPC instance is present – see parameter CON(J+112) MGCFlag
E1.59		Alternative initialization scheme implemented: the model can now also be initialized with full irradiation/DC power under the assumption it is curtailed from external (or internal, too)
E1.60		FLECS compiler warning removed; Apparent power limitation during FRT removed; Revision of the VarCtlVol function (STATE(K+34) during FRT set to +1 kvar and initialized to 0 after FRT exit)
E1.61		VarCtlVol function augmented by filtered terminal voltage set-point option, and limitation

E1.62		Compatibility with SMA Hybrid Controller model ensured
E1.63		Post-fault response of VarCtlVol function refined
E1.64		PLL algorithm revised (PLLFlag = 10.0) – beta version
E1.65		PLL algorithm revised (PLLFlag = 10.0) – preliminary version (no model acceptance test)
E1.66		VarCtlVolVolMin and VarCtlVolVolMax only applied when GriMngInvVArMod = 1; Initialization issue fixed when VarCtlVolVolNomSptMod = 0
E.167		Compatibility with SMAPPC master slave operation (please contact SMA, if needed); Compatibility with SMAPPC 1.33
E1.68		Project-specific version
E1.69		FRTAmpDGra ramp end condition refined
E1.70		Vol_PsD (STATE(K+43)) routed into FRT detection, instead of raw terminal voltage
E1.71		"Free" FRT characteristics implemented
E1.72		Power regulation time constant PwrCtl_VolDQFilTm introduced as parameter CON(J+139); FRT power toggling for BESS operation with very low initial power fixed
E1.73		FRTAmpQGra algorithm revised improving post-fault reactive current behaviour
E1.74		PLL calculated Vol_PsD now used for FRT detection and other calculations only when PLLFlag = 10
E1.75		Model information messages output redirected to LPDEV
G1.76		Communication with plant controller changed from MGCCTLVAL1Y8 to VARs based; All the functions and subroutines moved to CONTAINS; CON(J+112) changed from MGCFLAG to PC_BUS – defines plant controller bus number; Generating errors on LPDEV for reactive power > 0.6 and voltage outside FRT bounds
G1.77		Spike mitigation state machine revised to avoid current blocking during faults, when a double dip of the voltage signal appears at the beginning of a fault
G1.78		q-axis voltage calculation revised during initialization for to suppress initial conditions suspect warnings
G1.79		Compatibility with SMAHYC G3.3
G1.80		File naming (revision identifier) modified

G1.81		File naming (revision identifier) modified
G1.82		Introduction of WfilMod, WfilTm, VarFilMod and VarFilTm; Id set-point following freezing during FRT removed; 8inimum Id of 14% deactivated for SCS
G1.83		QoDEna and SMASCSFlag handling revised, so that battery inverter operation can be accomplished also with QoDEna == 0; Parameter AmpScl introduced; FRT current overshoot eliminated due to issues with high k factor; FRTAmpDGra algorithm revised; Corrected FRT partial current from 0.01 to 0.0; DCDC coupled inverter interface added (set SMASCSFlag to 3); FRT_AmpQFilTm (re-)initialization at fault entry/exit added; Spike mitigation functionality improved
G1.84		Parameter VarCtlVol_VolNomSptInit introduced – please see also modification of parameter VarCtlVol-VolNomSptMod
G1.85		Phase angle calculation modified – this fixes an issue with active power calculation during frequency deviation events
G1.86		Revised IniSchemeFlag logic, so that PPRIM reduction is effective even when IniSchemeFlag == 1
G1.87		1. Replacing apparent current limit with apparent power limit during FRT 2. Addition of CON (J+187) (IdMinPV) for calibrating the minimum 2kW auxiliary power consumption of the inverter 3. Addition of warning during initialization in case of breach of current and power limits
G1.88		Corrected FRT partial current from 0.01 to 0.0; Reduced signal noise during frequency deviation
G1.89		Added signals/channels W_avail, W_avail BESS (VAr_avail to be added later) In DCDC coupled mode, min Id during FRT changed to 0.14 pu as per PV mode DYDA output format improved Added signaling to HyCon, when PPrim changed from its initial value

Model validity

The inverter model "SMASC" described in this document is mainly intended for simulation of the SMA Sunny Central HE-20 and CP(-US) (XT) lines, and additionally the SMA Sunny Central (Storage) 2200(-US)/2475-EV/2500-EV(-US)/2750-EV(-US)/3000-EV/4000 UP/4200 UP/4400 UP/4600 UP and SMA Sunny Central Storage 1900/2200/2475/2900/2300 UP(-XT)/2400 UP(-XT)/2530UP(-XT)/2630 UP(-XT)/3450 UP(-XT)/3600 UP(-XT)/3800 UP(-XT)/3950 UP(-XT)/3450 UP/3600 UP/3800 UP/3950 UP lines. These devices support the DGS "full" mode in which reactive power is fed into the grid during faults. Therefore, the model can be used to study the in-fault behavior as well as the fault recovery (post-fault) behavior of the inverters (and, of course, the reaction of the grid) when these devices are connected to a network.
The model can also be used for simulation of the SMA SC 500HE-US inverter. Please note that this inverter does not support the DGS "full" mode. Instead, it only features the DGS "partial" mode in which feed-in of current is suppressed during faults. Nevertheless, the inverter remains connected to the grid in this mode, and resumes feed-in right after a fault has been cleared, i.e. the voltage has reached a threshold value.
Make sure to set the model parameter "FRTMod" to zero when simulating the SMA SC 500HE-US.
Please note that the terms "FRT" and "DGS" are used interchangeably.
In model generation D, basic functions of a Sunny Central storage inverter were added so that studies for this inverter can also be conducted with this model at a basic level. Especially projects with both solar and storage inverters and combined plant control of these inverters are targeted. The basic storage inverter function comprises bi-directional power flow and an integrated battery charge control.
The smallest time constant of the model is 0.01 s = 10 ms. Therefore, the model should be simulated with time step widths of 4, or 2, or 1 ms (recommended).

Known model inaccuracies

1. The active power set-point signal coming from the *P*(*f*) block and the signal coming from the active power set-point generation block is routed through a "MIN block" and then routed through a "common" rate limitation block (parameter WGra). In the inverter firmware there is one rate limitation block for the *P*(*f*) signal and an additional rate limitation block for the set-point signal. This is only relevant if parameter WCtlHzMod is activated.

Contents

1 Introduction and background

This document is intended to provide guidance to the PSS®E user in deploying the SMA Sunny Central line of solar inverters for power flow and stability studies. These inverters are typically integrated with an array of PV modules, step-up transformers and other balance-of-system components necessary to convert solar irradiance to grid-quality AC power for delivery at transmission or distribution voltage. The modular nature of PV plant construction allows for grid integration studies to be performed with an inverter model that is scalable to the capacity rating of the particular project under study.

The SMA Sunny Central inverters convert the DC power provided by the PV source circuits to AC power at three-phase output voltages in the range of 270 V to 690 V, depending on the particular inverter model. In a utility-scale photovoltaic power plant, this low voltage AC output would normally be connected to a pad-mounted step-up transformer which provides voltage transformation for integration of the inverter and its associated PV source circuits with the medium voltage power collection system within the plant. For transmission interconnected plants, a final transformation to high voltage or extra high voltage, as required for the particular transmission network interconnection, would occur at a collection substation.

The photovoltaic modules that serve as input sources to the inverter consist of solid state semiconductor cells that produce direct current as a function of the irradiance and the voltage to which they are subjected, on an essentially instantaneous basis. Several tests have shown that the fed-in AC power settles within one period of grid voltage in reaction to a step function DC power stimulus and can be neglected therefore in studies basing on RMS quantities.

Thus it is the inverter characteristics and controls that dominate the dynamic behavior of the plant and its interaction with the grid. SMA Sunny Central series inverters are classified as high-frequency, pulse-width-modulated, current-regulated inverters. They operate to regulate their respective AC output currents in response to a current command through high carrier frequency pulse width modulation (PWM) of the connected DC source. This provides a high fidelity sinusoidal output current waveform that is synchronized to the grid voltage waveform (i.e., it follows the grid frequency).

For a given level of solar irradiance, there is a unique DC voltage on the PV array that maximizes active power output. The inverter controls include the necessary intelligence to regulate this DC voltage to its optimum value on a quasi-continuous basis by varying the magnitude of its AC output current. This is known as maximum power point (MPP) tracking. But note that this tracking algorithm is not represented by the model.

2 Power flow model

An equivalence PV power plant utilizing SMA Sunny Central inverters may be modeled for power flow purposes as a generator connected to a P/V[1] bus (PSS®E type 2) with the appropriate nominal voltage from Table 1. The

- aggregate MVA of the plant (MBASE),
- maximum active power (PT) and
- reactive power limits (QT and QB)

must be specified as integral multiple of the individual inverter unit ratings defined in Table 1. However, the active power dispatch for the power flow simulation may be anywhere in the range of zero to (aggregate) PT.

Inverter type	MBASE (MVA)	PT (MW)	QT (Mvar)	QB (Mvar)	bus voltage (kV)
SC 500CP (XT)	0.500	0.500	0.240	-0.240	0.270
SC 630CP (XT)	0.630	0.630	0.302	-0.302	0.315
SC 720CP (XT)	0.720	0.720	0.345	-0.345	0.324
SC 760CP (XT)	0.760	0.760	0.364	-0.364	0.342
SC 800CP (XT)	0.800	0.800	0.384	-0.384	0.360
SC 850CP (XT)	0.850	0.850	0.408	-0.408	0.386
SC 900CP (XT)	0.900	0.900	0.432	-0.432	0.405
SC 1000CP XT	1.000	1.000	0.480	-0.480	0.405
SC 2200(-US)	2.200	2.200	1.320	-1.320	0.385
SC 2475-EV	2.475	2.475	1.485	-1.485	0.434
SC 2500-EV(-US)	2.500	2.500	1.500	-1.500	0.550
SC 2750-EV(-US)	2.750	2.750	1.650	-1.650	0.600
SC 3000-EV	3.000	3.000	1.800	-1.800	0.600
SC 2660 UP(-US)	2.660	2.660	1.596	-1.596	0.600
SC 2800 UP(-US)	2.800	2.800	1.680	-1.680	0.630
SC 2930 UP(-US)	2.930	2.930	1.758	-1.758	0.660
SC 3060 UP(-US)	3.060	3.060	1.836	-1.836	0.690
SC 4000 UP(-US)	4.000	4.000	2.400	-2.400	0.600
SC 4200 UP(-US)	4.200	4.200	2.520	-2.520	0.630

[1] The symbol *U* or *u* is used for voltage throughout the document.

SC 4400 UP(-US)	4.400	4.400	2.640	-2.640	0.660
SC 4600 UP(-US)	4.600	4.600	2.760	-2.760	0.690

Table 1: Power flow data by inverter type.

The following is only valid for inverters with increased power rating at low temperatures:

The apparent power dispatch of the inverter in the power flow solution should not exceed the values of MBASE in Table 1 at 50°C ambient conditions. At 25°C, the apparent power dispatch can even be up to 10% higher (addition of 1% per every 2.5°C step). Hence, the real power dispatch can be increased by 10% then, too.

Note that the reactive current command iq of the physical inverter control is always prioritized against the active power command id (unless active power priority switch PprioEna is activated). Therefore, the inverter active current I_d is limited by application of

$$I_d = \sqrt{I_{a,\max} - I_q^2}$$

where I_q is the inverter reactive current and $I_{a,max}$ is the maximum apparent current given by the maximum allowed apparent power of the inverter.

With this knowledge it is important to note that if the inverter is operated with S_{max} at low temperature and the temperature starts to rise up to, say, 50°C, then the power factor can even drop below 0.9.

E.g., at 25°C

$S_{max,\ 25°C}$ = 792 kVA operated with power $factor_{25°C}$ = 0.9 gives

$Q_{max,\ 25°C}$ = 345.2 kvar

Now, temperature rises to 50°C, then

$S_{max,\ 50°C}$ = 720 kVA still operated with $Q_{max,\ 25°C}$ = 345.2 kvar gives

power $factor_{50°C}$ = cos(asin($Q_{max,\ 25°C}$/$S_{max,\ 50°C}$)) = 0.88.

The temperature is not a model parameter and temperature dependence is not incorporated in the model.

2.1 Generator data in PSS®E

Figure 1 shows a typical data mask for the machine entry in the PSS®E load flow program. It is important that the "R Source" and "X Source" values are parameterized as shown in this mask.

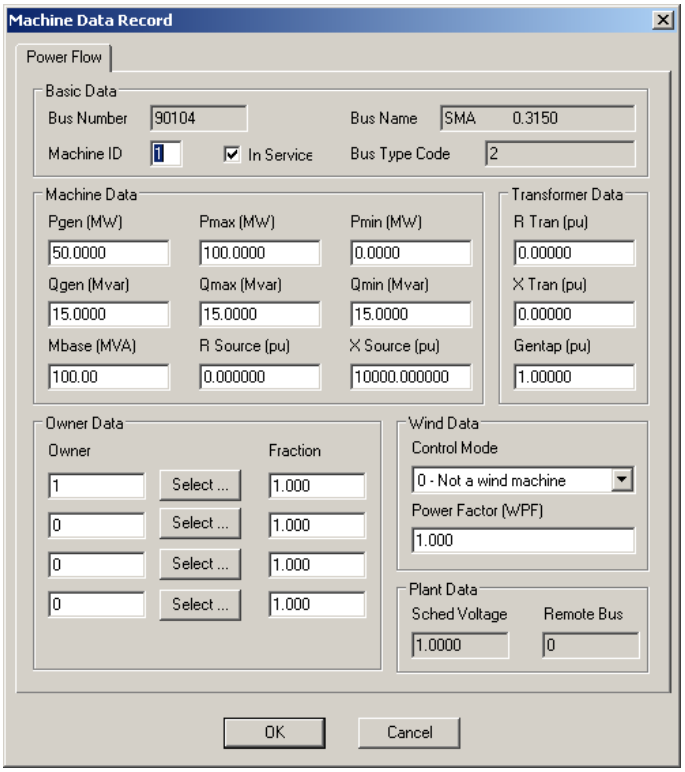


Figure 1: Typical data mask for machine entry in the PSS®E load flow program.

Furthermore, it is very important that the active power (Pgen), the reactive power (Qgen) and MBASE always satisfy the equation

$Pgen^2 + Qgen^2 <= MBASE^2$.

Otherwise, the model will initialize not correctly.

2.2 Capability curve

For more detailed power flow studies the *PQ* capability curve (Figure 2) of the inverter can be used, from which a PSS®E gcp file (Figure 3) can be constructed for usage with activity GCAP. A Microsoft Excel sheet (SMASC_CapabilityCurve.xlsx) is provided together with the model which should ease the preparation of the gcp file.

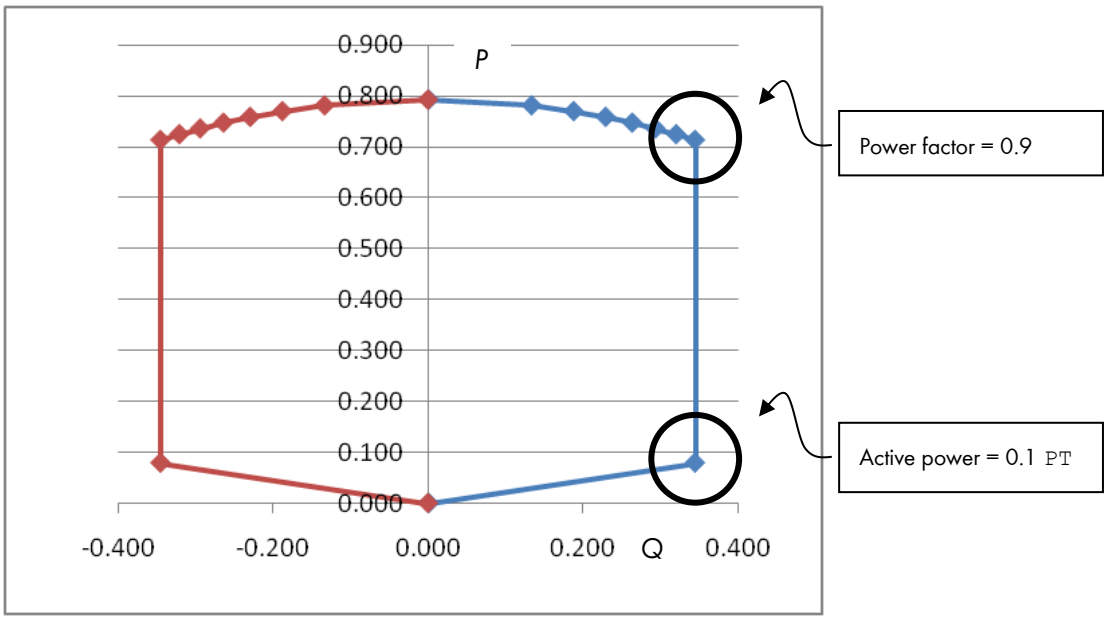


Figure 2: Exemplary *PQ* capability curve of a Sunny Central 720CP (XT).

Note that the CP-US (and newer) series is capable of providing a maximum power factor of 0.8 while the CP HE and the CP series are limited to a power factor of 0.9.

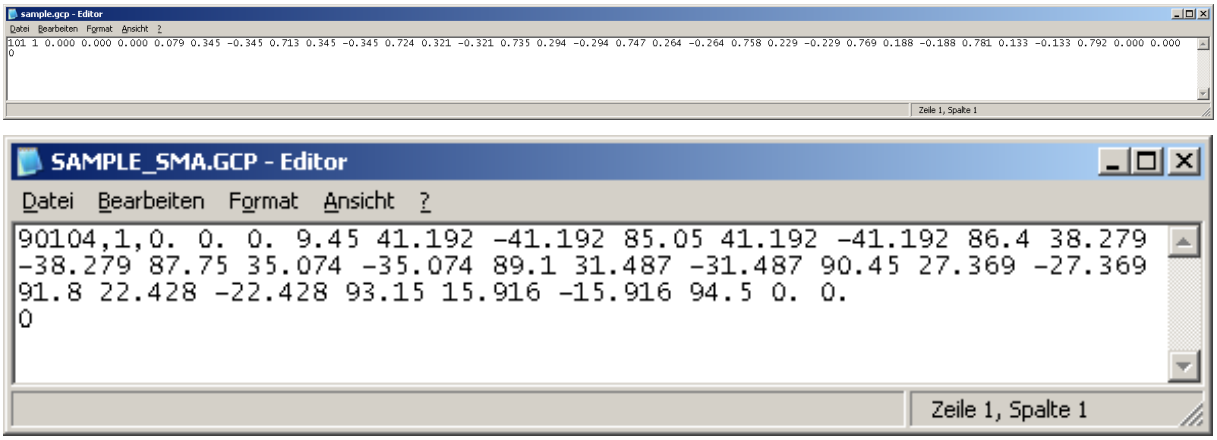


Figure 3: Sample PSS®E gcp file for usage with activity GCAP.

3 Dynamic model

The plant dynamic model has been implemented as a PSS®E user model called "SMASCxxx", making use of PSS®E's "coordinated call model" technique. It consists of a reduced order representation of the inverter controls represented in the block diagram of Figure 4.

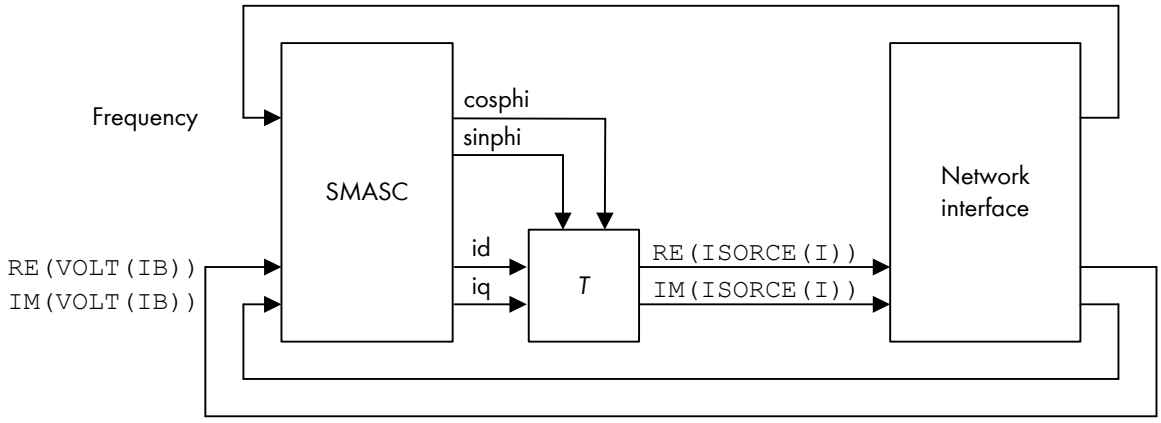


Figure 4: Positive sequence system dynamic model.

The model has two sources of excitation which are: the grid voltage (magnitude and angle in the external system reference frame), shown in rectangular coordinates as `RE(VOLT(IB))` and `IM(VOLT(IB))` in Figure 4, and the frequency, measured at the bus to which the inverter is connected. The model's outputs are the current commands in the *dq* reference frame id and iq, which are used to calculate the grid current, represented in rectangular coordinates in the generator terminal reference frame as `RE(ISORCE(I))` and `IM(ISORCE(I))`, via the phase rotation transformation *T*.

For most transient stability studies, the response of the plant to grid disturbances (short circuits) is of most interest. For these studies, the model calculates a virtual initial solar irradiance based on the plant's active power output in the power flow solution, and holds this irradiance constant through the simulation. However, the ability to simulate the response of the plant to irradiance transients is provided by variation of the model parameter PPrim.

In a similar manner, also the reactive power dispatch of the inverter is transferred from the power flow solution to the dynamic simulation, whereupon the power factor and the reactive power set-point can be altered during dynamic simulation, depending on the operating mode defined by parameter QVArMod, marked with an orange circle in the dyr file excerpt below.

In general, the three parameters

- WCtlHzMod (*P*(*f*) statics behavior),
- QVArMod (reactice power behavior) and
- FRTMod (dynamic grid support behavior)

define the operating mode of the solar inverter, whereas the remaining parameters (s. section 3.4) define the characteristics of these modes.

Invocation of the plant model in the PSS®E dyr input file, e.g. for simulations with a base frequency of 60 Hz is as follows (exemplary for version C1.41):

```
90104 'USRMDL' 1 'SMASC141' 1 1 0 120 40 200
                          0.123 0.9123 0.123 0.8 1.0 0.0 1.0 0.0 0.35
                          1.0 0.0 5.0 0.5 2.0
                          0.0 0.9 0.5 1.0 0.9 0.9
                          0.0 0.2 0.05 0.4
                          1.0 1.0
                          2.0 2.0 2.0 2.0
                          0.2 0.2 0.2 0.2 0.1 0.1
                          0.01 0.0 20.0 0.01 0.2 0.6 0.6
                          0.0 0.125 0.1
                          1.25 2.0 1.21 5.0 1.2 6.0 1.18 9.5 1.15 12.0
                          0.88 12.0 0.8 10.0 0.7 9.0 0.6 2.0 0.5 0.4
                          67.0 0.05 66.8 0.08 66.0 0.09 65.0 0.1 64.0 1.0 62.5 3.0
                          58.3 5.0 57.0 3.0 50.0 0.1 49.0 0.09 48.5 0.08 48.0 0.05
                          30.0 1.0 10.0 30.0 0.0 0.0 5.0 0.3
                          0.0 0.0 1.0 0.0
                          0.0 360.0 0.5 0.01 0.05 0.0 0.5 1.0
                          1.0 1.0
                          0.0 1.0
                          0.0 0.0 0.0 0.0 0.0 0.0/
/                         PPrim PWNom QVArNom PFLim PFPF PFPFExt QVArMod QoDEna QoDQMax
/                         VArCtlVol_Volref VArCtlVol_VolDB VArCtlVol_VArGra VArCtlVol_VAr ...
/                         PFPFExtStr PFPFStr PFWStr PFPFExtStop PFPFStop PFWStop
/                         WCtlHzMod PHzStr PHzStop PWGra
/                         WGra VArGra
/                         FRTMod FRTArGraNom FRTArGraNomHi FRTArGraNomLo
/                         FRTDbVolNomMax Reserved FRTDbVolNomMin Reserved FRTWRcvrTmF ...
/                         VArCmdFltTm FRTPreErrVEna FRTPreErrTm FRTSwOffTm FRTAmpQGra ...
/                         Reserved Reserved Reserved
/                         VCtl_Hi5Lim VCtl_Hi5LimTm ... VCtl_Hi1Lim VCtl_Hi1LimTm
/                         VCtl_Lo1Lim VCtl_Lo1LimTm ... VCtl_Lo5Limm VCtl_Lo5LimTm
/                         HzCtl_Hi6Lim HzCtl_Hi6LimTm ... HzCtl_Hi1Lim HzCtl_Hi1LimTm
```

```
/                        HzCtl_Lo1Lim HzCtl_Lo1LimTm ... HzCtl_Lo6Lim HzCtl_Lo6LimTm

/                        KPLL1 PLLFlag KPPLL2 KIPLL2 HzFltTm PLLFlag2 KPPLL3 KIPLL3

/                        Reserved Reserved GenTrpFlag PPrioEna

/                        SMASCSFlag DisChargeTm SOCIni KP_C KI_C CDB CNom FSCScale

/                        ChargePMax ChargePMin

/                        SMASCCONI QVArscale

/                        Reserved Reserved Reserved Reserved Reserved Reserved
```

Default parameters are defined in the following sections. SMA should be contacted in case of uncertainties regarding parameter changes.

In response, the model(s) report(s) with the following exemplary messages that identify the bus to which SMASC generator model(s) is/are connected, the model revision, the initial power factor, the initial excitation, and the initial active and reactive power dispatch, if available:

```
SMASC141 plant 1  at bus  90104 calling SMASC141 D Revision: 1.41 model for simulation of the SMA Sunny
Central solar inverters. SMA Solar Technology AG, Germany, 2018.

SMASC141 plant 1  at bus  90104 initialized with power factor:  0.998211

SMASC141 plant 1  at bus  90104 initialized with excitation:  0.000000

SMASC141 plant 1  at bus  90104 initialized with active power on system base (p.u.):  0.450002

SMASC141 plant 1  at bus  90104 initialized with active power on machine base (p.u.):  0.900004

SMASC141 plant 1  at bus  90104 initialized with reactive power on system base (p.u.):  0.026951

SMASC141 plant 1  at bus  90104 initialized with reactive power on machine base (p.u.):  0.053901

SMASC141 plant 1  at bus  90104 deployed in constant reactive power mode (QVArMod = 1).

SMASC141 plant 1  at bus  90104 deployed in DGS full mode (DGSMod = 1 / 2).
```

3.1 Islanding detection

The SMA Sunny Central CP/HE inverter series can operate in an islanding detection mode, in which isolated grids are reliably detected – whereupon the inverter disconnects from the grid. This behavior is NOT covered by the SMASC model.

3.2 Initialization

SMASC initializes the active power dispatch from the steady-state solution and adjusts all internal variables and states accordingly. Parameter PPrim is therefore ignored for the purpose of initialization, but can be altered during any dynamic simulation runs for provision of irradiation changes.

In the same way, the reactive power is transferred from the power flow solution to the dynamic simulation and, again, all internal variables and states are initialized in order to match the solution. Parameter QVArNom is

ignored during initialization but can be altered, right as PPrim, later in the simulation in Q set-point mode (QVArMod = 1).

Consequently, also parameters PF and PFExt are adjusted to match the steady-state and are tunable during simulation runs in power factor mode (QVArMod = 0) if desired.

In reactive power mode 2 (QVArMod = 2, i.e. power factor = *f*(*P*)) the user must take care to choose the reactive power in the steady-state solution in accordance to the parameter settings, otherwise the initialization of the dynamic simulation will fail.

In reactive power mode 3 (QVArMod = 3, i.e. *Q* = *f*(*U*)) the reference voltage for *Q*(*U*) voltage control is adjusted to meet the steady state. Therefore, the parameter VarCtlVol_Volref is ignored during initialization but can be altered later in the simulation.

When the VArCtlVol mode is used, please make sure to activate this mode only after initialization.

When SMASCSFlag is set to 2, the associated generator must initialize with zero active power.

3.3 Machine array variables

Machine array variables `PELEC`, `QELEC`, `ITERM`, `ETERM` and `ANGLE` are used in their conventional sense. Other variables are reassigned as follows:

`VOTHSG(I)`	Measured bus frequency
`VOEL(I)`	Initial irradiance (taken from the power flow solution)
`ECOMP(I)`	Inverter direct axis current command id
`VUEL(I)`	Inverter quadrature axis current command iq
`PMECH(I)`	Not used (from SMASC C1.36)
`EFD(I)`	Desired reactive power in p.u. (from plant control model)
`XADIFD(I)`	Desired active power in p.u. (from plant control model)
`ANGLE(I)`	Voltage angle of generator bus derived from PLL algorithm

3.4 Dyr file entry

The model's dyr file entry is as follows:

```
BusNum 'USRMDL' 1 'SMASC189' 1 1 1 200 60 300 ICON(M) CON(J) CON(J+1)
... CON(J+200)
```

3.5 Model parameters

In this section there is given a standard parameterization only. Please note that there exist individual parameter sets depending on the inverter type listed in Table 1. Please contact SMA in order to obtain the parameter set for the respective inverter type that has to be simulated in your study.

3.5.1 ICONs

ICON	Parameter	Description	Range	Default
M	*SlackBusNumber* ♬	Number of the slack bus if available; in other cases the SMASC bus number can be used	n/a	n/a

3.5.2 CONs

CON	Parameter	Description	Range	Default
J	*Pprim* ♬	Primary power (irradiation) in p.u. Note: the model initializes from the power flow solution. Hence, this parameter is ignored during initialization	0 ... 1	1
J+1	*PWNom* ♬	Maximum active power in p.u.; ignored at initialization	0 ... 1	1
J+2	*QVArNom* ♬	Reactive power set-point in p.u.; ignored at initialization	- sin(acos(PFLim)) ... sin(acos(PFLim))	0
J+3	PFLim ♬	Reactive power capability of the device; reactive power is calculated from PFLim by sin(acos(PFLim))	0.8 ... 1	0.8
J+4	*PFPF* ♬	Power factor set-point; ignored at initialization	PFLim ... 1	1
J+5	*PFPFExt* ♬	Excitation for power factor control; ignored at initialization	0: overexcited* 1: underexcited*	0
J+6	QVArMod ♬	Reactive power mode. Set to 1 when SMA's controller is used.	0: Power factor 1: Q set-point 2: Power factor(*P*) 3: Q(*U*)	0
J+7	QoDEna ♬	Activation of "Q on Demand" function	0: deactivated 1: activated[2]	0
J+8	QoDQMax ♬	Reative power limit for "Q on Demand" function	0 ... 1	0.3
J+9	VarCtlVol_Volref ♬	Reference voltage for Q(*U*) voltage control in p.u. Function obsolete – use parameters from J+119.	0.8 ... 1.2	1
J+10	VarCtlVol_VolDB ♬	Width for symmetric deadband for Q(*U*) voltage control in p.u. Function obsolete – use parameters from J+119.	0 ... 0.2	0

[2] For SunnyCentral PV inverter, FRTMod has to be set to "DGS limited", if QoDEna is activated.

J+11	VarCtlVol_VarGra ♬	Gradient for Q(*U*) statics ΔQ[p.u.]/Δ*U*[p.u.] Function obsolete – use parameters from J+119.	0 ... 25	5
J+12	VarCtlVol_VarMax ♬	Maximum absolute reactive power for Q(*U*) in p.u. Function obsolete – use parameters from J+119.	0 ... 0.6	0.5
J+13	VarCtlVol_VarTm ♬	First-order time constant for Q(*U*) dynamics in s Function obsolete – use parameters from J+119.	2 ... 60	2
J+14	PFPFExtStr ♬	Excitation of the start point for PF(*P*) control	0: overexcited* 1: underexcited*	0
J+15	PFPFStr ♬	Power factor of the start point for PF(*P*) control	PFLim ... 1	0.9
J+16	PFWStr ♬	Active power of the start point for PF(*P*) control in p.u.	0 ... 1	0.5
J+17	PFPFExtStop ♬	Excitation of the stop point for PF(*P*) control	0: overexcited* 1: underexcited*	1
J+18	PFPFStop ♬	Power factor of the stop point for PF(*P*) control	PFLim ... 1	0.9
J+19	PFWStop ♬	Active power of the stop point for PF(*P*) control in p.u.	0 ... 1	0.9
J+20	WctlHzMod ♬	*P*(*f*) droop mode. Deactivate if controller P(f) functionality is enabled.	0: deactivated 1: activated	0
J+21	PHzStr ♬	Grid frequency offset for starting power reduction in Hz	0 ... 5	0.2
J+22	PhzStop ♬	Grid frequency offset for power resetting in Hz	0 ... 5	0.05
J+23	PWGra ♬	Gradient for power reduction in p.u./Hz	0 ... 1	0.4
J+24	Wgra ♬	Gradient of changing active power set-point in p.u./s	0 ... 1	1.0
J+25	VarGra ♬	Gradient of changing reactive power set-point in p.u./s	0 ... 2	1.0
J+26	FRTMod ♬	Dynamic grid support mode; Note that the "DGS limited" behavior correlates to SC CP firmware release 13 while the "DGS full" behavior correlates to all SC types.	0: "DGS limited" 1: "DGS full" ("BDEW") 2: "DGS full" ("SDLWindV")	1
J+27	FRTArGraNom [3] ♬	Static reactive current feed-in factor $K = \Delta I_r / \Delta U$ ("BDEW curve")	0 ... 10	2

[3] Please note factors higher than 2 may not be advisable in weak grid scenarios.

J+28	FRTArGraNomHi [3]	Static reactive current feed-in factor $K = \Delta I_r / \Delta U$ for high voltages ("SDL-WindV" curve) Attention: this parameter is obsolete; please see parameters J+160 – J+171	0 ... 10	2
J+29	FRTArGraNomLo [3]	Static reactive current feed-in factor $K = \Delta I_r / \Delta U$ for low voltages ("SDL-WindV" curve) Attention: this parameter is obsolete; please see parameters J+160 – J+171	0 ... 10	2
J+30	FRTDbVolMax [4]	Positive dead-zone for "DGS full" in p.u. (this parameter is only used for FRT detection)	0 ... 1	0.1
J+31	FRTDbVolMaxHyst	Hysteresis for the positive dead-zone for "DGS full" in p.u. (this parameter is only used for FRT detection)	0 ... 1	0.08
J+32	FRTDbVolMin [4]	Negative dead-zone for "DGS full" in p.u. (this parameter is only used for FRT detection)	0 ... 1	0.1
J+33	FRTDbVolMinHyst	Hysteresis for the negative dead-zone for "DGS full" in p.u. (this parameter is only used for FRT detection)	0 ... 1	0.08
J+34	FRT_AmpDGra	Recovery time gradient of active power after dynamic grid support "DGS full" in p.u./s	0.01 ... 10	10.0
J+35	Reserved			1.0
J+36	*VarCmdFilTm*	Reactive current first-order delay block time constant in s; Please set this parameter to 0.01 if you are experiencing problems with oscillations in your simulations.	0 ... 0.1	0.0
J+37	FRT_VolFilMod	Defines DGS pre-error voltage calculation method. If deactivated, the DGS voltage deviation signal is calculated by $U/U_{nom} - 1$. If activated, the DGS voltage deviation signal is calculated by $U/U_{pre} - 1$, where U_{pre} is the	0: deactivated 1: activated	1

[4] Please note corresponding PPC model parameter FRTThrVolNomMax should be set to allow a wider dead-zone for DGS mode in the PPC.

		first-order lag low-pass filtered voltage *U*.		
J+38	FRT_VolDFilTm ♬	Time constant of first-order lag low-pass filter for pre-error voltage calculation	0 ... tbd	20.0
J+39	FRT_WaitTm ♬	FRT hold time – time for which FRT current characteristics is held after a fault has been cleared (voltage returned to deadband) in s. 0.02s is minimum in real device.	0.02 ... 10	0.5
J+40	FRT_AmpQGra ♬	Gradient of reactive current filter after FRT exit in p.u.	0.01 ... 100	0.02
J+41	*FRTSpkMtgLo* ♬	Lower threshold for FRT spike mitigation; set this parameter so that is it well above the voltage during the fault; see section 4.2.8. Set to zero if J+114 is set to 0.1.	0 ... 1- FRTDb-VolNomMin	0.8
J+42	*FRTSpkMtgHi* ♬	Upper threshold for FRT spike mitigation; set slightly higher than FRTSpkMtgLo; see section 4.2.8. Set to zero if J+114 is set to 0.1.	0 ... 1- FRTDb-VolNomMin	0.82
J+43	Reserved			0.0
J+44	Reserved			0.125
J+45	Reserved			0.1
J+46	VCtl_Hi5Lim ♬	Voltage limit for high voltage decoupling protection (*U5>*) in p.u.	s. Technical Information sheet	1.2
J+47	VCtl_Hi5LimTm ♬	Delay for high voltage decoupling protection (*U5>*) in s	s. Technical Information sheet	0.16
J+48	VCtl_Hi4Lim ♬	Voltage limit for high voltage decoupling protection (*U4>*) in p.u.	s. Technical Information sheet	1.16
J+49	VCtl_Hi4LimTm ♬	Delay for high voltage decoupling protection (*U4>*) in s	s. Technical Information sheet	0.6
J+50	VCtl_Hi3Lim ♬	Voltage limit for high voltage decopling protection (*U3>*) in p.u.	s. Technical Information sheet	1.14
J+51	VCtl_Hi3LimTm ♬	Delay for high voltage decoupling protection (*U3>*) in s	s. Technical Information sheet	1.0
J+52	VCtl_Hi2Lim ♬	Voltage limit for high voltage decopling protection (*U2>*) in p.u.	s. Technical Information sheet	1.12
J+53	VCtl_Hi2LimTm ♬	Delay for high voltage decoupling protection (*U2>*) in s	s. Technical Information sheet	2.0
J+54	VCtl_Hi1Lim ♬	Voltage limit for high voltage decopling protection (*U1>*) in p.u.	s. Technical Information sheet	1.1

J+55	VCtl_Hi1LimTm ♬	Delay for high voltage decoupling protection (*U1*>) in s	s. Technical Information sheet	5.0
J+56	VCtl_Lo1Lim ♬	Voltage limit for low voltage decoupling protection (*U1*<) in p.u.	s. Technical Information sheet	0.9
J+57	VCtl_Lo1LimTm ♬	Delay for low voltage decoupling protection (*U1*<) in s	s. Technical Information sheet	5.0
J+58	VCtl_Lo2Lim ♬	Voltage limit for low voltage decoupling protection (*U2*<) in p.u.	s. Technical Information sheet	0.8
J+59	VCtl_Lo2LimTm ♬	Delay for low voltage decoupling protection (*U2*<) in s	s. Technical Information sheet	2.0
J+60	VCtl_Lo3Lim ♬	Voltage limit for low voltage decoupling protection (*U3*<) in p.u.	s. Technical Information sheet	0.7
J+61	VCtl_Lo3LimTm ♬	Delay for low voltage decoupling protection (*U3*<) in s	s. Technical Information sheet	1.0
J+62	VCtl_Lo4Lim ♬	Voltage limit for low voltage decoupling protection (*U4*<) in p.u.	s. Technical Information sheet	0.6
J+63	VCtl_Lo4LimTm ♬	Delay for low voltage decoupling protection (*U3*<) in s	s. Technical Information sheet	0.6
J+64	VCtl_Lo5Lim ♬	Voltage limit for low voltage decoupling protection (*U5*<) in p.u.	s. Technical Information sheet	0.2
J+65	VCtl_Lo5LimTm ♬	Delay for low voltage decoupling protection (*U5*<) in s	s. Technical Information sheet	0.16
J+66	HzCtl_Hi6Lim ♬	Frequency limit for high frequency decoupling protection (*f6*>) in Hz	s. Technical Information sheet	65.0
J+67	HzCtl_Hi6LimTm ♬	Delay for high frequency decoupling protection (*f6*>) in s	s. Technical Information sheet	0.1
J+68	HzCtl_Hi5Lim ♬	Frequency limit for high frequency decoupling protection (*f5*>) in Hz	s. Technical Information sheet	64.0
J+69	HzCtl_Hi5LimTm ♬	Delay for high frequency decoupling protection (*f5*>) in s	s. Technical Information sheet	0.2
J+70	HzCtl_Hi4Lim ♬	Frequency limit for high frequency decoupling protection (*f4*>) in Hz	s. Technical Information sheet	63.5
J+71	HzCtl_Hi4LimTm ♬	Delay for high frequency decoupling protection (*f4*>) in s	s. Technical Information sheet	0.4
J+72	HzCtl_Hi3Lim ♬	Frequency limit for high frequency decoupling protection (*f3*>) in Hz	s. Technical Information sheet	62.0
J+73	HzCtl_Hi3LimTm ♬	Delay for high frequency decoupling protection (*f3*>) in s	s. Technical Information sheet	1.0
J+74	HzCtl_Hi2im ♬	Frequency limit for high frequency decoupling protection (*f2*>) in Hz	s. Technical Information sheet	61.5
J+75	HzCtl_Hi2LimTm ♬	Delay for high frequency decoupling protection (*f2*>) in s	s. Technical Information sheet	2.0

J+76	HzCtl_Hi1Lim ♬	Frequency limit for high frequency decoupling protection (*f1*>) in Hz	s. Technical Information sheet	61.0
J+77	HzCtl_Hi1LimTm ♬	Delay for high frequency decoupling protection (*f1*>) in s	s. Technical Information sheet	5.0
J+78	HzCtl_Lo1Lim ♬	Frequency limit for low frequency decoupling protection (*f1*<) in Hz	s. Technical Information sheet	59.0
J+79	HzCtl_Lo1LimTm ♬	Delay for low frequency decoupling protection (*f1*<) in s	s. Technical Information sheet	5.0
J+80	HzCtl_Lo2Lim ♬	Frequency limit for low frequency decoupling protection (*f2*<) in Hz	s. Technical Information sheet	58.0
J+81	HzCtl_Lo2LimTm ♬	Delay for low frequency decoupling protection (*f2*<) in s	s. Technical Information sheet	2.0
J+82	HzCtl_Lo3Lim ♬	Frequency limit for low frequency decoupling protection (*f3*<) in Hz	s. Technical Information sheet	57.5
J+83	HzCtl_Lo3LimTm ♬	Delay for low frequency decoupling protection (*f3*<) in s	s. Technical Information sheet	1.0
J+84	HzCtl_Lo4Lim ♬	Frequency limit for low frequency decoupling protection (*f4*<) in Hz	s. Technical Information sheet	57.0
J+85	HzCtl_Lo4LimTm ♬	Delay for low frequency decoupling protection (*f4*<) in s	s. Technical Information sheet	0.8
J+86	HzCtl_Lo5im ♬	Frequency limit for low frequency decoupling protection (*f5*<) in Hz	s. Technical Information sheet	56.0
J+87	HzCtl_Lo5LimTm ♬	Delay for low frequency decoupling protection (*f5*<) in s	s. Technical Information sheet	0.2
J+88	HzCtl_Lo6Lim ♬	Frequency limit for low frequency decoupling protection (*f6*<>) in Hz	s. Technical Information sheet	55.0
J+89	HzCtl_Lo6LimTm ♬	Delay for low frequency decoupling protection (*f16*<) in s	s. Technical Information sheet	0.1
J+90	*KPLL1* ♬	First-order low-pass filter time delay (valid for PLLFlag = 0)		30
J+91	*PLLFlag* ♬	Determines whether inverter PLL is modeled by a simple first-order delay (0) with parameter KPLL1, or by a PLL control loop (1) with parameters KPPLL2 and KIPLL2. For experimental studies the PLL can also be disabled: PLLFlag = 2: angle is directly obtained from PSS®E BUSDAT routine PLLFlag = 3: angle is directly obtained from measurement of the complex bus voltage `VOLT(IB)`	0 ... 10	1

		PLLFlag = 4: same as PLLFlag =1, but machine variable `ANGLE(I)` is kept/wrapped in interval [-90; +90] degrees PLLFlag = 5: same as PLLFlag =1, but machine variable `ANGLE(I)` is kept/wrapped in interval [0; +180] degrees PLLFlag = 6: same as PLLFlag =1, but machine variable `ANGLE(I)` is output in radians (unwrapped) PLLFlag = 7: same as PLLFlag =1, but machine variable `ANGLE(I)` is set to 0.0 PLLFlag = 8: same as PLLFlag =1, but machine variable `ANGLE(I)` is obtained from BUSDAT routine and output in degrees (wrapped) PLLFlag = 9: same as PLLFlag =1, but machine variable `ANGLE(I)` is obtained from BUSDAT routine and output in radians (wrapped) PLLFlag = 10: Sunny Central PLL algorithm		
J+92	*KPPLL2* ♬	PLL 2 control loop control gain (valid for PLLFlag = 1)		50 or 100
J+93	*KIPLL2* ♬	PLL 2 control loop integration gain (valid for PLLFlag = 1)		30
J+94	*HzFltTm* ♬	Time constant of first-order lag frequency filter; if this parameter is > 0 then the frequency is determined by filtering the system frequency (1.0 + BSFREQ(IB))*f) with this filter, where f = 50 or 60. This parameter is overwritten by PLLFlag2.	0 ... 10	0
J+95	*PLLFlag2* ♬	Activation of second PLL model for frequency measurement	0: deactivated 1: activated	1
J+96	*KPPLL3* ♬	PLL 2 control loop control gain (valid for PLLFlag2 = 1)		5
J+97	*KIPLL3* ♬	PLL 2 control loop integration gain (valid for PLLFlag2 = 1)		0.3

J+98	Reserved	Should be set to 0. If set to values greater than 0, this parameter defines the number of a signal debug text file (see CON(J+99), too).		0
J+99	Reserved ♬	If set to values greater than 0, some model information is logged when the model is called by PSS®E; if set 0, this is suppressed. At the same time, this parameter specifies the time span with which a signal debug text file is written (see CON(J+98), too).		0
J+100	*GenTrpFlag* ♬	Determines whether the generator is tripped through the GENTRP command (1) or not (0). If GENTRPFLAG = 0, then only the current injection commands for direct and quadrature current are set to zero, but the generator is not tripped using GENTRP. If GENTRPFLAG = 1, then the generator is tripped using GENTRP.	0: deactivated 1: activated	0
J+101	PprioEna ♬	Activation of active power priority switch. Reactive power priority is recommended.	0: deactivated 1: activated	0
J+102	*SMASCSFlag* ♬	Activation of storage inverter functionality; set to 1 for simulation of storage inverters; set to 2 for simulation of combined PV/storage setup; set to 3 for simulation of DCDC coupled PV inverters	0: deactivated 1: storage-only 2: PV/storage 3: DCDC coupled	0
J+103	*DischargeTm* ♬	Battery discharge time in s; see section 4.7.	0 ... tbd	9999
J+104	*SOCIni* ♬	Battery state of charge at initialization in p.u.	0 ... 1	0.7
J+105	*KP_C* ♬	Charge PI controller proportional gain	0 ... tbd	1
J+106	*KI_C* ♬	Charge PI controller integral gain	0 ... tbd	0.001
J+107	*CDB* ♬	Charge controller deadband	0 ... 1	0
J+108	*Cnom* ♬	Charge controller set-point	0 ... 1	0.7
J+109	*FSCScale* ♬	Scaling of charge pilot control signal	tbd	1
J+110	*ChargePMax* ♬	Maximum charge power of the storage inverter	0 ... 1	1

J+111	*ChargePMin* ♬	Minimum charge power of the storage inverter	0 ... 1	1
J+112	*PC_BUS*♬	Set to the bus number with which the controlling SMAPPC/SMAHYC model is associated.	n/a	n/a
J+113	*QVArScale* ♬	Multiplication factor for Iq set-point signal for plant control response time correction. 0.6 is a recommended setting for ease of translating to PSCAD model.	Tbd	0.6
J+114	*VREps*	Spike mitigation based on speed of signal change. 0.1 – enabled, 1 – disabled. Set to 1 if J+41 and J+42 are in use (not set to zero).	n/a	0.1
J+115	FRT_AmpDLim ♬	During FRT mode, id is limited to FRT_AmpDLim	0 ... 2	2
J+116	FRT_AmpQLim ♬	During FRT mode, iq is limited to FRT_AmpQLim	0 ... 2	2
J+117	Reserved	n/a	n/a	n/a
J+118	Reserved	n/a	n/a	n/a
J+119	GriMngInvVArMod ♬	Disable (0)/Enable (1) AC voltage-dependent reactive power control (VarCtlVol mode)	0 ... 1	0
J+120	VarCtlVolLoVolRef3 ♬	Low voltage reference point 3 in p.u.	0 ... 2	0.85
J+121	VarCtlVolLoVolRef2 ♬	Low voltage reference point 2 in p.u.	0 ... 2	0.92
J+122	VarCtlVol LoVolRef1HiVolRef1 ♬	Low/high voltage reference point 1 in p.u.	0 ... 2	1.0
J+123	VarCtlVolHiVolRef2 ♬	High voltage reference point 2 in p.u.	0 ... 2	1.08
J+124	VarCtlVolHiVolRef3 ♬	High voltage reference point 3 in p.u.	0 ... 2	1.15
J+125	VarCtlVolLoGra3 ♬	Low voltage gradient 3 in p.u./p.u. ¥	0 ... 100	2.0
J+126	VarCtlVolLoGra2 ♬	Low voltage gradient 2 in p.u./p.u. ¥	0 ... 100	0.1
J+127	VarCtlVolLoGra1 ♬	Low voltage gradient 1 in p.u./p.u. ¥	0 ... 100	2.0
J+128	VarCtlVolHiGra1 ♬	High voltage gradient 1 in p.u./p.u. ¥	0 ... 100	1.5
J+129	VarCtlVolHiGra2 ♬	High voltage gradient 2 in p.u./p.u. ¥	0 ... 100	1.0
J+130	VarCtlVolHiGra3 ♬	High voltage gradient 3 in p.u./p.u. ¥	0 ... 100	2.0
J+131	VarCtlVolVArSptFilTm ♬	Filter (first-order delay) time constant in s	0 ... 100	0.5
J+132	VolNomSpt ♬	Voltage set-point in p.u. Keep at 1.0 if used. Not possible to change from 1 in PSCAD model.	0 ... 2	1.0

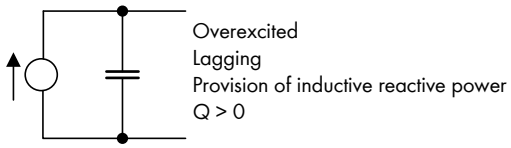
J+133	Frt_AmpQFilTm ♬	Time constant of the first-order lag (PT1) filter, which is used for determining the FRT pre-fault reactive current (to which the FRT fault reactive current from the FRT characteristics is added, to give the total FRT reactive current)	0 ... 1000	20.0
J+134	IniSchemeFlag ♬	Defines the methodology of active power initialization. 0: Active power from load flow solution is assumed to be the maximum power available by irradiation (DC power); for to increase the output above this value, parameter Pprim has to be increased 1: Active power from load flow solution is assumed to represent the power curtailment while the DC power is assumed to be at maximum	0 ... 1	0.0
J+135	VArCtlVolVolNomSptMod ♬	Source of voltage set-point for VarCtlVol functionality: 0: VolNomSpt (J+132) 1: filtered terminal voltage and initialize with VArCtlVol_VolNomSptInit 2: filtered terminal voltage and initialize with measured terminal voltage (1 or 2 is recommended when using function to increase stability.)	0 ... 2	0.0
J+136	VarCtlVolVolFilTm ♬	Terminal voltage filter time constant	0 ... tbd	0.5
J+137	VarCtlVolVolMin ♬	Lower terminal voltage limitation	0 ... 2	0.9
J+138	VarCtlVolVolMax ♬	Upper terminal voltage limitation	0 ... 2	1.1
J+139	PwrCtl_VolDQFilTm	Time constant in s for filtering the voltage for active power control; if set to 0, a standard value of 0.46 s is applied.	0 ... tbd	0.46
J+140	Reserved			
J+141	Reserved			
J+142	Reserved			
J+143	Pll_Inv_Tlength ♬	Time length for calculation of settling space in s. J+91 should be set to 10 for use with parameters from J+143 to J+157.	0.001...1.0	0.01

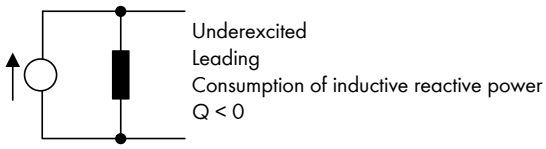
J+144	Pll_Inv_Tsample ♬	Sample time of control algorithm in MATLAB/Simulink in s	1e-4... 10e-4	1/6000
J+145	Pll_Inv_TimeStep ♬	Time step of simulation in s	0.001...0.02	0.001
J+146	Pll_Inv_ HzFilOff2On_Vol ♬	Voltage for transition from HzFilOff to HzFilOn in p.u.	0...1	0.6
J+147	Pll_Inv_ HzFilOff2On_NomSum ♬	Moving average of voltage from HzFilOff to HzFilOn in p.u. Keep at 0.5 for best match with PSCAD model.	0... 10000	0.5
J+148	Pll_Inv_ HzFilOn2Off_NomSum ♬	Moving average of voltage from HzFilOn to HzFilOff in p.u.. Keep at 80 for best match with PSCAD model.	0... 10000	80
J+149	Pll_Inv_ HzFilOn2Wt_Vol ♬	Voltage for transition from HzFilOn to HzFilWait in p.u.	0...1	0.75
J+150	Pll_Inv_ HzFilWt2On_Vol ♬	Voltage for transition from HzFilWait to HzFilOn in p.u.	0...1	0.65
J+151	Pll_Inv_SetTm ♬	Settling time used for PI control in s. Keep at 0.05 for best match with PSCAD model.	0.001... 1.0	0.05
J+152	Pll_Inv_DmpRto ♬	Damping ratio used for PI control	0...100	2.0
J+153	Pll_Inv_VolDQFilTm ♬	Voltage dq-axis filter time constant in s. Keep at 0.01 for best match with PSCAD model.	0.001...0.01	0.01
J+154	Pll_Inv_VolDQRtg ♬	Nominal voltage in V	300...600	600
J+155	Pll_Inv_Fn ♬	Nominal frequency in Hz	50/60	50
J+156	Pll_Inv_HzGraLim ♬	Frequency gradient limiter in Hz/s	0...10	5.0
J+157	Pll_Inv_HzFilTm ♬	Frequency filter time constant. Set to 0.1 for best match with PSCAD model.	0.001...0.1	0.1
J+158	Reserved	n/a	n/a	n/a
J+159	Reserved	n/a	n/a	n/a
J+160	Frt_LoGra1 ♬	Please see documentation of the Sunny Central PSCAD model.	n/a	n/a
J+161	Frt_LoGra2 ♬	""	n/a	n/a
J+162	Frt_LoGra1 ♬	""	n/a	n/a
J+163	Frt_LoVolRef1 ♬	""	n/a	n/a
J+164	Frt_LoVolRef2 ♬	""	n/a	n/a
J+165	Frt_LoVolRef3 ♬	""	n/a	n/a
J+166	Frt_HiGra1 ♬	""	n/a	n/a
J+167	Frt_HiGra2 ♬	""	n/a	n/a
J+168	Frt_HiGra3 ♬	""	n/a	n/a
J+169	Frt_HiVolRef1 ♬	""	n/a	n/a

J+170	Frt_HiVolRef2 ♬	""	n/a	n/a
J+171	Frt_HiVolRef3 ♬	""	n/a	n/a
J+172	WFilMod ♬	Activation of PT1 filter for active power set-point	0 ... 1	0
J+173	VarFilMod ♬	Activation of PT1 filter for reactive power set-point	0 ... 1	0
J+174	WFilTm ♬	Time constant of PT1 filter for active power set-point	n/a	n/a
J+175	VarFilTm ♬	Time constant of PT1 filter for reactive power set-point	n/a	n/a
J+176	AmpScl ♬	Allows for correction of the current maximum	0.9 ... 1.1	1.0
J+177	DCDCBatSize ♬	Battery size of DCDC coupled inverter in pu on MBASE		
J+178	Reserved			
J+179	WSptMin	WSptMin of DCDC coupled inverter interface		
J+180	BatWSptMax	BatWSptMax of DCDC coupled inverter interface		
J+181	BatWSptMin	BatWSptMin of DCDC coupled inverter interface		
J+182	Frt_AmpQFilTmInit-Mode ♬	Frt_AmpQFilTm initialization at FRT entry (1) or exit (2), or both (3); 0 is equivalent to previous operation	0, 1, 2, 3	
J+183	Frt_AmpQFilTmInit ♬	To this value Frt_AmpQFilTm is initialized		
J+184	SpikeVoltChgCyc ♬	For time period of SpikeVoltChgCyc cycles the voltage used for FRT characteristics is the measured voltage instead of the filtered voltage	0 ... 5	2
J+185	SpikeCurrMode ♬	Injected current during spike mitigation is either zero (0.0), or pre-fault reactive current (1.0)	0.0 or 1.0	0.0
J+186	VArCtlVol_ VolNomSptInit ♬	Please see VArCtlVolVolNomSptMod	n/a	1.0
J+187	IdMinPV	Please set IdMinPV to Paux / Pnom, where Paux - inverter auxiliary/standby power consumption and Pnom - nominal inverter output power, e.g., IdMinPV = 2e03 W / 4e06 W = 0.0005	n/a	0.0005
J+188	Reserved	n/a	n/a	n/a

...				
J+199	Reserved	n/a	n/a	n/a

* The term "overexcited" corresponds to the often used term "lagging". Both means provision of inductive reactive power (Q >0), whereas the term "underexcited" corresponds to the often used term "leading". Both means consumption of inductive reactive power (Q < 0).





♫ Parameters with this symbol can be tuned by the user.
¥ Must be a positive number; internally converted into a gradient with decreasing slope.
Parameters in *italic* are no device parameters, but are needed for simulation purposes or are set-points.

3.5.3 VARs

VAR	Description
L	Generator status (0 = on line, 1 = off line)
L+1	Base frequency in Hz
L+2	Initial active power on plant base in p.u.
L+3	Initial terminal bus voltage in p.u.
L+4	Memory for PLL
L+5	Counter for phase unwrapping
L+6	Reserved for test
L+7	Id command in non-FRT situations
L+8	Apparent current limit
L+9	Iq command before dynamic limitation block
L+10	Internal auxiliary signal
L+11	Internal signal (delayed id command after dynamic limitation block)
L+12	Measured voltage in p.u.
L+13	Internal auxiliary signal
L+14	Timer memory for FRT detection flip-flop
L+15	Internal auxiliary signal
L+16	Measured bus frequency in Hz
L+17	Internal auxiliary signal
L+18	Internal auxiliary signal
L+19	Internal auxiliary signal
L+20	Internal auxiliary signal
L+21	Timer memory for picdro relay VCtl_Hi2
L+22	Timer memory for picdro relay VCtl_Hi1
L+23	Internal auxiliary signal
L+24	Timer memory for picdro relay VCtl_Hi1

L+25	Timer memory for picdro relay VCtl_Hi2
L+26	Internal auxiliary signal
L+27	Timer memory for picdro relay HzCtl_Hi2
L+28	Timer memory for picdro relay HzCtl_Hi1
L+29	Internal auxiliary signal
L+30	Timer memory for picdro relay HzCtl_Lo1
L+31	Timer memory for picdro relay HzCtl_Lo2
L+32	Internal auxiliary signal
L+33	Internal auxiliary signal
L+34	Internal auxiliary signal
L+35	Internal auxiliary signal
L+36	Internal auxiliary signal
L+37	Internal auxiliary signal
L+38	Internal auxiliary signal
L+39	Internal auxiliary signal
L+40	Id command
L+41	Internal auxiliary signal
L+42	Timer memory for FRT situation handling
L+43	Memory for reactive power when FRT is entered
L+44	Internal auxiliary signal
L+45	Internal auxiliary signal
L+46	Internal auxiliary signal
L+47	Relay state memory for picdro relay VCtl_Hi2
L+48	Relay state memory for picdro relay VCtl_Hi1
L+49	Internal auxiliary signal
L+50	Relay state memory for picdro relay VCtl_Lo1
L+51	Relay state memory for picdro relay VCtl_Lo2
L+52	Internal auxiliary signal
L+53	Relay state memory for picdro relay HzCtl_Hi2
L+54	Relay state memory for picdro relay HzCtl_Hi1
L+55	Internal auxiliary signal
L+56	Relay state memory for picdro relay HzCtl_Lo1
L+57	Relay state memory for picdro relay HzCtl_Lo2
L+58	Internal auxiliary signal
L+59	State memory for FRT situation handling
L+60	State memory for FRT detection including hold time
L+61	Internal auxiliary signal
L+62	Internal auxiliary signal
L+63	Internal auxiliary signal
L+64	Flag for signaling if inverter is to be tripped permanently
L+65	Internal auxiliary signal

L+66	Internal auxiliary signal
L+67	Internal auxiliary signal
L+68	Internal auxiliary signal
L+69	Internal auxiliary signal
L+70	Internal auxiliary signal
L+71	Internal auxiliary signal
L+72	Internal auxiliary signal
L+73	VarCtlVol_Volref at time of model initialization
L+74	VarCtlVol_Volref back-tracked from steady-state solution
L+75	Internal auxiliary signal
L+76	Timer memory for picdro relay VCtl_Hi3
L+77	Timer memory for picdro relay VCtl_Lo3
L+78	Timer memory for picdro relay HzCtl_Hi3
L+79	Timer memory for picdro relay HzCtl_Lo3
L+80	Relay state memory for picdro relay VCtl_Hi3
L+81	Relay state memory for picdro relay VCtl_Lo3
L+82	Relay state memory for picdro relay HzCtl_Hi3
L+83	Relay state memory for picdro relay HzCtl_Lo3
L+84	PLLdphi1
L+85	PLLom1
L+86	PLLsinphi1
L+87	PLLcosphi1
L+88	PPrim at time of model initialization
L+89	QVArNom at time of model initialization
L+90	Reactive power set-point on machine base calculated from steady-state solution
L+91	PFPF at time of model initialization
L+92	Power factor set-point calculated from steady-state solution
L+93	PFExt at time of model initialization
L+94	Power factor excitation set-point calculated from steady-state solution
L+95	Initialization flag
L+96	PWNom at time of model initialization
L+97	Internal auxiliary signal
L+98	Internal auxiliary signal
L+99	Internal auxiliary signal
L+100	Internal auxiliary signal
L+101	Internal auxiliary signal
L+102	FRT detection flag (for spike mitigation logic); see also VAR(L+163)
L+103	Simulation step counter
L+104	Internal auxiliary signal
L+105	Internal auxiliary signal
L+106	State memory for FRTWaitTimer flip-flop

L+107	Timer memory for FRTWaitTimer flip-flop
L+108	Timer memory for FRTWaitTimer flip-flop
L+109	State memory for FRTPartialWaitId flip-flop
L+110	Timer memory for FRTPartialWaitId flip-flop
L+111	Timer memory for FRTPartialWaitId flip-flop
L+112	State memory for FRTPartialRampIq flip-flop
L+113	Timer memory for FRTPartialRampIq flip-flop
L+114	Timer memory for FRTPartialRampIq flip-flop
L+115	Internal signal LVRTi
L+116	Internal signal HVRT
L+117	Internal signal LVRT
L+118	Internal signal LVRT release state
L+119	Timer memory for LVRT detection flip-flop
L+120	Internal signal LVRT + FRTSwOffTm
L+121	Internal signal HVRT + FRTSwOffTm
L+122	Steady-state reactive current component
L+123	File written flag for SMASCCONi.txt
L+124	Reserved
L+125	Reserved
L+126	Not used
L+127	PLLdphi2
L+128	PLLom2
L+129	PLLsinphi2
L+130	PLLcosphi2
L+131	State for flip-flop FrtQRampActive
L+132	Internal signal reactive current filter after FRT exit: PsQR_AmpPsQ_SptOut
L+133	Internal signal reactive current filter after FRT exit
L+134	PLLFmeas
L+135	ROCOF PLL
L+136	PLLFmeas2
L+137	ROCOF PLL2
L+138	Voltage as measured by ETERM(I) in mode 3
L+139	Memory for active power when FRT is entered
L+140	Active power set-point for storage inverter from charge controller
L+141	Battery state of charge
L+142	Effective (used) id set-point
L+143	Timer memory for picdro relay VCtl_Hi4
L+144	Relay state memory for picdro relay VCtl_Hi4
L+145	Timer memory for picdro relay VCtl_Hi5
L+146	Relay state memory for picdro relay VCtl_Hi5
L+147	Timer memory for picdro relay VCtl_Lo4

L+148	Relay state memory for picdro relay VCtl_Lo4
L+149	Timer memory for picdro relay VCtl_Lo5
L+150	Relay state memory for picdro relay VCtl_Lo5
L+151	Timer memory for picdro relay HzCtl_Hi4
L+152	Relay state memory for picdro relay HzCtl_Hi4
L+153	Timer memory for picdro relay HzCtl_Hi5
L+154	Relay state memory for picdro relay HzCtl_Hi5
L+155	Timer memory for picdro relay HzCtl_Hi6
L+156	Relay state memory for picdro relay HzCtl_Hi6
L+157	Timer memory for picdro relay HzCtl_Lo4
L+158	Relay state memory for picdro relay HzCtl_Lo4
L+159	Timer memory for picdro relay HzCtl_Lo5
L+160	Relay state memory for picdro relay HzCtl_Lo5
L+161	Timer memory for picdro relay HzCtl_Lo6
L+162	Relay state memory for picdro relay HzCtl_Lo6
L+163	Internal signal FRT detection: Frt_State
L+164	Internal signal FRT detection: FilEnable_Int
L+165	Internal signal FRT detection: Amp_PsQ
L+166	Internal signal FRT detection: Amp_PsQ_Frt / Amp_PsQ_Fil_1
L+167	Internal signal FRT detection: Vol_Ps_Fil_1
L+168	Internal signal FRT detection: State_LVRT_wait
L+169	Internal signal FRT detection: State_HVRT_wait
L+170	Internal signal FRT detection: State_LVRT
L+171	Internal signal FRT detection: State_HVRT
L+172	Internal signal: PsQR_Frt_Stt
L+173	Reserved
L+174	Active power control value coming from SMAPPC model
L+175	Reactive power control value coming from SMAPPC model
L+176	MGC bus number written flag
L+177	Internal signal active current recovery function: Amp_PsD_Spt_FrtMin
L+178	Internal signal active current recovery function: Amp_PsD_Spt_Ramp_Int1
L+179	Internal signal active current recovery function: AmpSpt_Dif
L+180	Internal signal active current recovery function: RampEndDetection
L+181	Internal signal active current recovery function: FrtRampActive
L+182	Reserved
L+183	Reserved
L+184	Reserved
L+185	Active power flow direction
L+186	LVRT detected flag
L+187	HVRT detected flag
L+188	Reserved

L+189	Reserved
L+190	Test variable for VArCtlVol function (Output of the characteristic curve over time; to be evaluated between 0.0 and 2.0 seconds)
L+191	Iq base component
L+192	Iq fault component
L+193	Reserved
...	Reserved
L+199	Angle for current injection routine in degrees
L+200	Reserved
L+201	Moving Average Filter
...	...
L+250	Moving Average Filter
L+251	PllSubStt
L+252	RevPLL_block
L+253	RevPLL_count
L+254	RevPLL Phi
L+255	Reserved
...	
L+259	Reserved

3.5.4 STATEs

STATE	**Description**
K	PLL integrator
K+1	PT1 filter for active current recovery after FRT situations
K+2	Filter for replicating FRT current characteristics
K+3	Filter for replicating FRT current characteristics
K+4	PT1 filter for power factor limitation
K+5	Voltage filter for FRT detection
K+6	Power factor ramp
K+7	Active current ramp
K+8	Reactive current ramp
K+9	Q(*U*) dynamics PT1 filter
K+10	Irradiation PT1 filter
K+11	Reserved for test
K+12	PLL filter integrator
K+13	PLL VCO integrator
K+14	Reactive current PT1 filter
K+15	Pre-fault reactive current PT1 filter (time constant = 20 s)
K+16	Frequency measurement PT1 filter
K+17	PLL filter integrator 2

K+18	PLL VCO integrator 2
K+19	Flip-flop for reactive current ramp after FRT exit
K+20	State of charge (storage inverter option)
K+21	Voltage filter for id/iq generation
K+22	Charge controller integrator output in p.u. on MBASE
K+23	q-axis voltage calculation filter for improving initialization
K+24	Reserved
K+25	FRT Detection algorithm state
K+26	FRT Detection algorithm state
K+27	FRT Detection algorithm state
K+28	FRT Detection algorithm state
K+29	FRT Detection algorithm state
K+30	FRT Detection algorithm state
K+31	State of active current recovery function
K+32	Voltage filter for improved network solution
K+33	Low-pass filter for power to current set-point calculation
K+34	Low-pass filter for VArCtlVol function output (this portion is added to the Iq set-point)
K+35	Low-pass filter for VArCtlVolFilTm function
K+36	Reserved
...	Reserved
K+39	Reserved
K+40	Revised PLL x / phitrack
K+41	Revised PLL x_Pll_Inv / Modified Integrator
K+42	Revised PLL x_Pll_Inv_VolQFilTm / PT1 VolPsQ
K+43	Revised PLL x_Pll_Inv_VolDFilTm / PT1 VolPsD
K+44	Revised PLL / RevPLL_HzFil
K+45	Revised PLL dsindt
K+46	Revised PLL dcosdt
K+47	Revised PLL x_Pll_Inv_Ki
K+48	Revised PLL timer_SM22_SM24
K+49	Revised PLL timer_SM23_SM24
K+50	Revised PLL timer_SM24_SM21
K+51	Revised PLL xspace
K+52	Reserved
...	Reserved
K+59	Reserved

4 Functions for dynamic simulation

This chapter describes the functions implemented in the SMA inverter model relevant for transient stability studies.

4.1 Active power control

4.1.1 Frequency-dependent active power *P*(*f*)

This function provides frequency-dependent active power reduction in case of frequencies greater than the system frequency.

Default parameter settings for activation:

	WCtlHzMod	*P*(*f*) droop mode	0: deactivated 1: activated	1
	PHzStr	Grid frequency offset for starting power reduction in Hz	0 ... 5	0.2
	PHzStop	Grid frequency offset for power resetting in Hz	0 ... 5	0.05
	PWGra	Gradient for power reduction in %/Hz	0 ... 100	40

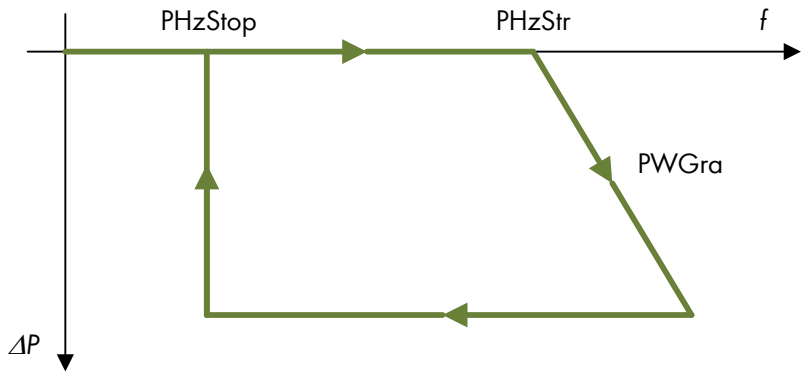


Figure 5: Active power change vs. frequency if *P*(*f*) mode activated.

Please note the set-point for the active power is generated by calculating the minimum of the output of the *P*(*f*) module and the external active power set-point module (PWNom). The resulting signal is routed through the "WGra" module which limits the rate-of-change to plus/minus WGra (CON(J+24)). If the inverter is used with a plant controller, the *P*(*f*) function is usually done by the plant controller.

4.2 Reactive power control

4.2.1 Reactive power provision by power factor set-point

This function provides provision of reactive power depending on a user-defined power factor.

4.2.2 Reactive power provision by Q set-point

This function provides provision of reactive power depending on a user-defined reactive power set-point.

4.2.3 Voltage-dependent reactive power Q(*U*)

Please do not confuse this function with the voltage-dependent reactive power control (VArCtlVol) mode (described in section 4.2.5).

This function provides reactive power provision as a function of voltage *U*.

Default parameter settings:

	VArCtlVol_VArTm	First-order delay time constant for Q(*U*) dynamic in s	2 ... 60	2
	QVArMod	Reactive power mode	0: Power factor 1: Q set-point 2: Power factor(*P*) 3: Q(*U*)	3
	VArCtlVol_Volref	Reference voltage for Q(*U*) voltage control in p.u.	0.8 ... 1.2	1
	VArCtlVol_VolDB	Width for symmetric deadband for Q(*U*) voltage control in p.u.	0 ... 0.2	0
	VArCtlVol_VArGra	Gradient for Q(*U*) statics ΔQ[p.u.]/Δ*U*[p.u.]	0 ... 25	5
	VArCtlVol_VArMax	Maximum absolute reactive power for Q(*U*) in p.u.	0 ... sin(acos(PFLim))	0.6

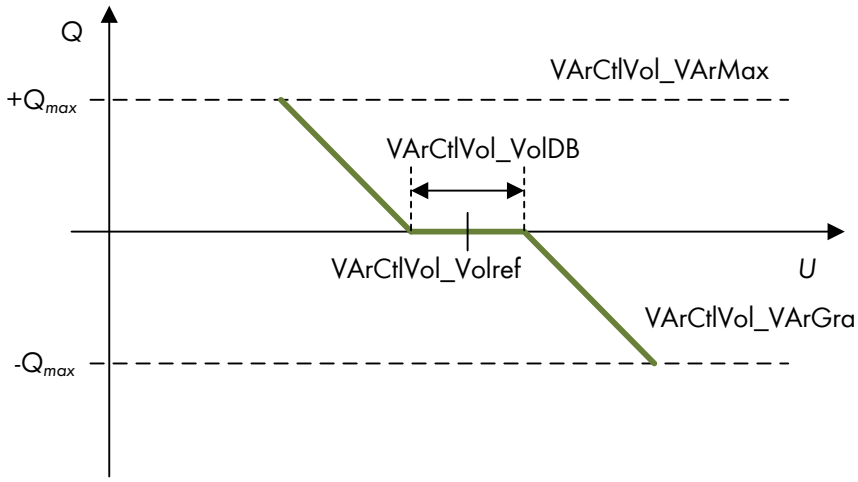


Figure 6: Example for Q(*U*) statics.

4.2.3.1 Initialization

In reactive power mode 3 (QVArMod = 3, i.e. Q = *f*(*U*)) the reference voltage for Q(*U*) voltage control is adjusted to meet the steady state. Therefore, the parameter VArCtlVol_Volref is ignored during initialization but can be altered later in the simulation.

4.2.4 Active power-dependent power factor cosφ(*P*)

This function provides automatic adjustment of the power factor as a function of active power.

Default parameter settings:

	QVArMod	Reactive power mode	0: Power factor 1: Q set-point 2: Power factor(*P*) 3: Q(*U*)	2
	PF_PFExtStr	Excitation of the start point for PF(*P*) control	0: overexcited 1: underexcited	0
	PF_PFStr	Power factor of the start point for PF(*P*) control	PFLim ... 1	0.9
	PF_WNomStr	Active power of the start point for PF(*P*) control in p.u.	0 ... 1	0.5
	PF_PFExtStop	Excitation of the stop point for PF(*P*) control	0: overexcited 1: underexcited	1
	PF_PFStop	Power factor of the stop point for PF(*P*) control	PFLim ... 1	0.9
	PF_WNomStop*	Active power of the stop point for PF(*P*) control in p.u.	0 ... 1	0.9

* Be sure to adjust PF_WNomStop to be greater than PF_WNomStr, otherwise it will be automatically set to PF_WNomStop = PF_WNomStr + 0.001.

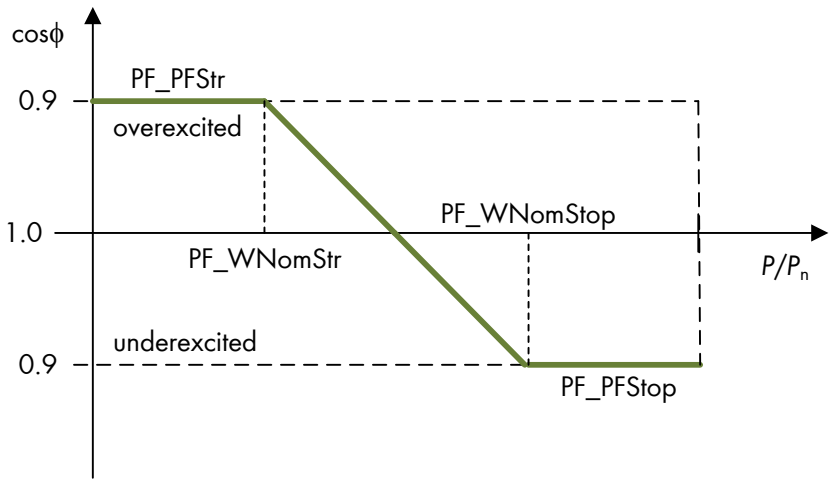


Figure 7: Example for cosφ(*P*) statics.

4.2.4.1 Initialization

The user must take care that the reactive power is initialized correctly, i.e. the steady-state solution must match the correct reactive power resulting from the characteristics in Figure 7 defined by the dyr file parameters.

Otherwise initial conditions will be designated as being "suspect" by PSS®E.

4.2.5 Voltage-dependent reactive power control (VArCtlVol)

Please the Sunny Central 2200/2500-EV Operating Manual for a description of this mode. Please note the gradient parameters must be positive numbers and form a curve with monotonous characteristics.

The following figure provides a screenshot from the Operating Manual.

13 Function Description SMA Solar Technology AG

13.4.4 Reactive Power Control as a Function of Grid Voltage: VArCtlVol Mode

The reactive power is controlled as a function of the grid voltage. By supplying reactive power, the inverter performs voltage-stabilizing measures in the event of overvoltage or undervoltage. The parameterization is carried out by means of a reactive power/voltage characteristic curve. The characteristic curve can be flexibly configured by parameterizing the slope and a type of deadband through two voltage points.

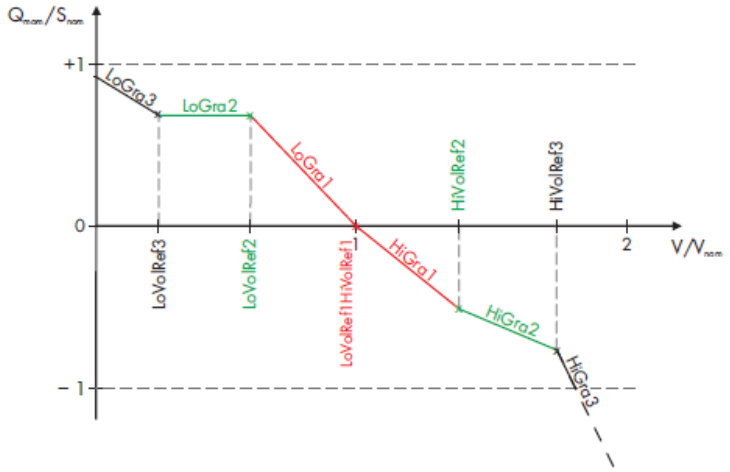


Figure 96: Characteristic curve of the voltage-dependent reactive power control

A quotient is derived from the ratio of grid voltage to nominal voltage.

When the grid voltage is equal to the defined nominal voltage, the reactive power feed-in is zero. If the grid voltage changes and exceeds or falls short of a defined threshold, the inverter reacts according to the voltage/reactive power characteristic curve by adjusting its reactive power feed-in. For each voltage quotient three thresholds can be configured, and the gradients of the reactive power adjustment for decreasing or increasing grid voltage can be defined individually for each threshold.

Overview of the relevant parameters

Parameter	Description
VArCtlVol.LoVolRef1HiVolRef1	Voltage quotient at which reactive power feed-in is zero
VArCtlVol.HiVolRef2/HiVolRef3	Threshold of the voltage quotient at increased grid voltage
VArCtlVol.HiGra1/HiGra2/HiGra3	Gradient of reactive power adjustment of the given voltage band at increased grid voltage
VArCtlVol.LoVolRef2/LoVolRef3	Threshold of the voltage quotient at reduced grid voltage
VArCtlVol.LoGra1/LoGra2/LoGra3	Gradient of reactive power adjustment of the given voltage band at increased grid voltage
VArCtlVol.VArSptFilTm	Filter constant by which the measured values of the grid voltage are filtered This enables more stable control.
VolNomSptMan	Voltage setpoint at 0 Q_{Mom}/S_{Nenn}

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See also parameters VArCtlVolVolNomSptMod, VArCtlVolVolFilTm, VArCtlVolVolMin, VArCtlVolVolMax for additional functionality.

Dynamic grid support

4.2.6 Dynamic grid support “full” (fault ride-through)

This mode is available for the Sunny Central HE-20 and Sunny Central (CP) line only. Older Sunny Central inverters do not feature this mode. Note that the “DGS limited” behavior correlates to firmware release 13 of the CP line while the “DGS full” behavior correlates to firmware releases below 13.

In the dynamic grid support “full” mode the inverter is able to inject active or reactive current according to the parameter FRTArGraNom. If FRTArGraNom is set to zero the inverter feeds in active power. If FRTArGraNom is greater than zero the inverter feeds in reactive power.

See also the description of parameter CON(J+133) Frt_AmpQFilTm.

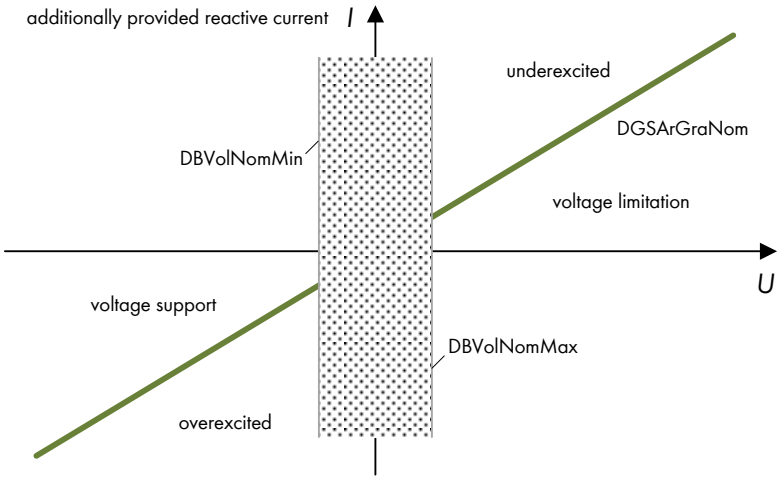


Figure 8: Illustration of dynamic grid support characteristics.

Note: The voltage at the points designated by FRTDbVolMin and FRTDbVolMax is exactly [1–FRTDbVolMin] and [1+FRTDbVolMax] when FRT_VolFilMod = 0. When FRT_VolFilMod = 1, these points are [Ufilt–FRTDbVolMin] and [Ufilt+FRTDbVolMax] where Ufilt is the low-pass filtered voltage, i.e. the normalized one-minute average of the voltage.

The following alternative characteristic curve can be activated by setting FRTMod = 2 (note the continuous characteristics at the ends of the dead zone).

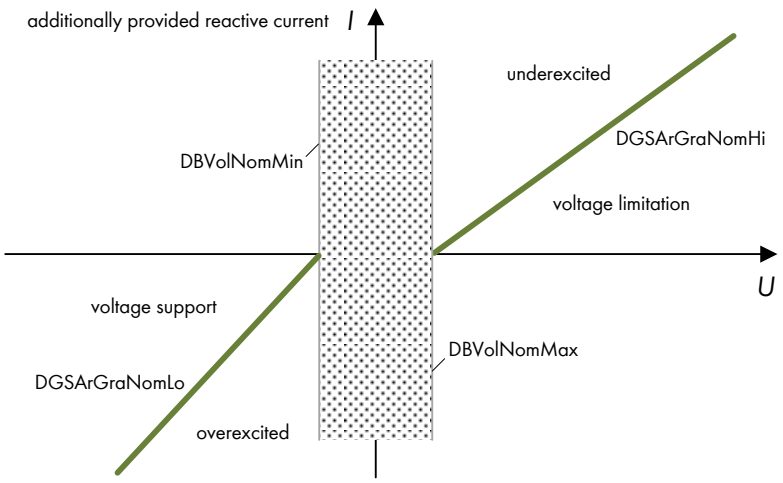


Figure 9: Illustration of dynamic grid support characteristics ("SDLWindV" curve).

The parameter FRT_AmpDGra defines the recovery speed of the active power after the fault state has been removed. The reactive power behavior is not affected by this parameter.

Note that the inverter behavior can be more intricate than replicated by this model when the voltage is very close to the DGS boundaries for a longer period of time. Please contact SMA if you want to study inverter reaction in that case with more details.

The parameters DGSArGraNomLo/Hi are obsolete beginning with model version 1.71; the characteristics can now be set with the parameters described in the documentation of the PSCAD model (J+160 – J+171).

4.2.7 Dynamic grid support "partial" (no reactive power feed-in)

The inverter is not tripped in case of voltage dips below nominal voltage plus FRTDbVolMin or above nominal voltage plus FRTDbVolMax but disables feed-in of active and/or reactive power. After recurrence of the voltage the inverter resumes feed-in according to the parameterization before the voltage dip.

The parameter FRTWRcvrTmP defines the recovery time of the active power after the fault state has been removed. The reactive power behavior is not affected by this parameter.

4.2.8 Spike mitigation

This function was introduced to avoid spikes when the voltage recovers very fast at FRT exit. It is activated when the voltage falls below FRTSpkMtgLo. The function then waits for the voltage to recover above FRTSpkMtgHi. When this happens, the injection of current is suppressed for two simulation steps. This function can be deactivated by setting FRTSpkMtgLo = FRTSpkMtgHi = 0.

4.2.9 Dynamic grid support voltage detection

The signal which is used for detection of a dynamic grid support situation can be obtained in two different ways:

1) The signal is calculated by the measured voltage divided by the nominal voltage. From this result is subtracted the value 1 p.u.

2) The signal is calculated by the measured voltage divided by a low-pass filtered voltage. From this result is subtracted the value 1 p.u. The low-pass filtered voltage is obtained through a first-order lag (PT1) block with time constant FRT_VolDFilTm. The state of the filter is frozen during the FRT situation.

The parameter FRT_VolFilMod decides which method is used.

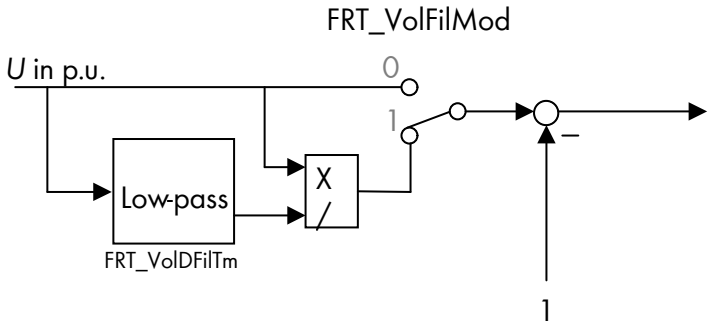


Figure 10: Dynamic grid support voltage detection signal processing chain.

4.2.9.1 Detection band hysteresis

Dynamic grid support for high voltage situations is activated, i.e. (H)FRT mode is entered, when the voltage exceeds 1+ FRTDbVolMax. HFRT mode is left, when thereupon the voltage falls below 1+ FRTDbVolMaxHyst.

Dynamic grid support for low voltage situations is activated, i.e. (L)FRT mode is entered, when the voltage falls below 1- FRTDbVolMin. LFRT mode is left, when thereupon the voltage exceeds 1- FRTDbVolMminHyst.

4.3 Decoupling protection

In under-/overvoltage and under-/overfrequency situations specified by the protection scheme parameters, the PWM pulse signals of the inverter bridge are deactivated. Therefore, active and reactive current injection commands are set to zero in this case. Additionally, the generator can be tripped using the GENTRP command by setting the parameter GenTrpFlag to 1.

4.3.1 Voltage decoupling protection

There are five overvoltage and five undervoltage trip points each with a distinct time delay. Additionally, in the physical inverter there can be defined another trip threshold which evaluates the instantaneous value of the terminal voltage. This trip point is therefore not incorporated in the RMS model SMASC.

4.3.1.1 Alternative undervoltage decoupling protection

n/a

4.3.2 Frequency decoupling protection

There are six overfrequency and six underfrequency trip points each with a distinct time delay.

4.4 Selection of the PLL model for reference angle calculation

The model provides four different implementations (PLLFlag = 0...3) to determine the reference angle. For PLLFlag = 2 and PLLFlag = 3, the reference angle is directly obtained from the bus voltage.

The PLL behavior of the physical inverter can be taken into account by two different PLL model implementations, selected by parameter PLLFLAG. PLL model 1 (PLLFlag = 0) is just the representation of a first-order delay low-pass filter with the single parameter KPLL1.

	KPLL1	First-order low-pass filter time delay	1 ... 30	30
	PLLFlag	Determines whether inverter PLL is modeled by a simple first-order delay (0) with parameter KPLL1, or by a PLL control loop (1) with parameters KPPLL2 and KIPLL2. For experimental studies the PLL can also be disabled: PLLFlag = 2: angle is directly obtained from PSS®E BUSDAT routine PLLFlag = 3: angle is directly obtained from measurement of the complex bus voltage `VOLT(IB)`		1
	KPPLL2	PLL 2 control loop control gain		10
	KIPLL2	PLL 2 control loop integration gain		30

PLL model 2 (PLLFlag = 1) represents a closed-loop control structure according to Figure 11 and can be used if PLL model 1 (PLLFlag = 0) does not give satisfactory results.

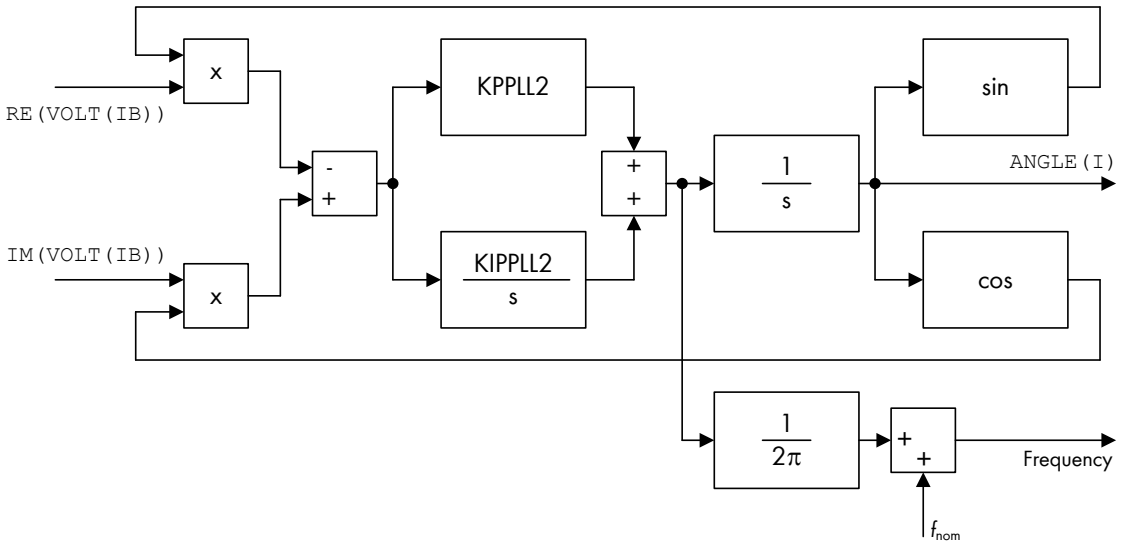


Figure 11: Block diagram of PLL model 2 (PLLFlag = 1).

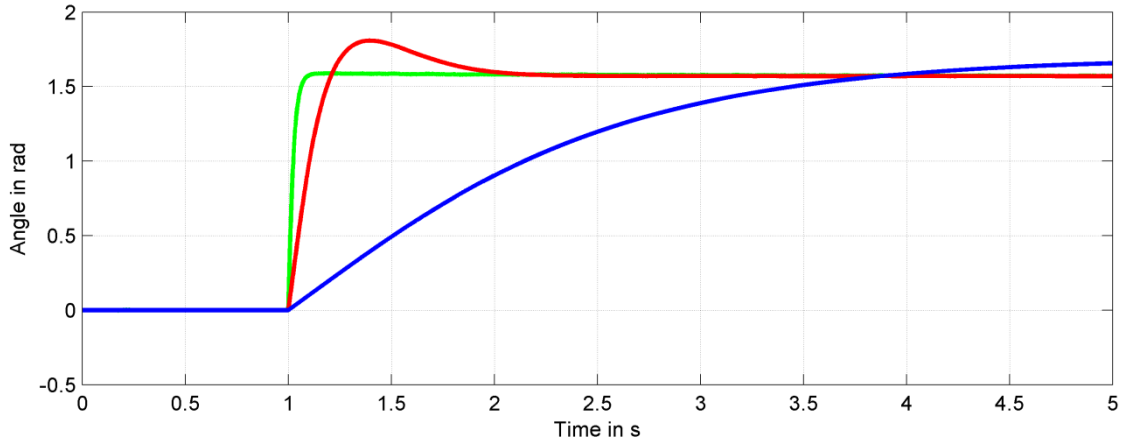


Figure 12: PLL model 2 (PLLFlag = 1) response to a step function at t = 1 s stimulus with three different parameterizations: KPPLL2 = 1, KIPLL2 = 0.1 (blue); KPPLL2 = 10, KIPLL2 = 30 (red); KPPLL2 = 50, KIPLL2 = 30 (green).

4.5 Selection of the PLL model for frequency calculation

The model provides two different implementations (PLLFlag2 = 0...1) to determine the frequency. For PLLFlag2 = 0 the frequency is directly obtained from the bus frequency. Dynamics are represented by a first-order delay low-pass filter with the single parameter HzFltTm.

The PLL behavior of the physical inverter can be taken into account by activation of a PLL model implementation according to Figure 11. Please note that angle and frequency calculation are two separate implementations, though the same PLL structure is used.

Frequency measurement can be realized in the following ways:

- PLLFmeas2 is the frequency measurement obtained from PLL2 (with PLLFlag2 activated)
- STATE(K+16) is VAR(L+16) – first-order low-pass filtered with time constant HzFltTm.

The following combinations are possible:

1) HzFltTm=0 and PLLFlag2=0 Frequency = PLLFmeas
2) HzFltTm=0 and PLLFlag2=1 Frequency = PLLFmeas2
3) HzFltTm>0 and PLLFlag2=0 Frequency = STATE(K+16)
4) HzFltTm>0 and PLLFlag2=1 Frequency = PLLFmeas2

For example when PLLFlag2 = 0 and HzFltTm is set to 0.01 the system frequency measurement is obtained from VAR(L+16) first-order low-pass filter with time constant of 10 ms.

4.6 Iq set-point scaling

For achieving a correct response of the inverter model SMASC when used in conjunction with the plant control model SMAPPC, please note the following:

In the plant control model, the reference for active and reactive power set-points and signals can be modified by parameters PRefTot and QRefTot. This accounts for deploying multiple generators (by using the sum of the

active and reactive power values of all controlled generators to calculate PRefTot and QRefTot). The physical SMA Power Plant Controller internally uses such parameters, too, where the active power reference is usually the sum of the maximum active power values of all connected inverters, while the reactive power reference is usually the sum of the maximum reactive power values of all connected inverters – e.g., PRefTot might be 50 (MW) (25 x SC 2500 inverters), and QRefTot might be 30 (Mvar) (60% of the active power rating). The Power Plant Controller then uses this value of 30 Mvar for normalization of all reactive power signals, and consequently, it requests a reactive power provision of 30 Mvar from all connected devices when a control value of 100% (1 p.u.) is sent (signal `EFD(I)` in the SMAPPC model).

The physical SMA SC inverter refers this reactive power command of 100% to the maximum reactive power of the device, i.e. it then provides full reactive power, which might be 60% of the inverter MVA rating, e.g. 1500 kvar for a SC 2500 inverter.

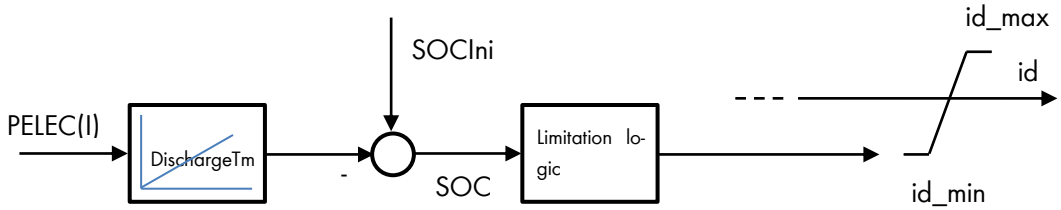
In contrast, the model SMASC refers all power signals to `MBASE(I)`, and would therefore provide 50 Mvar for an aggregated 50 MVA generator (`MBASE(I)` = 50 MVA), if the set-point QVArNom is set to 1.0 or the external Iq set-point signal `EFD(I)` is set to 1.0. To correct this, the model contains parameter QVArScale, with which the Iq set-point signal is multiplied before it is transferred to the generator front-end (current injection) model.

For example, QVArScale = 0.6 would result in a reactive power provision of 30 Mvar if the set-point QVArNom is set to 1.0 or the external Iq set-point signal `EFD(I)` is set to 1.0 for a 50 MVA generator.

4.7 Storage inverter functionality

Consider a storage inverter plant rated 50 MVA, with a storage size or energy rating of 250 MWh. The plant is supposed to always be in a state of charge between 0% and 100%.

From these data we calculate a discharge time (parameter DischargeTm) of 5 hours = 18000 s. Please note that parameter SMASCSFlag must be set to 1 to enable this function.



Limitation logic:

```
id_min = -1.0
idmax  = 1.0
IF (SOC >= 0.98)
     id_min = 0.0
ELSEIF (SOC <= 0.02)
     id_max = 0.0
ENDIF
```

Figure 13: Storage inverter functionality block diagram. `PELEC(I)` is the electric output active power of the generator normalized to `MBASE(I)`.

The following figure shows the block diagram of the battery charge controller. Please see also the documentation of the plant control model.

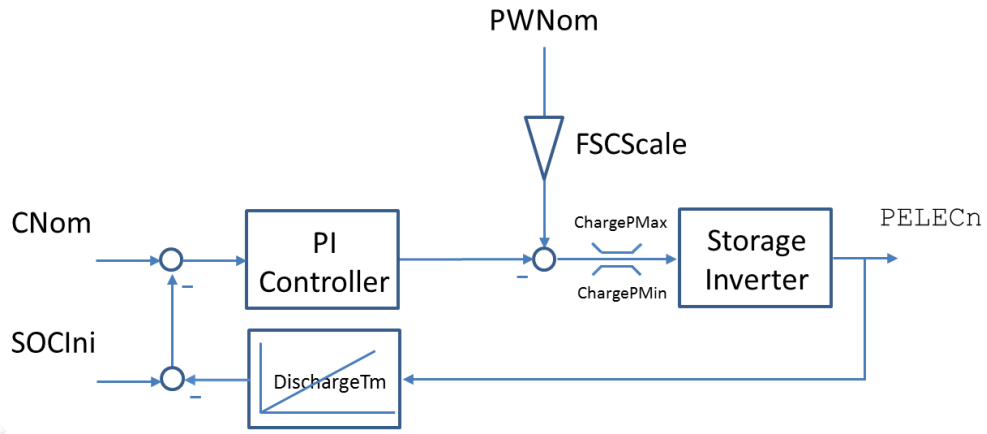


Figure 14: Block diagram of the battery charge controller. `PELECn` is the electric output active power of the generator normalized to `MBASE(I)`.

The PI controller is parameterized with KP_C and KI_C, and the output of the integration block (designated with DischargeTm) is the state of charge (SOC) of the battery.

For simulation of a combined PV/storage inverter setup together with the plant control functions parameter SMASCSFlag must be set to 2.

Please note: when SMASCSFlag is set to 2, the associated generator must initialize with zero active power.

5 Appendix

5.1 Model output for activity DOCU (exemplary for C1.38)

```
** SMASC176 **   BUS X-- NAME --X BASEKV MC       C O N S   S T A T E S       V A R S

                1 PVPLANT      0.3850 1       1-   200      1-    60      1-   300

            MBASE           Z S O R C E             X T R A N   GENTAP

             50.0      0.00+J      1.00      0.00+J      0.00  1.00000

  ICONS and CONS:

  SLACK_BUS

              9999

  PPrim             PWNom             QVArNom           PFLim             PFPF              PFPFExt

            1.000             1.000             0.000             0.800             0.800             0.000

  QVArMod           QoDEna            QoDQMax           VArCtlVol_Volref  VArCtlVol_VolDB   VArCtlVol_VArGra

            1.000             0.000             0.600             1.000             0.000             5.000

  VArCtlVol_VArMax  VArCtlVol_VArTm   PFPFExtStr        PFPFStr           PFWStr            PFPFExtStop

            0.500             2.000             0.000             0.900             0.500             1.000

  PFPFStop          PFWStop           WCtlHzMod         PHzStr            PHzStop           PWGra

            0.900             0.900             0.000             0.200             0.050             0.500

  WGra              VArGra            FRTMod            FRTArGraNom       FRTArGraNomHi     FRTArGraNomLo

            1.000             2.000             2.000             2.000             2.000             2.000

  FRTDbVolMax    FRTDbVolMaxHyst      FRTDbVolMin       FRTDbVolMinHyst   FRT_AmpDGra       Reserved

            0.250             0.250             0.200             0.200            10.000             1.000

  VArCmdFilTm       FRT_VolFilMod     FRT_VolDFilTm     FRT_WaitTm        FRT_AmpQGra       FRTSpkMtgLo

            0.000             1.000             1.000             0.020            10.000             0.000

  FRTSpkMtgHi       Reserved          Reserved          Reserved          VCtl_Hi5Lim       VCtl_Hi5LimTm

            0.000             0.000             0.125             0.100             1.300             0.100

  VCtl_Hi4Lim       VCtl_Hi4LimTm     VCtl_Hi3Lim       VCtl_Hi3LimTm     VCtl_Hi2Lim       VCtl_Hi2LimTm

            1.300             0.100             1.300             0.100             1.250             1.000

  VCtl_Hi1Lim       VCtl_Hi1LimTm     VCtl_Lo1Lim       VCtl_Lo1LimTm     VCtl_Lo2Lim       VCtl_Lo2LimTm

            1.200            60.000             0.800            21.000             0.800            21.000

  VCtl_Lo3Lim       VCtl_Lo3LimTm     VCtl_Lo4Lim       VCtl_Lo4LimTm     VCtl_Lo5Lim       VCtl_Lo5LimTm

            0.800            21.000             0.800            21.000             0.800            21.000
```

HzCtl_Hi6Lim	HzCtl_Hi6LimTm	HzCtl_Hi5Lim	HzCtl_Hi5LimTm	HzCtl_Hi4Lim	HzCtl_Hi4LimTm
55.000	0.100	55.000	0.100	55.000	0.100
HzCtl_Hi3Lim	HzCtl_Hi3LimTm	HzCtl_Hi2Lim	HzCtl_Hi2LimTm	HzCtl_Hi1Lim	HzCtl_Hi1LimTm
55.000	0.100	55.000	0.100	53.000	60.000
HzCtl_Lo1Lim	HzCtl_Lo1LimTm	HzCtl_Lo2Lim	HzCtl_Lo2LimTm	HzCtl_Lo3Lim	HzCtl_Lo3LimTm
45.000	0.100	45.000	0.100	45.000	0.100
HzCtl_Lo4Lim	HzCtl_Lo4LimTm	HzCtl_Lo5Lim	HzCtl_Lo5LimTm	HzCtl_Lo6Lim	HzCtl_Lo6LimTm
45.000	0.100	45.000	0.100	47.000	60.000
KPLL1	PLLFlag	KPPLL2	KIPLL2	HzFltTm	PLLFlag2
30.000	10.000	50.000	30.000	0.000	0.000
KPPLL3	KIPLL3	WriteFileNum	WriteTimeSpan	GenTrpFlag	PPrioEna
5.000	0.300	0.000	12.500	1.000	0.000
SMASCSFlag	DischargeTm	SOCIni	KP_C	KI_C	CDB
0.000	3600.000	0.900	0.010	0.050	0.000
CNom	FSCScale	ChargePMax	ChargePMin	PC_BUS_NO	QVArScale
0.900	1.000	1.000	1.000	3.000	0.600
VREps	FRT_AmpDLim	FRT_AmpQLim	Reserved	Reserved	GriMngInvVArMod
0.010	2.000	2.000	0.000	0.000	0.000
VolLoVolRef3	VolLoVolRef2	VolRef1HiVolRef1	VolHiVolRef2	VolHiVolRef3	VArCtlVolLoGra3
0.850	0.920	1.000	1.080	1.150	2.000
VArCtlVolLoGra2	VArCtlVolLoGra1	VArCtlVolHiGra1	VArCtlVolHiGra2	VArCtlVolHiGra3	VVolVArSptFilTm
0.100	2.000	2.500	1.000	2.000	0.010
VolNomSpt	Frt_AmpQFilTm	IniSchemeFlag	VArCtlVolNomSptMod	VArCtlVolVolFilTm	VArCtlVolVolMin
1.000	1.000	1.000	1.000	0.500	0.900
VArCtlVolVolMax	PwrCtl_VolDQFilTm	Reserved	Reserved	Reserved	Pll_Inv_TLength
1.100	0.000	0.000	0.000	0.000	0.010
Pll_Inv_TSample	Pll_Inv_TimeStep	HzFilOff2On_Vol	HzFilOff2OnNomSum	HzFilOn2OffNomSum	HzFilOn2Wt_Vol
0.000	0.001	0.600	0.500	80.000	0.750
HzFilWt2On_Vol	Pll_Inv_SetTm	Pll_Inv_DmpRto	Pll_InvVolDQFilTm	Pll_Inv_VolDQRtg	Pll_Inv_Fn
0.650	0.045	2.000	0.005	385.000	50.000
Pll_Inv_HzGraLim	Pll_Inv_HzFilTm	Reserved	Reserved	Frt_LoGra1	Frt_LoGra2
300.000	0.100	0.000	0.000	0.000	2.000

Frt_LoGra3	Frt_LoVolRef1	Frt_LoVolRef2	Frt_LoVolRef3	Frt_HiGra1	Frt_HiGra2
2.000	1.000	0.800	0.000	0.000	2.000
Frt_HiGra3	Frt_HiVolRef1	Frt_HiVolRef2	Frt_HiVolRef3	Reserved	Reserved
2.000	1.000	1.250	2.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved				
0.000	0.000				

STATES:

PLL_int	Reserved	x_HP_lim	x_LP_lim	x_PT1_lim	PT1_DGS
0.000	0.000	0.000	0.000	0.000	0.000
Curr_Derat	W_Derat	Var_Derat	VDN_PT1	StatGen_PT1	Test_PT1
0.000	0.000	0.000	0.000	0.000	0.000
PLL_Filt_int	PLL_VCO_int	Iq_PT1_Filt	QPreFault	Frq_Filt	PLL2_Filt_int
0.000	0.000	0.000	0.000	0.000	0.000
PLL2_VCO_int	AmpPsQ_SptOut_int	Batt_SOC	Volt_Filt_ctrl	CC_Int	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	AmpPsD_SptR_int	Volt_Filt_nw	LP_Filt_W2Amp	LPF_VarCtlVol	LPF_VarCtlVolFilTm
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	PLL_phitrack	RevPLL_ModInt
0.000	0.000	0.000	0.000	0.000	0.000
RevPLL_PT1_VolPsQ	RevPLL_PT1_VolPsD	RevPLL_HzFil	RevPLL_dsindt	RevPLL_dcosdt	RevPLL_InvKi
0.000	0.000	0.000	0.000	0.000	0.000
RevPLL_Tm_SM2224	RevPLL_Tm_SM2324	RevPLL_Tm_SM2421	RevPLL_xspace	Reserved	Reserved

```
          0.000            0.000            0.000            0.000            0.000            0.000
Reserved         Reserved         Reserved         Reserved         Reserved         Reserved
          0.000            0.000            0.000            0.000            0.000            0.000
VARS:
Gen_Status       Base_Freq        P_init_pu        V_init_pu        PLL_memory       phi_count
          0.000            0.000            0.000            0.000            0.000            0.000
Reserved         ICidout_unfilt   ICIs             LP_Pos_phsq      LPIS_MAX         LPyi1_Lim
          0.000            0.000            0.000            0.000            0.000            1.867
DGSVol_dPos      Reserved         DZDVtg_abnormal  LPyi1_Lim_Delay  Freq_meas        FRTInvert
          0.000            0.000            0.000            0.000            0.000            0.000
Tm_picdro1       Tm_picdro2       Reserved         Tm_picdro3       Tm_picdro4       Reserved
          0.000            0.000            0.000            0.000            0.000            0.000
Tm_picdro5       Tm_picdro6       Reserved         Tm_picdro7       Tm_picdro8       Reserved
          0.000            0.000            0.000            0.000            0.000            0.000
Tm_picdro9       Tm_picdro10      Reserved         DERTanPhi        Derat_W          Derat_Var
          0.000            0.000            0.000            0.000            0.000            0.000
VDNNormal_Mode   VDN_FLFL         PwrAtLimit_Old   VDN_QSpnt        ICid_out         SGCyi
          0.000            0.000            0.000            0.000            0.000            1.000
Tm_picdro11      FRT_Q_store      Tm_picdro12      Tm_picdro13      Tm_picdro14      Rly_picdro1
          0.000            1.000            1.000            1.000            0.000            1.014
Rly_picdro2      Reserved         Rly_picdro3      Rly_picdro4      Reserved         Rly_picdro5
          0.050           -0.001            0.050           -0.007           -1.000            1.014
Rly_picdro6      Reserved         Rly_picdro7      Rly_picdro8      Reserved         Rly_picdro9
          1.014            0.050            1.000            1.014            0.000            1.000
Rly_picdro10     Reserved         PT1_Gen_input    Wrt_file_flag    Inv_Trp_Flag     Reserved
          0.050           -0.001            0.000            0.000            0.000           -0.002
Reserved         Reserved         Reserved         Reserved         Reserved         Reserved
         -0.002            1.000           -1.000            0.050            0.000            0.050
PWMEna           VArCtlVol_Volref  VArCtlVol_Volref_BckShutdown          Tm_picdro15      Tm_picdro16
         -0.001            0.123            1.000            0.000            0.000            0.000
Tm_picdro17      Tm_picdro18      Relay_picdro11   Relay_picdro12   Relay_picdro13   Relay_picdro14
         -0.001           50.000           50.000            0.050            1.000            0.050
```

PLLdphi	PLLom	PLLsinphi	PLLcosphi	PPRIM_init	QVARNOM_init
1.000	1.000	0.050	0.000	0.000	0.000
QSpt_init	PF_init	PFSpt_init	PFEXT_init	PF_ss_init	Init_Flag
0.000	0.000	0.000	0.000	0.050	0.000
PWNOM_init	FLFL_state	FLFL_hold	Tm_picdro19	Relay_picdro15	PT1_Iq_Filt
0.000	1.000	0.000	0.000	-0.100	0.150
FRT_Flag	Sim_count	Iq_sup_mem	count_Iq_sup	Relay_picdro16	Tm_picdro20
0.050	0.000	0.050	0.000	0.000	0.000
Tm_picdro21	Relay_picdro17	Tm_picdro22	Tm_picdro23	Relay_picdro18	Tm_picdro24
0.000	0.000	0.000	0.000	0.000	0.000
Tm_picdro25	LVRTi_sig	HVRT_sig	LVRT_sig	LVRT_relay_St	LVRT_relay_Tm
0.000	0.000	0.000	1.000	0.000	0.000
LVRT_FLFL	HVRT_FLFL	LPu0	Reserved	Reserved	Reserved
50.000	3.000	-0.001	0.000	0.000	0.000
Reserved	PLLdphi_2	PLLom_2	PLLsinphi_2	PLLcosphi_2	Frt_QRamp_St
50.000	50.000	50.000	50.000	50.000	0.500
PsQR_AmpPsQ_SptOut	PsQR_AmpPsQ_SptOut_int	PLLFmeas	ROCOF	PLLFmeas2	ROCOF2
0.000	-0.001	0.050	-0.001	1.014	-1.000
Volt_meas_mode3	P_Frt_store	PSpt_CC	SOC	Id_Spt	Tm_picdro26
0.000	1.014	2.499	-0.017	0.000	0.000
Relay_picdro19	Tm_picdro27	Relay_picdro20	Tm_picdro28	Relay_picdro21	Tm_picdro29
0.000	0.000	0.000	0.000	0.000	0.000
Relay_picdro22	Tm_picdro30	Relay_picdro23	Tm_picdro31	Relay_picdro24	Tm_picdro32
0.000	0.000	0.000	0.000	0.000	0.000
Relay_picdro25	Tm_picdro33	Relay_picdro26	Tm_picdro34	Relay_picdro27	Tm_picdro35
0.000	0.000	0.000	0.000	0.000	0.000
Relay_picdro28	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	PsQR_Frt_Stt	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
pctl_val	qctl_val	Reserved	Amp_PsD_Spt_FrtMin	Amp_PsD_Spt_Ramp_Int1	AmpSpt_Dif
0.000	0.000	0.000	0.000	0.000	0.000

RampEndDetection	FrtRampActive	Reserved	Reserved	Reserved	Flow_dir
0.000	0.000	0.000	0.000	0.000	0.000
LVRT_Flag	HVRT_Flag	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Curr_Angle	Reserved	MA_Filt1	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	MA_Filt2	PllSubStt
0.000	0.000	0.000	0.000	0.000	0.000
RevPLL_block	RevPLL_count	RevPLL_Phi	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0.000	0.000	0.000	0.000	0.000	0.000
Reserved	Reserved				
0.000	0.000				

6 Disclaimer

This document and the associated models have been prepared to facilitate the behavioral simulation of the response of SMA Sunny Central solar inverters to grid and parameter disturbances. The modeling data presented herein are intended to produce simulation results that closely approximate the response of the inverters to these disturbances, and do not necessarily represent the physical implementation of the inverter or plant control algorithms.