CS-220:Assignment-7(Project report)
Processor development

PDS-1:

Deciding the registers and usage protocol:

An array of 32 registers with size 32 bits and address bits of length 5 bits (reg-0 to reg-31).

Register's name	Register number(according to the address)	Functionality:
$zero	Reg-0	Register with the value '0'.
$ai	Reg-1	Register holding immediate values.
$r0, $r1	Reg-2,3	Register holding return values of a function.
$a0-$a3	Reg-4 to 7	Register holding arguments to be passed to a function.
$t0-$t9	Reg-8 to 17	Registers for temporary storage.
$p0-$p7	Reg-18 to 25	Registers used to hold values that need to be preserved across function calls(storage of variables permanently).
$k0, $k1	Reg- 26, 27	Kernel-mode interrupts
$gp	Reg-28	Global pointer
$sp	Reg-29	Stack pointer
$fp	Reg-30	Frame pointer
$ra	Reg-31	Return address

PDS-2:

Deciding upon the size for instruction and data memory in VEDA:
Number of words allocated for instructions= 26(25+1 buffer)
Number of words allocated for data memory=6.

PDS-3:

Designing the instruction layout for R-, I- and J-type instructions and their respective encoding methodologies:

1)R-type:

opcode	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

2)I-type:

opcode	rs	rt	Immediate/ address
6 bits	5 bits	5 bits	16 bits

3)J-type:

opcode	address
6 bits	26 bits

List of funct codes:

Instruction	opcode	funt code
add	0	32
sub	0	34
addu	0	60
subu	0	56
addi	0	33

addiu	0	57
and	0	36
or	0	37
andi	0	20
ori	0	21
sll	0	0
srl	0	2
lw	51	-
sw	53	-
beq	4	-
bne	5	-
bgt	7	-
bgte	15	-
ble	6	-
bleq	31	-
j	2	-
jr	7	-
jal	8	-
slt	9	-
slti	5	-

Team members-
Mokshagna Prattipati (210761)
Kruthi Akkinepally (210088)