Bangladesh Army University of Engineering & Technology (BAUET)
Department of Computer Science and Engineering

Microprocessor and Micro-controller

Pin Function of 8086/8088 Microprocessor

Professor Dr. Md. Rabiul Islam
Dept. of Computer Science & Engineering
Rajshahi University of Engineering & Technology
Rajshahi-6204, Bangladesh.
rabiul_cse@yahoo.com

Outline

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References

Chapter 8 Barry B. Brey, “The Intel Microprocessors 8086/8088, 80186/80188, 80286, 80386, 80486, Pentium, and Pentium Pro Processor, Architecture, Programming, And Interfacing”, 4th Edition, Prentice Hall, 1997.

Pin Function of 8086/8088 microprocessor

Pin Out Diagram:

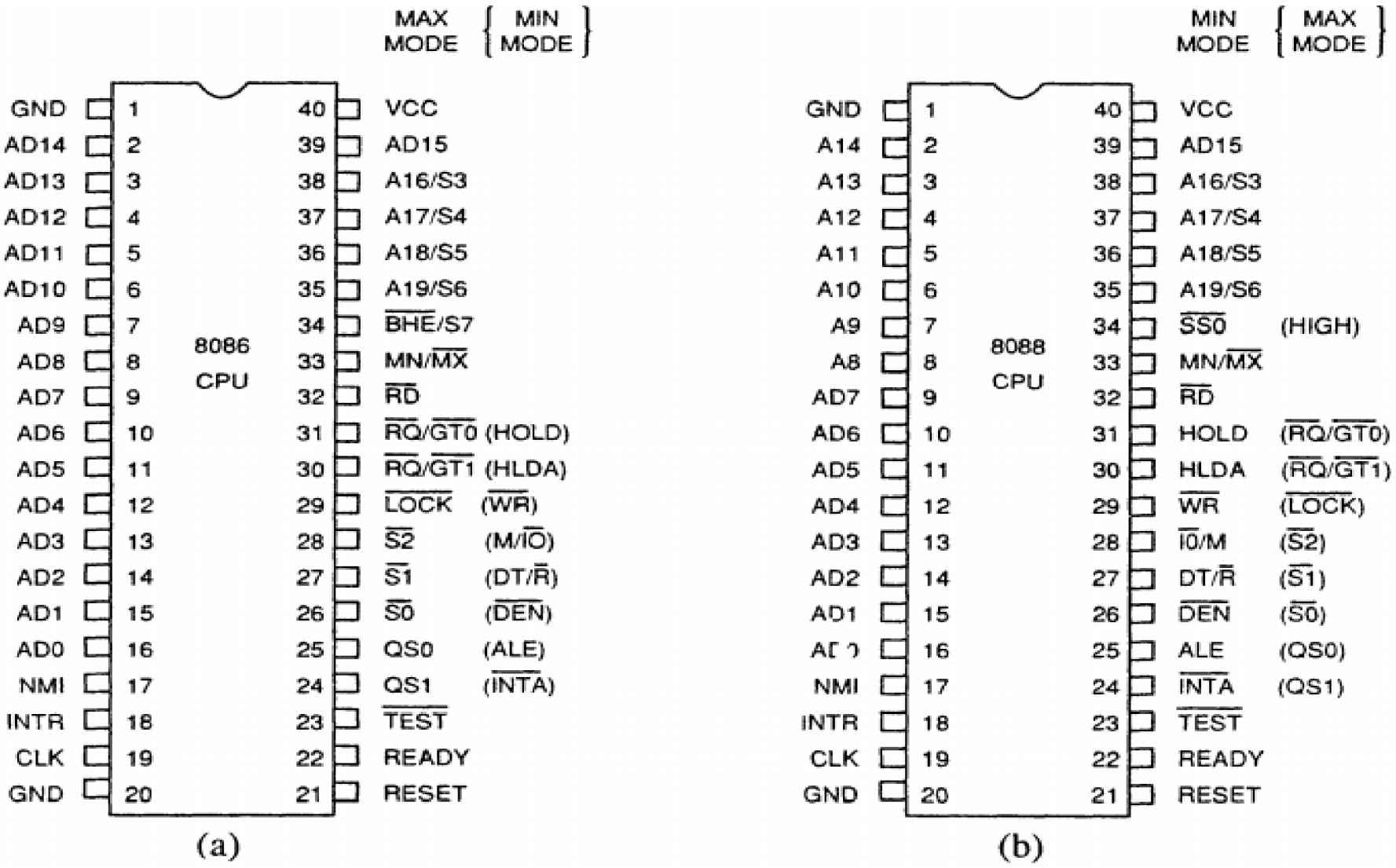

Figure: Pin-out diagram of (i) 8086 microprocessor (ii) 8088 microprocessor

Pin Function of 8086/8088 microprocessor

Pin Functions of General Pins:

AD_7–AD_0 The 8088 **address/data bus** lines compose the multiplexed address data bus of the 8088 and contain the rightmost 8-bits of the memory address or I/O port number whenever ALE is active (logic 1) or data whenever ALE is active (logic 0). These pins are at their high-impedance state during a hold acknowledge.

A_{15}–A_8 The 8088 **address bus** provides the upper-half memory address bits that are present throughout a bus cycle. These address connections go to thei high-impedance state during a hold acknowledge.

AD_{15}–AD_8 The 8086 **address/data bus** lines compose the upper multiplexed address/data bus on the 8086. These lines contain address bits A_{15}–A_8 whenever ALE is a logic 1, and data bus connections D_{15}–D_8. These pins enter a high-impedance state whenever a hold acknowledge occurs.

A_{19}/S_6–A_{16}/S_3 The **address/status bus** bits are multiplexed to provide address signals A_{19}–A_{16} and also status bits S_6–S_3. These pins also attain a high-impedance state during the hold acknowledge.

Status bit S_6 always remains a logic 0, bit S_5 indicates the condition of the IF flag bits, and S_4 and S_3 show which segment is accessed during the current bus cycle. Refer to Table for the truth table of S_4 and S_3. These two status bits could be used to address four separate 1M byte memory banks by decoding them as A_{21} and A_{20}.

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Pin Functions of General Pins:

TABLE Function of status bits S_3 and S_4

S_4	S_3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

$\overline{RD}$ Whenever the **read signal** is a logic 0, the data bus is receptive to data from the memory or I/O devices connected to the system. This pin floats to its high-impedance state during a hold acknowledge.

READY This input is controlled to insert wait states into the timing of the microprocessor. If the READY pin is placed at a logic 0 level, the microprocessor enters into wait states and remains idle. If the READY pin is placed at a logic 1 level, it has no effect on the operation of the microprocessor.

INTR **Interrupt request** is used to request a hardware interrupt. If INTR is held high when IF = 1, the 8086/8088 enters an interrupt acknowledge cycle (INTA becomes active) after the current instruction has completed execution.

$\overline{TEST}$ The **Test** pin is an input that is tested by the WAIT instruction. If $\overline{TEST}$ is a logic 0, the WAIT instruction functions as a NOP. If $\overline{TEST}$is a logic 1, then the WAIT instruction waits for $\overline{TEST}$ to become a logic 0. This pin is most often connected to the 8087 numeric coprocessor.

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Pin Functions of General Pins:

NMI	The **non-maskable interrupt** input is similar to INTR except that the NMI interrupt does not check to see if the IF flag bit is a logic 1. If NMI is activated, this interrupt input uses interrupt vector 2.
RESET	The reset input causes the microprocessor to reset itself if this pin is held high for a minimum of four clocking periods. Whenever the 8086 or 8088 is reset, it begins executing instructions at memory location FFFF0H and disables future interrupts by clearing the IF flag bit.
CLK	The **clock pin** provides the basic timing signal to the microprocessor. The clock signal must have a duty cycle of 33% (high for one-third of the clocking period and low for two-thirds) to provide proper internal timing for the 8086/8088.
V_{CC}	This **power supply** input provides a +5.0 V, ±10 % signal to the microprocessor.
GND	The **ground** connection is the return for the power supply. Note that the 8086/8088 microprocessors have two pins labeled GND—both must be connected to ground for proper operation.

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Pin Functions of General Pins:

MN/$\overline{\text{MX}}$	The **minimum/maximum mode** pin selects either minimum mode or maximum mode operation for the microprocessor. If minimum mode is selected, the MN/MX pin must be connected directly to +5.0 V.
$\overline{\text{BHE}}$/S_7	The **bus high enable** pin is used in the 8086 to enable the most-significant data bus bits (D_{15}–D_8) during a read or a write operation. The state of S_7 is always a logic 1.

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Minimum Mode Pins:

IO/$\overline{\text{M}}$ or M/$\overline{\text{IO}}$	The IO/$\overline{\text{M}}$ (8088) or the M/$\overline{\text{IO}}$ (8086) pin selects memory or I/O. This pin indicates that the microprocessor address bus contains either a memory address or an I/O port address. This pin is at its high-impedance state during a hold acknowledge.
$\overline{\text{WR}}$	The **write line** is a strobe that indicates that the 8086/8088 is outputting data to a memory or I/O device. During the time that the $\overline{\text{WR}}$ is a logic 0, the data bus contains valid data for memory or I/O. This pin floats to a high-impedance during a hold acknowledge.
$\overline{\text{INTA}}$	The **interrupt acknowledge** signal is a response to the INTR input pin. The $\overline{\text{INTA}}$ pin is normally used to gate the interrupt vector number onto the data bus in response to an interrupt request.
ALE	**Address latch enable** shows that the 8086/8088address/data bus contains address information. This address can be a memory address or an I/O port number. Note that the ALE signal does not float during a hold acknowledge.
DT/$\overline{\text{R}}$	The **data transmit/receive** signal shows that the microprocessor data bus is transmitting (DT/$\overline{\text{R}}$ = 1) or receiving (DT/$\overline{\text{R}}$ = 0) data. This signal is used to enable external data bus buffers.
DEN	**Data bus enable** activates external data bus buffers.

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Minimum Mode Pins:

TABLE Bus cycle status (8088) using $\overline{SSO}$

IO/$\overline{M}$	*DT/$\overline{R}$*	*$\overline{SSO}$*	*Function*
0	0	0	Interrupt acknowledge
0	0	1	Memory read
0	1	0	Memory write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	I/O read
1	1	0	I/O write
1	1	1	Passive

HOLD The **hold** input requests a direct memory access (DMA). If the HOLD signal is a logic 1, the microprocessor stops executing software and places its address, data, and control bus at the high-impedance state. If the HOLD pin is a logic 0, the microprocessor executes software normally.

HLDA **Hold acknowledge** indicates that the 8086/8088 microprocessors have entered the hold state.

$\overline{SSO}$ The $\overline{SSO}$ status line is equivalent to the S_0 pin in maximum mode operation of the microprocessor. This signal is combined with IO/R and DT/R to decode the function of the current bus cycle (refer to Table).

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Maximum Mode Pins:

$\overline{S2}$, $\overline{S1}$, and $\overline{SO}$	The **status bits** indicate the function of the current bus cycle. These signals are normally decoded by the 8288 bus controller described later in this chapter. Table shows the function of these three status bits in the maximum mode.
$\overline{RO}$/$\overline{GT1}$ and $\overline{RO}$/$\overline{GT0}$	The **request/grant** pins request direct memory accesses (DMA) during maximum mode operation. These lines are both bi-directional and are used to request and grant a DMA operation.
$\overline{LOCK}$	The **lock output** is used to lock peripherals off the system. This pin is activated by using the LOCK: prefix on any instruction.
QS_1 and QS_0	The **queue status** bits show the status of the internal instruction queue. These pins are provided for access by the numeric coprocessor (8087). Refer to Table for the operation of the queue status bits.

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Maximum Mode Pins:

TABLE Bus control functions generated by the bus controller (8288) using $\overline{S2}$, $\overline{S1}$, and $\overline{SO}$

$\overline{S2}$	$\overline{S1}$	$\overline{SO}$	*Function*
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

TABLE Queue status bits

QS_1	QS_0	*Function*
0	0	Queue is idle
0	1	First byte of opcode
1	0	Queue is empty
1	1	Subsequent byte of opcode

Thank you